Sequential switching shunt regulation using DC transformers for solar array power processing in high voltage satellites

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***Abstract*—This paper proposes a solar array regulation technique for a high-voltage satellite power bus. The regulation method combines on-off control at low frequency, i.e. kHz range, of highly efficient isolated and unregulated dc-dc converters operating at high frequency, i.e. hundreds of kHz. Although this technique can adopt different implementations, this paper deals with a hysteretic voltage control loop at low frequency, also known (Sequential Switching Shunt Regulator - S3R), and unregulated, isolated, current-fed, zero-voltage and zero-current push-pull dc-dc converters. Design guidelines and experimental validation are provided.**

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ACRONYMS

BCR: Battery Charge Regulator.
BCDR: Battery Charge Discharge Regulator.
BDR: Battery Discharge Regulator.
DC: Direct Current.
DC-DC: Direct Current to Direct Current.
DCX: Direct Current Transformer.
DET: Direct Energy Transfer.
ECSS: European Cooperation for Space Standardization.
EP: Electrical Propulsion.
EPC: Electronic Power Conditioner.
GEO: Geostationary Orbit.
HV: High Voltage.
LEO: Low Earth Orbit.
LV: Low Voltage.
MEA: Main Error Amplifier.
MPP: Maximum Power Point.
MPPT: Maximum Power Point Tracking.
PCU: Power Conditioning Unit.
PPU: Power Processing Unit.
SAS: Solar Array Section.
S3DCX: Sequential Switching Shunt DCX Regulator.
S3R: Sequential Switching Shunt Regulator.
SSR: Switching Shunt Regulator.
TWTA: Travelling Wave Tube Amplifier.
ZCS: Zero Current Switching.
ZVZC: Zero Voltage Zero Current.
ZVS: Zero Voltage Switching.

I. INTRODUCTION

Solar array regulation is a critical power conversion function for any spacecraft. Two main methods are dominant nowadays: Maximum Power Point Tracking (MPPT) DC-DC converters and Switching Shunt Regulators (SSRs). While the first approach is typical in low and medium-power Low Earth Orbit (LEO) and interplanetary missions using unregulated bus architectures, the second method is widely used in medium and high-power satellites for Geostationary Orbit (GEO) satellites using fully regulated bus architectures, being the Sequential Switching Shunt Regulator (S3R) [1-4], the most common SSR employed. The fully regulated bus is realized by the Power Conditioning Unit (PCU), which integrates the SSR, the Battery Charge Regulator (BCR) and the Battery Discharge Regulator (BDR), as represented in figure 1, [5, 6]. In the European Space

standard [7], 100V-120V DC bus voltage is recommended for power levels higher than 8kW, hence, most of the space companies have adapted their products to this voltage for the largest platforms. However, 100V starts to be inadequate for the actual needs, since the most powerful platforms already reach 20-25kW, also motivated by the use of high-power Electrical Propulsion (EP) systems [8]. Large bus current lead to high mass harness and considerable DC losses, but also impacts on the maximum bus impedance (Z_{bus}) and bus capacitor (C_{bus}) [7]. Further, EP systems require high-power, high-voltage supplies, which are provided by the Power Processing Units (PPUs) directly connected to the regulated bus. Two-level power conversion results in a penalty on efficiency and with obvious consequences on the thermal design, size and mass. Besides, other systems, such as Electronic Power Conditioners (EPCs) for Travelling Wave Tube Amplifiers (TWTAs), also demand high-voltage supplies and could benefit of high voltage bus.

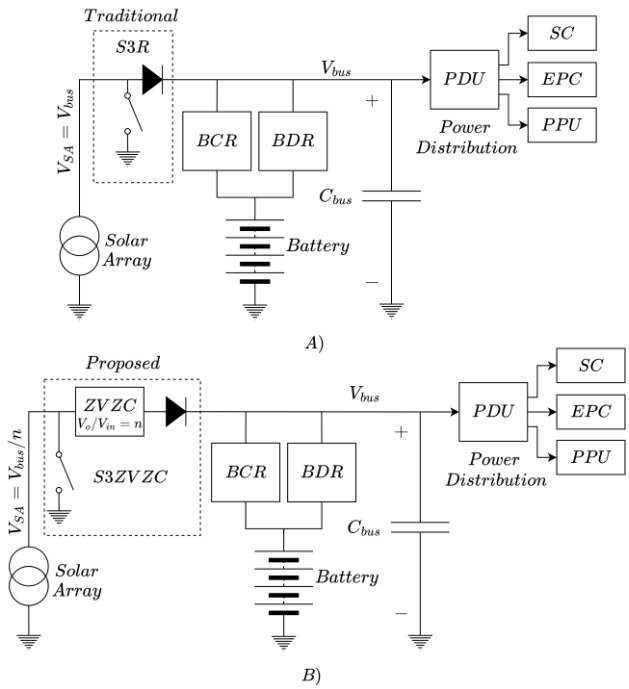

Fig. 1. High-power spacecraft electrical architecture: a) traditional [5] b) proposed approach.

As a result, a higher bus voltage, around 300V, is being considered, and two main approaches have been pondered to address its implementation. In [9], the solar array voltage is increased up to 300V-350V, and a Direct Energy Transfer (DET) connection from the solar generator to the electric thruster is suggested. The Battery Charge Discharge Regulator (BCDR) controls the bus voltage. While it is a conceptually simple solution, there are relevant technical challenges associated with the high-voltage solar array, such as, arcing due to differential charging of the different materials, high-voltage slip rings, qualification and cost [9]. Furthermore, it is a costly solution that requires full requalification of the solar array if the bus voltage is changed. In [10], a two-stage approach is proposed for an ion-thruster supply with MPPT tracking. The main advantages of this approach are the simplicity and heritage, since only well-known power regulators are used for its implementation. Besides, it exhibits very good regulation for large power transients that happen in ion-thrusters. The main disadvantage is the efficiency penalty due to S3R diodes and the Weinberg converter losses.

In [11] a two-bus approach is presented, implementing a High-Voltage bus (HV_{bus}) at 450V, and Low-Voltage bus (LV_{bus}) at 100V, featuring an integrated power processing DC-DC converter. The power cell can operate in different operating modes, including MPPT and bus regulated for both busses, HV_{bus} and LV_{bus}. However, it requires a complex power processing DC-DC converter and control, making the practical implementation difficult with space-qualified electronic parts.

In this work, a different approach for the solar array regulator is proposed. It uses highly efficient, isolated, unregulated, constant gain, high-frequency DC-DC converter, also known as “DC-Transformer” (DCX). The DCXs, switching at hundreds of kHz or more, are controlled as traditional S3R power cells at low frequency, i.e. kHz range, [1,12]. This concept is adaptable to any regulated or unregulated bus.

The proposed Switching Sequential Shunt Regulator using DCX (S3DCX) has the following benefits when compared to the existing solutions: a) It is a simple concept that can be implemented with different DCX topologies, allowing voltage decoupling between solar array and distribution bus, which overcomes the limitations of the direct energy transfer regulators and provides increased flexibility in solar array design; b) Higher (or lower) bus voltage could be achieved with very high efficiency (>95%) end to end; c) It can be used as direct replacement of the S3R with minimum changes in regulated or unregulated bus architectures and variations; d) It is highly modular and accepts parallel and series connection of isolated secondary sides to achieve higher current and voltage.

The design of BCRs and high-power BDRs [13,14] are topics already discussed in the literature, therefore, these will not be covered in this work.

The rest of this article is organized as follows: Section II introduces the S3DCX power cell as well as a particular implementation and modeling of the regulator. Section III details the design and simulation of the S3DCX for a 300V-2kW prototype. Section IV details the experimental

validation of the proposed prototype and discusses the results. Finally, Section V concludes this article.

II. S3DCX: POWER CELL AND REGULATOR

Different DCX topologies have been proposed for industrial, medical, telecommunications and many other areas. Resonant techniques [15], and particularly the LLC converter [16, 17], have been widely accepted, but these are mostly oriented to have regulated outputs with complex control loops. Another type of unregulated DCX with Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) are described in [18] and [19]. Both converters use the magnetizing current of the transformer to achieve ZVS for all switches, but the method to achieve ZCS is slightly different. In [18], the leakage inductance of the transformer resonates with the output capacitor to achieve ZCS without any inductor. In [19], the converter is current-fed and the resonant circuit is formed by the leakage inductance and a resonant capacitor placed at the input. A fundamental feature of these DCXs is that the conversion gain is just the transformer turns ratio, so they are very simple and robust to parameter drifts. A detailed analysis of those types of DCX can be found in [20]. In the case at hand, the method proposed in [19] is better suited than the one described in [18], because a photovoltaic source inherently behaves as a current source below its Maximum Power Point (MPP). This is also reinforced by the fact that the solar array harness inductance is relatively large in high-power satellites. Besides, a large capacitor is required as the main bus capacitor at the secondary side to fulfill the output impedance requirements [7]. As discussed in [20], any dual-ended topology is suitable, but current-fed ZVZC push-pull is widely used in satellite applications, mainly in EPC for TWTA [19]. Hence, this converter topology, represented in figure 2, is selected as DCX for this work. Briefly, the main benefits of the selected DCX are: a) Galvanic isolation provides easy adjustment of required output by transformer turns ratio and possibility of secondary side output connections (series and parallel); b) It takes advantage of the natural solar array behavior and harness inductance to have a nearly constant current source; c) It uses for its advantage all the parasitic elements of the transformer in a resonant manner, resulting in a very compact, simple, lightweight, and high efficiency solution; d) All power semiconductors are operated in ZVS and ZCS; e) ZVS and ZCS (neglecting magnetizing current) are load independent in a wide range; f) Simple and low loss gate drive (rad-hard driver implementation is not linked to any complex driver integrated circuit); g) Good power semiconductor utilization (>75% equivalent duty cycle); h) Operation at fixed frequency and duty cycle (very simple and robust drive pulse generation); i) Reduced number of components; j) Very low EMI.

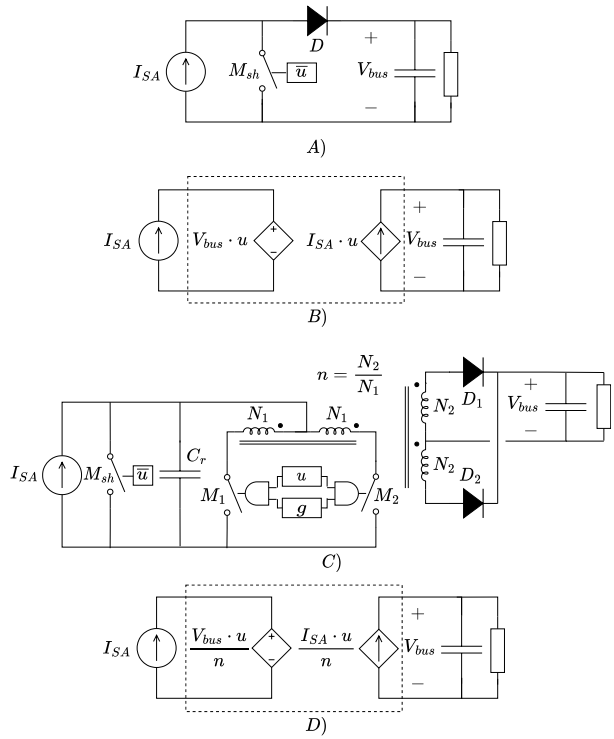

Fig. 2. DET and DCX (current-fed ZVZC push-pull) power cells and averaged models.

Figures 2A and 2B represents the schematic and the large signal averaged model for the DET shunt regulator, respectively, and figures 2C and 2D shows the circuit schematic and averaged model of the proposed DCX. The control signal, *u*, dictates the power transfer from the solar array to the main bus in both cases (1), but the working principle is slightly different. When *u=1*, in the DET case, the transistor M_{sh} is off and the diode D connects the solar array section to the bus, while in the DCX, the M_1 and M_2 driving pulses, *g*, operating at switching frequency, f_s, enable the power transfer. When *u=0*, the transistor M_{sh} shunts the solar array in the DET and the DCX power cells. An important difference is that DCX allows voltage and current conversion ratio (gain is transformer turns ratio, *n*) when it transfers power to the bus, as it can be noted in the DCX averaged model. The main waveforms of the power cells are represented in figure 3. Although M_1 and M_2 can be used to perform power control transfer, *u*, and therefore one transistor is saved, M_{sh} simplifies current limiting during shunt operation.

$$u(t) = \begin{cases} 1 & : SA \quad power \quad transfer \\ 0 & : SA \quad shunted \end{cases} \tag{1}$$

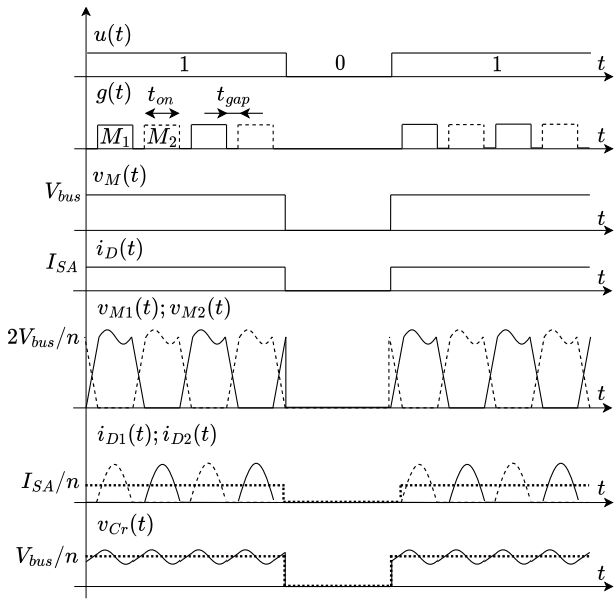

Fig. 3. DET and DCX main waveforms sketch.

$\langle V_{Cr} \rangle = V_{bus}/n$, implying that the solar array operating point, and therefore, the power injected to the bus, can be controlled by the bus voltage in closed loop operation.

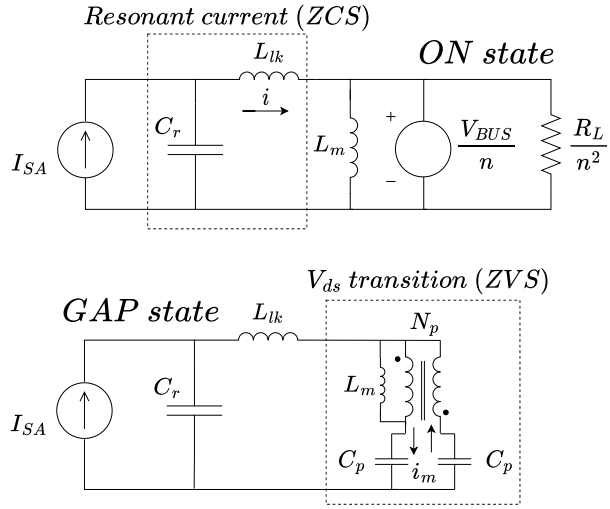

Fig. 4. DCX equivalent circuits for ON and GAP states

The working principle of the DCX can be explained with the two equivalent circuits shown in figure 4. During the ON state, i.e. M_1 or M_2 is in conduction, a resonant switch current occurs due to the resonant circuit formed by the resonant capacitor, C_r, and the transformer leakage inductance, L_{lk}. During the GAP state, i.e. M_1 and M_2 are turned-off, the magnetizing current charges and discharges all the parasitic capacitances, i.e. MOSFETs, diodes and transformer.

The analysis of the ON state circuit results in the resonant current, i, whose governing differential equation is given by (2). MOSFET current is $i_M = i - i_m$, being i_m, the magnetizing current and diode current is $i_D = i_M/n$.

$$L_{lk} C_r \frac{\partial^2 i}{\partial t^2} + i = I_{SA} \tag{2}$$

On the other hand, the analysis of the GAP state results in the governing differential equation (3), where the resonant circuit is formed by the magnetizing inductance, L_m, and the parasitic capacitance, C_p, given by (4). C_M is the parasitic MOSFET capacitance, C_{TR} is the parasitic transformer capacitance and C_D is the diode capacitance referred to the primary side.

$$L_m C_p \frac{\partial^2 i_m}{\partial t^2} + \frac{i_m}{2} = 0 \tag{3}$$

$$C_p = C_M + C_{TR} + C_D \cdot n^2 \tag{4}$$

The detailed design procedure to solve (2) and (3) for ZVS and ZCS conditions can be found in the appendix. It is clear from the ON state equivalent circuit that

Satellite solar arrays are typically divided into several sections, i.e., an arrangement of several solar cell strings in parallel. In the proposed regulator, each section is attached to one DCX, please refer to figure 2c. In a sequential control scheme, some DCX converters are permanently ON providing power to the bus, while others DCX are OFF and only one DCX is turning ON and OFF to eventually perform output voltage regulation. This can be achieved by sequential hysteretic control [1] as illustrated in figure 5, and being this scheme one of the most common methods employed in solar array regulation for medium and large satellites.

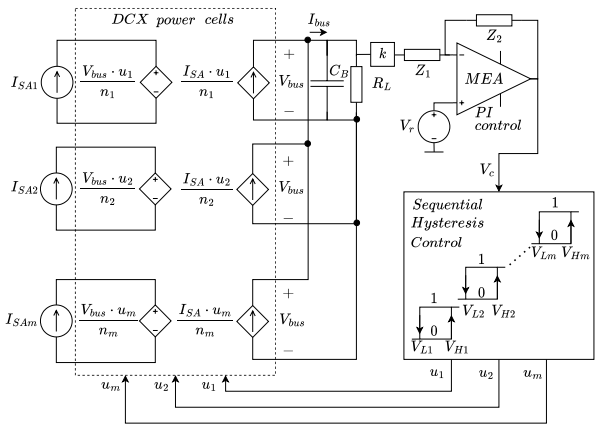

Fig. 5. S3DCX: Sequential hysteresis control scheme

The linearized model of the S3DCX regulator is given by (5), resulting in a voltage-controlled current-source that supplies the main bus capacitor, represented in figure 6.

The voltage loop gain, $T_v(s)$ and the closed-loop output impedance $Z_O(s)$ are given by (6) and (7), respectively.

$$G = \frac{I_{bus}}{V_c} = \frac{\sum_{i=1}^{m} I_{SAi}/n_i}{V_{Hm} - V_{L1}} \tag{5}$$

$$T_v(s) = kG\frac{k_p(s + k_i/k_p)}{s}\frac{1}{C_B(s + (1/R_L C_B))} \tag{6}$$

$$Z_O(s) = \frac{\widetilde{v_o}}{\widetilde{i_o}} = \frac{1}{C_B(s + (1/R_L C_B))[1 + T_v(s)]} \tag{7}$$

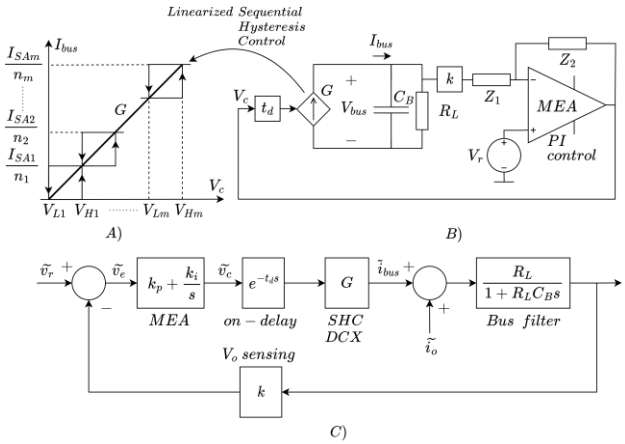

Fig. 6. S3DCX: a) Linearized sequential hysteresis control; b) Small-signal linear model; c) Voltage feedback loop

To avoid phase and gain margin degradation, [21], the regulator turn-on delay, t_d, must be smaller than $1/\omega_c$, being ω_c the crossover frequency of the loop gain (6), $|T_v(j\omega_c)|=1$.

The closed loop output impedance is constrained by the output impedance mask, defined in the standard [7], clause 5.7.2.o.

III. DESIGN, SIMULATION AND PROTOTYPE IMPLEMENTATION

A 2kW, five power-cell S3DCX regulator has been designed, simulated and implemented. Detailed step-by-step calculations are included in the appendix.

A. Design

The main characteristics of the S3DCX regulator and the solar array simulator are summarized in table 1.

TABLE I
S3DCX: main design parameters

Description	Value	Comment
Solar array section (SAS) – Agilent E4351B simulator		
V_{OC}	120V	Open-circuit voltage
V_{MP}	110V	Maximum power voltage
I_{SC}	4A	Short-circuit current
I_{MP}	3.9A	Maximum power current
P_{MP}	429W	Maximum power
C_{SAS}	200nF	Agilent E4351B
L_h	33µH	Added inductance
DCX transformer – push-pull ($N_1=N_{1a}=N_{1b}$; $N_2=N_{2a}=N_{2b}$)		
Core	RM14	Material 3C95
$n=N_2/N_1$	15/5	V_{SAS}=100V; V_O=300V
DCX & shunt – circuit		
C_r	0.5 µF	CB182G0105J
M_1; M_2; M_{sh}	IXTQ42N25P	Si MOSFET (250V, 42A)
D_1; D_2	STPSC10H12	SiC diode (1.2kV, 10A)
t_{on}	2.8µs	f_s=135kHz; D=0.378
t_{gap}	0.9µs	f_{output}=270kHz
R_{cl}	50mΩ	Max shunt current= 14A
Control loop		
k	$4.08\cdot10^{-3}$	ADUM3190, V_{ref}=1.225V
k_p	298.8	Split into three stages
k_i	$97.96\cdot10^{3}$	
t_d	< 25µs	
G	1.11	
R_L	> 45Ω	P_{Omax}=2kW; V_O=300V
C_{BUS}	400µF	B32778G1206K000

Based on the simplified transformer circuit model shown in figure 7, measured parameters for the five transformers are included in table 2. These parameters are, magnetizing inductance L_m, leakage inductance L_{lk}, parasitic capacitance of the transformer C_{TR}, resistance of the primary R_1 and secondary winding R_2 and resonant frequency f_{res}.

TABLE II
S3DCX: transformer characterization

L_m [µH]	L_{lk1} [nH]	L_{lk2} [nH]	C_{TR} [pF]	R_1 [mΩ]	R_2 [mΩ]	f_{res} [kHz]
172.8	650	680	235	9.7	41.6	789
174.5	680	610	211	9.1	40.9	830
169.7	765	690	174	9.3	41.6	925
168.9	590	625	162	11.8	41.2	962
165.1	590	630	201	13.1	41.9	874

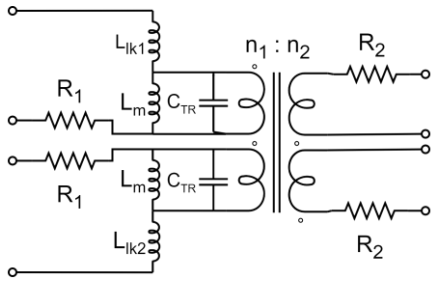

Fig. 7. S3DCX: Transformer equivalent circuit model.

B. Simulation: switching and large-signal averaged models

Computer simulation models have been implemented for both, switching and large-signal averaged versions. The output impedance of the S3DCX, which meets the impedance mask required by the European space standard [7], clause 5.7.2.o., is represented in figure 8.

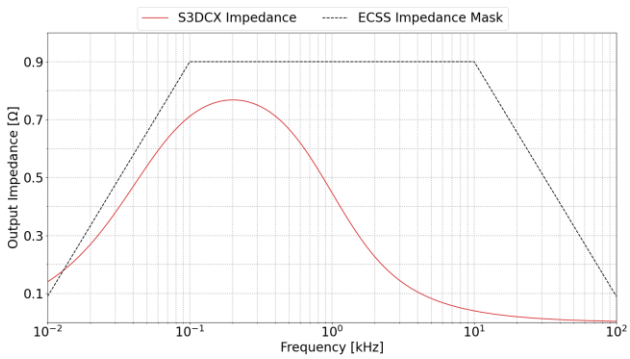

Fig. 8. S3DCX output impedance and ECSS impedance mask [7].

A half bus power load step simulation is shown in figure 9. Nominal bus voltage ripple and bus voltage transient meet the European space standard [7], clauses 5.7.2.m and 5.7.2.i.1, respectively.

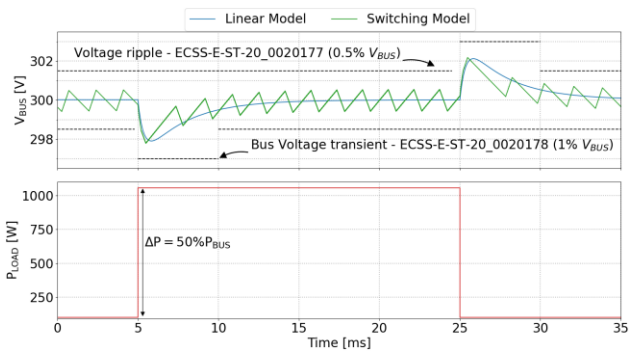

Fig. 9. S3DCX transient response simulation results. Top figure: Output voltage (switching and large-signal averaged models). Bottom figure: power load step.

The S3DCX prototype is shown in figure 10. The five DCXs are identical, and the output connections are hard-wired to allow independent or series connections to the output bus capacitor, which is external and not shown in the figure. The main error amplifier, MEA, is implemented using an isolated error amplifier, and t_{on} and t_{gap} signals are obtained using only discrete electronic parts.

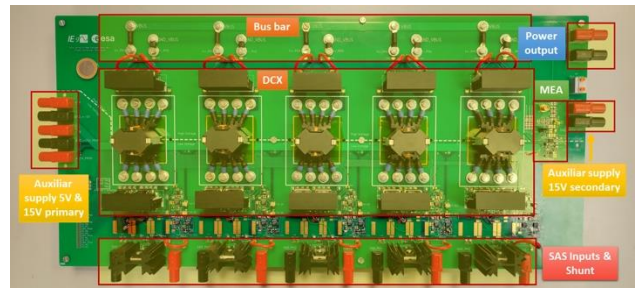

Fig. 10. S3DCX prototype: 2kW, five power cells.

IV. EXPERIMENTAL VALIDATION

Several tests have been carried out to validate the proposed solar regulation concept using independent and series configurations at the output of the regulator, as represented in figure 11.

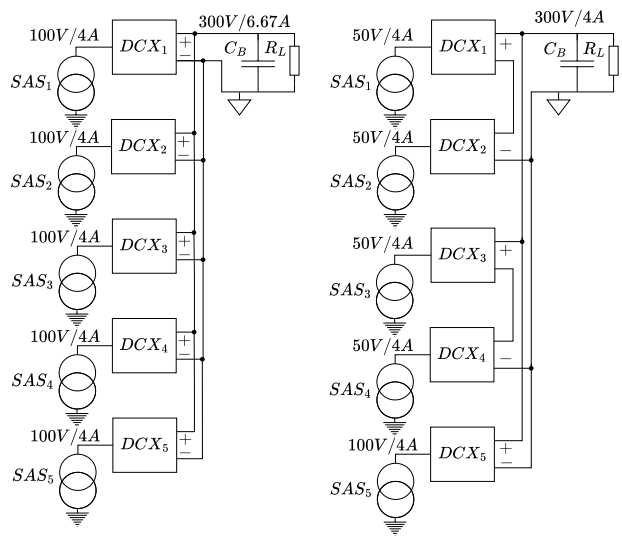

Fig. 11. Left figure: S3DCX five-independent output configuration. Right figure: Two solar array sections with two DCX in series and one independent.

A. DCX: shunt and ZVZC operation

Figure 12 shows the detail of the ON (u=1) and OFF (u=0) of the DCX. It is clearly observed from the MOSFET voltage and diode current that ZVS and ZCS are achieved even during the transients. Besides, on-delay,

t_d, is limited to 18µs. It can be also noticed that the shunt transistor goes into current limitation mode during the OFF action to discharge the parasitic capacitance of the solar array and the resonant capacitor of the DCX.

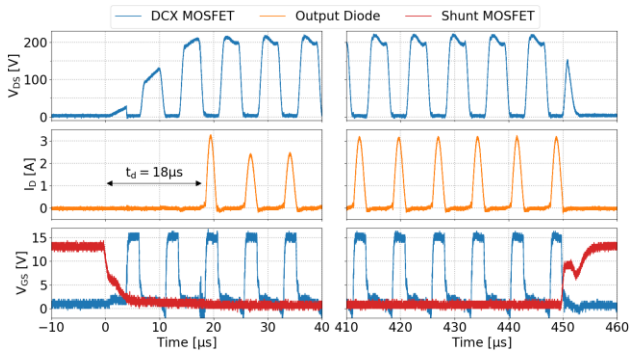

Fig. 12. Left: DCX ON detail. Right: DCX OFF detail. Top: V_{DS} M_1, Middle: I D_1, Bottom: Blue trace: V_{GS} M_1, Red trace: V_{GS} shunt transistor.

B. DCX: efficiency

The efficiency of each DCX has been measured at different solar array currents, which could represent different irradiance levels or different solar array orientation, please refer to table III. Efficiency measurements also include power consumption of ancillary electronics and is close to 95.5% in nominal operation.

TABLE III
DCX: efficiency measurements

I_{SAS} [A]	DCX1 [%]	DCX2 [%]	DCX3 [%]	DCX4 [%]	DCX5 [%]
1	92.5	92.5	92.0	91.9	92.0
2	95.3	95.2	94.8	94.8	94.8
3	95.9	95.3	95.5	95.4	95.5
4	95.8	95.8	95.4	95.1	95.3

C. S3DCX: voltage regulation

Figure 13 illustrates the regulator's response under a 1kW load power step, from 100W to 1.1kW (50% of the bus power). The configuration of the S3DCX is the one indicated in figure 11 (left). At the beginning, DCX 1 is regulating the output voltage and the rest of DCX are fully off. Once the load step happens, DCX 1 and DCX 2 go to fully on and DCX 3 regulates the output voltage. As it can be observed in the AC bus voltage waveform (bottom), the steady state bus voltage ripple does not exceed the 0.5% of the nominal bus voltage (1.5V) and the peak values during load transients are within 1% of the bus voltage (3V). Bus voltage steady state is reached in less than 5ms.

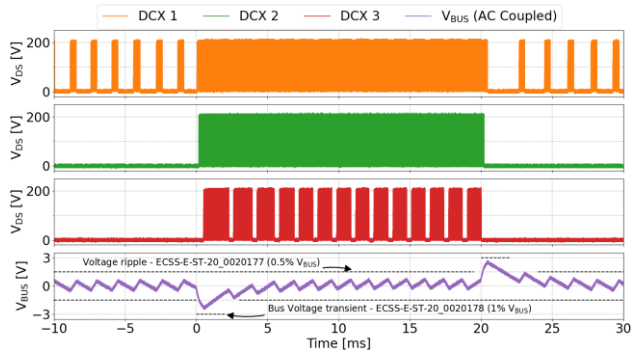

Fig. 13. S3DCX voltage regulation. Top: DCX 1: V_{DS} M_1; Middle-top: DCX 2: V_{DS} M_1; Middle-bottom: DCX 3: V_{DS} M_1; Bottom: bus voltage (AC coupled).

D. S3DCX: output series connection – voltage regulation

Figure 14 illustrates the operation of the regulator with the configuration represented in figure 11 (right) under a step load of approximately 500W. At the beginning, DCX 3 and DCX 4 are regulating the bus voltage and the load step forces the operation of DCX 5. It is important to note that DCX 3 and DCX 4 are accommodating 50V solar sections and, DCX 5 at 100V solar section, as it can be observed from the voltage measured in the resonant capacitor, C_r, of each DCX.

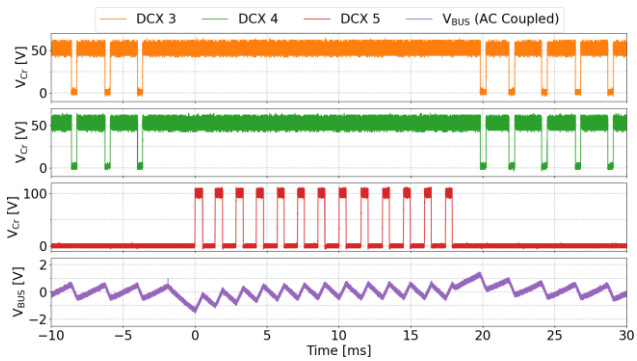

Fig. 14. S3DCX voltage regulation – output series connection. Top: DCX 3: V_{Cr}; Middle Top: DCX 4: V_{Cr}; Middle Bottom: DCX 5: V_{Cr}; Bottom: bus voltage (AC coupled).

E. S3DCX: output series connection – unbalanced solar array currents

The last results show the proper operation of the regulator with output series connection and unbalanced solar array currents. The regulator has been configured as represented

in figure 11 (right), but SAS 2 reduces its current to I_{SC}=3.2A and I_{MP}=3A. As depicted in figure 15, as the output current is limited, the operating point of the solar sections adjust to a value where both currents are equal. This effect is clearly shown in figure 16, where SAS 1 and SAS 2 exhibit different voltages, either during regulation or fully-on operation modes. It is also worth to note, that SAS 3 operates at the nominal value, since SAS 3 and SAS 4 are not unbalanced. Thus, it is important to remark that DCX output series connection is possible, with no loss of ZVZC conditions, even with unequal I-V curves of the solar array.

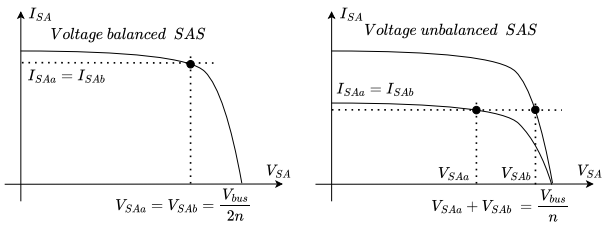

Fig. 15. Sketch of balanced and unbalanced solar array sections in output series connection.

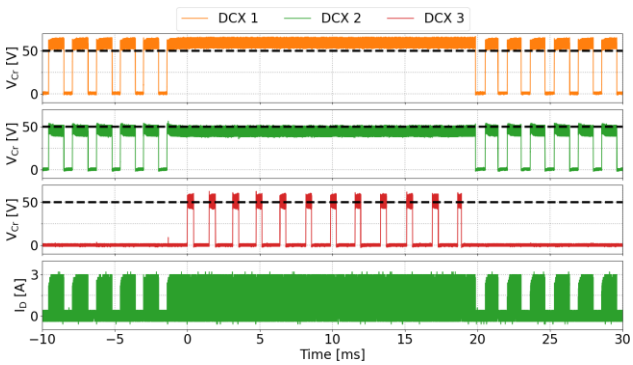

Fig. 16. S3DCX voltage regulation – output series connection and unbalanced solar array currents. Top: DCX 1: V_{Cr}; Middle Top: DCX 2: V_{Cr}; Middle Bottom: DCX 3: V_{Cr}; Bottom: DCX 1: I D_1.

V. CONCLUSION

This paper introduces a different concept for solar array regulation that solves some of the problems associated to direct energy transfer regulators commonly used in bus regulated satellites. The use of the proposed DCX topology provides two degrees of freedom for regulating bus voltage: transformer turns ratio, and output series connection of individual solar array sections, offering true adaptability to accommodate different types of solar arrays. Although this concept has been validated for a high voltage bus at 300V, assuming step-up voltage conversion, other approaches are possible. Design example, computer simulation and experimental prototype has been also included in this paper to show the operating principles of the proposed regulator. Next steps include higher bus voltage (600V and 900V), miniaturization of DCX increasing switching frequency (GaN power semiconductors and planar magnetics) and digital implementation (control and pulse-width modulated gate signals).

APPENDIX

Design guidelines: ZVZC converter

1) Estimate the parasitic capacitance, C_p (2), from power semiconductors and transformer.

$$\begin{aligned} &C_M \approx 500pF \\ &C_{TR} \approx 300pF \\ &C_D \approx 100pF \\ &C_p = C_M + C_{TR} + C_D \cdot n^2 \approx 1.7nF \end{aligned} \quad \text{(A-1)}$$

2) Definition of the magnetizing current, i_m, as a percentage of the input current. An initial tentative of 20% of input current is considered. Low values i_m means larger transformers and longer t_{gap}, but lower transformer losses and better ZCS transitions.

$$i_m = 0.2I_{SA} = 0.8A \quad \text{(A-2)}$$

3) Estimation of required gap time to charge the parasitic capacitance, t_{gap}, and estimation of on time, t_{on}, as a percentage of t_{gap} to maximize power transfer. Estimation of switching frequency, f_s.

$$t_{gap_{min}} > \frac{4V_{bus}C_p}{i_m n} = 0.85\mu s \quad \text{(A-3)}$$

$$t_{on} \approx \frac{t_{gap_{min}}}{0.3} = 2.85\mu s \quad \text{(A-4)}$$

$$f_s = \frac{1}{2(t_{on} + t_{gap})} = 135kHz \quad \text{(A-5)}$$

4) Estimation of magnetizing inductance, L_m. and transformer design.

$$L_m = \frac{V_{bus}t_{on}}{2i_m n} = 178\mu H \quad \text{(A-6)}$$

5) Transformer design. From the above inputs, a RM14/I core and 3C95 material with five turns on primary, n_1=5, and fifteen turns on secondary, n_2=15 is considered. Measured values of five transformers will result in the following values (average of five measured transformers).

$$\begin{aligned} &L_M \approx 170\mu H \\ &C_{TR} \approx 200pF \\ &L_{lk} \approx 650nH \end{aligned} \quad \text{(A-7)}$$

6) Check if the transformer values are consistent with the original design and go back to step 1, if necessary.

7) Gap time, t_{gap}, calculation from measured values and using the following expressions

$$\begin{aligned} t_{gap} &= \frac{1}{\omega_{gap}}\left(\arcsin\left[\frac{8L_m\cos(\theta)C_p\omega_{gap})}{t_{on}}+\sin(\theta)\right]-\theta\right)=0.9\mu s \\ \omega_{gap} &= \frac{1}{\sqrt{L_m C_p}} \\ \tan(\theta) &= \frac{-2}{\omega_{gap} t_{on}} \end{aligned} \quad \text{(A-8)}$$

8) Calculation of resonant frequency, ω_r, to satisfy zero current switching condition. Resonant frequency is found by numerical methods.

$$\begin{aligned} &\cos(\omega_r t_{on}) - \omega_r \frac{t_{gap}}{2}\sin(\omega_r t_{on}) = 1 \\ &f_r = \frac{\omega_r}{2\pi} \approx 300kHz \end{aligned} \quad \text{(A-9)}$$

9) Calculation of resonant capacitor, C_r.

$$C_r = \frac{1}{\omega_r^2 L_{lk}} \approx 500nF \quad \text{(A-10)}$$

Design guidelines: S3ZVZC MEA

10) Definition of maximum bus voltage ripple as per ECSS-E-ST-20C Rev.2, clause 5.7.2.m.

$$\begin{aligned} &\Delta V_{bus|pp} < 0.5\% V_{bus} \\ &\Delta V_{bus|pp} = 1V \end{aligned} \quad \text{(A-11)}$$

11) Definition of bus capacitance as per ECSS-E-ST-20C Rev.2, clauses 5.7.2.m and 5.7.2.o.

$$C_{bus} = 400\mu F \quad \text{(A-12)}$$

12) Definition of MEA voltage reference, V_{ref}, and voltage feedback gain, K. V_{ref} is given by the internal voltage reference of the isolated error amplifier.

$$V_{ref} = 1.225V \quad \text{(A-13)}$$

$$K = V_{ref}/V_{bus} = 4.083 \cdot 10^{-3} \quad \text{(A-14)}$$

13) Definition of the hysteresis of the comparator and the transconductance of the regulator, G. Hysteresis voltage is selected as a function of the voltage supply rail and number of power cells. If the upper limit of the k cell is equal to the lower limit of the $k + 1$ cell, and the transformer turns ratio of all power cells are the same, n, the transconductance of regulator is simply the transconductance of one power cell.

$$V_{Hi} - V_{Li} = V_{HL} = 1.2V \quad \text{(A-15)}$$

$$G = I_{SA}/(n \cdot V_{HL}) = 1.11A/V \quad \text{(A-16)}$$

14) Calculation of proportional gain and integral term of the MEA, k_p and k_i, respectively, k_i is adjusted to be one decade below the crossover frequency of the voltage loop.

$$K_p = \frac{V_{HL}}{K\Delta V_{bus|pp}} = 293.88 \quad \text{(A-17)}$$

$$k_i = k_p\frac{\omega_c}{10} = \frac{k_p^2 KG}{10C_{bus}} = 97.96 \cdot 10^3 s^{-1} \quad \text{(A-18)}$$

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