Design of Cyclic Correlator for Channel Estimation in DTMB System

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Abstract
In this paper, a cyclic-correlation based channel estimator is implemented for DTMB system. It exploits the quasi-cyclic structure of PN guard interval in DTMB system to obtain channel estimation results. Under SMIC 0.18μm standard CMOS technology, the proposed correlator can stably work at the frequency of 60MHz, and the circuit area is about 152k gates. Computational simulation shows that the proposed scheme has comparable performance with FFT-based channel estimator. Implementation results demonstrate that more than 3800 clock cycles and 82% design complexity reduction can be achieved without loss in performance of rms AMSE.

Keywords: Correlation, channel estimation, DTMB, PN sequence, FFT/IFFT

1. Introduction:
DTMB[1] (Digital Terrestrial / Television Multimedia Broadcasting), the standard of Chinese digital television broadcasting, has recently been released, within which TDS-OFDM(Time Domain Synchronous OFDM) is regarded as a critical technology. Generally, OFDM is widely used as a modulation technique for broadband communication systems, which efficiently mitigates the multipath interference and renders a better performance of demodulation by inserting cyclic prefix (CP) between two consecutive frames. However, pilots, used to process channel estimation, either employed in time domain or frequency domain, will inevitably reduce the capacity or bandwidth efficiency of the system. In TDS-OFDM scheme, a cyclic pseudo-noise sequence, defined as the frame head, is inserted before the beginning of the frame body to perform as the guard intervals to combat ISI as well as the training sequences for channel estimation. Good autocorrelation property of PN sequence makes it an excellent choice for channel estimation. In addition, it improves the bandwidth efficiency of system by replacing both CP sequence and training symbols.

In [2], a channel estimation scheme by using FFT/IFFT operation is proposed for DTMB system. The received signals and demodulated PN sequence are transformed into frequency domain using FFT, followed by a complex number multiplication between the both. However, this method inevitably introduces two FFT processors and one corresponding IFFT processor, which leads to a large processing duration and complexity of the receiver. Therefore, we attempt to find out an alternative of channel estimation method in time domain.

In this paper, after verifying the equivalence of channel estimation between time domain method and frequency domain method, we proposed a novel correlation-based structure in time domain. The received signal cyclically correlates with the local PN255 (8 orders PN) sequence to estimate the channel impulse response. Since the value of PN sequence is either zero or one, being modulated into \(1+i\) or \(-1-i\) before transmitted, multiplexers and additions are adopted instead of complex multiplier in this design by demapping \(1+i\) into zero or one. This design bypasses multiplication by multiplexers and addition/subtraction saves nearly 3800 clock cycles and 10 percents registers.

This paper is organized as follows. The introduction on the method of channel estimation for DTMB system is given. Section 2 provides the equivalence verification on cyclic correlation both in time domain and frequency domain. The implementation of the cyclic correlator is carried out in Section 3. Finally, conclusions are given in Section 4.

2. Equivalence Verification
In DTMB system, PN sequence, inserted before each frame body as the frame head, achieves a quasi-cyclic form by combining two overlapped PN255. Fig. 1 shows the structure of frame head where both PN_255_1 and PN_255_2 represent 8 orders PN sequence.

\[ R_{y_p}(n) = \sum_{i=0}^{N-1} p^*(i)y(n+i) \]

where \(p^*\) denotes conjugation for the operation data are complex numbers. \(y(n)\) can be expressed by the convolution between transmitted signal \(s(n)\) and channel impulse

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response $h(n)$. The auto-correlation of PN sequences $R_{pp}$ has the following value

$$R_{pp}(n) = \sum_{i=0}^{M-1} p(i)p((n+i)\mod N) = \begin{cases} M, & n = 0 \\ -1, & n = 1,2,...,M-1 \end{cases}$$ (2)

The value with $n \neq 0$ has little interference after normalized. Therefore, the correlation between received signal and locally generated $p(i)$ that expressed in equation (1) can be used as channel impulse response $h(n)$ in the receiver equalization part.

Assume that $k=i+n$, then equation (1) can be rewritten as

$$R_{pp}(n) = \sum_{k=-\infty}^{n-M} p(k) y(k) = \sum_{k=0}^{M-1} p(-(k-n)) y(k)$$ (3)

Here, we define:

$$\hat{p}^*(i) = p^*(-i), \quad i = 0,1,...,M-1$$ (4)

Then the equation (3) can be rewritten as

$$R_{pp}(n) = \sum_{k=0}^{M-1} \hat{p}^*(n-k) y(k)$$ (5)

From equation (5), we can see that $R_{pp}$ can be obtained by cyclic convolution between $\hat{p}(i)$ and $y(n)$. We conduct $Y(m)$ and $\hat{P}(m)$ are respectively the N-point FFT of $y(n)$ and $\hat{p}(i)$ being zero-padded to the length of N. The channel estimation $h(n)$ (here can be replaced by $R_{pp}$) is given by

$$R_{pp}(m) = IFFT\{Y(m)\hat{P}(m)\}, \quad 0 \leq m \leq M-1$$ (6)

According to the deduction, both cyclic correlation computes in time domain and FFT estimation in frequency domain could obtain channel impulse response. Matlab results are shown in Fig. 2. Simulation uses M frames to compute the root mean square (RMS) value of the average mean error which is approximated as

$$rms \ AMSE = \left[ \frac{1}{M} \sum_{k=1}^{M} (\hat{h} - h)^2 \right]^{1/2}$$ (7)

where $\hat{h}$ and $h$ respectively represents the estimated and the ideal channel response. The simulations use the multi-path channel model (Table III) with additive white Gaussian noise (AWGN).

Remark 1: PN sequence in frequency domain adopts inverted version of PN sequence that used in the correlator. Furthermore, zero-padding needs to be done before PN sequence is sent to N-point FFT module without changing the circulation of the sequence.

3. Design of Cyclic Correlator

Refer to the FFT-based channel estimation method in [1], the implementation of this frequency estimation entails two 2k-FFT and a corresponding 2k-IFFT modules to process the Real-time data stream. Fig. 3 shows the structure of FFT estimation.

![Fig. 3 Correlation implemented by FFT](image)

The received signal $y$ enters FFT2k_y processor while PN sequence should be mapped to $I+i$ or $-I-i$ before entering the FFT2k_pn. The input data stream is divided into in-phase and quadrature (I/Q) components. After multiplying the output of FFT2k_y with FFT2k_pn by a complex-number multiplier, data is sent to IFFT2k which yields channel impulse response in 2048 clock cycles.

We adopt serial pipeline FFT processors to compute data in real time. Since the delay of the FFT2k is about 2048 clock cycles, it cost at least 4096 clock cycles be-
fore the equalizer obtains channel impulse response regardless of the delay of multipliers.

Block diagram of the simple correlator is illustrated in Fig. 4(a). In this design, cyclic correlation is performed between the local PN sequence and the received signal, thus RAM or registers are needed to store the received 255 symbols to match PN255. Valid correlation values output after the stored 255 received numbers finished additions. Since the value of PN sequence is either zero or one, being modulated into $1+i$ or $-1-i$ before transmitted, multiplexers and additions are adopted instead of complex multiplier in this design by demapping $1+i$ into zero or one. This design bypasses multiplication and saves nearly 3800 clock cycles.

![Fig. 4 Block diagram of correlator.](image)

(a) simple correlator.  (b) complex correlator

However, 254 accumulated additions exits in the aforementioned design results in an unfairly critical path. The Fig. 4(b) shows the structure of complex correlator proposed in this paper outperforms the simple correlator presented in Fig. 4(a).

The input data is divided into I/Q paths before enter the correlator. To obtain cyclic correlation, the received data should be fetched twice from the RAM which already exists in the system. When the RAM is read over for the first time, an eight bits counter within the control unit sends the output a valid signal. The transfigurated design place registers between consecutive adders to guarantee the Real-time operation during the process of the correlation and minimize the critical path as well. As the width of adders gradually accumulates, the register width is extended step by step to reduce the cost of registers. After accumulated additions, two operation units apply on the I/Q data to calculate the final correlation values.

Compared with design implemented by FFT processors, multiplexers are used instead of multipliers as presented in Fig. 4(b). The consumption of registers is reduced by about 10 percents and hundreds of inverters are reduced as well.


Based on SMIC 0.18μm standard CMOS technology, the proposed correlator can work under the frequency of 60MHz, and the circuit area is about 152k gates, making it available for low complexity design. Channel estimation realized in frequency domain with the FFT/IFFT processors is inferior in speed to the cyclic correlator proposed in the paper, since more than 3800 clock cycles are reduced. A performance comparison between FFT estimation and cyclic correlation method is made in Table 1.

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<thead>
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<th>Table 1. Performance comparison</th>
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<td>Tech</td>
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<td>bit width</td>
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<td>Gate#</td>
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However, the implications to the equivalence are limited. FFT processors in the receiver not only perform a critical part in channel estimation but also prepare data for the following stage of equalization while the design we proposed just applies in channel estimation.

References


[3] Bowei Song, Lin Gui and Yunfeng Guan, “On chan-


