Abstract — Digital television/terrestrial multimedia broadcasting (DTMB) was announced as the Chinese digital television terrestrial broadcasting (DTTB) standard in August, 2006[1]. It adopts TDS-OFDM (time-domain synchronous-orthogonal frequency division multiplexing) as the baseline modulation technology [2]. There is not pilot information in order to avoid reduction of channel throughput. It uses pseudo-noise (PN) sequence as guard interval (GI) and the training sequence for both multi- and single-carrier block transmissions which makes the synchronization faster than CP-OFDM (cyclic prefix-orthogonal frequency division multiplexing) systems[3]. It can resist the inter-symbol interference(ISI) and can be used for channel estimation and synchronization. In this paper, a full-mode channel estimation scheme for DTMB demodulator is developed. This method utilizes the PN sequence to obtain channel estimation and equalization both in three kinds of frame head (FH) mode as well as in single and multi-carrier modulation transmission mode. To implement on hardware realization, interference cancellation is predigest, then equalization and filter for channel impulse response are optimized. A low cost VLSI architecture for channel estimation and equalization is proposed which works effectively and achieves low complexity as well. Computational simulation results show that the proposed scheme has little BER loss in performance. VLSI implementation results are presented in the end of this paper.

Index Terms —DTMB, PN sequence, channel estimation, long echo, full-mode, VLSI.

I. INTRODUCTION

In terrestrial broadcasting transmission system of terrestrial digital television, a key problem is that the channel is frequency-selective multi-path channel. An accurate channel estimation and compensation is required to get a better reception performance. Literature [4] and [5] proposed a timing-domain channel estimation method based on the PN sequence’s self-relevant characteristics. This method can improve both in area and power consumption. The PN595 mode in the national standard does not have quasi-cyclic characteristic, so it can’t be used to achieve full-mode channel estimation. Literature [6] addressed an iterative interference cancellation method for multi-carrier PN420 mode to obtain accurate channel estimation. But this method requires several iterations for the whole frame body (FB) and frame head to get more accurate channel impulse response (CIR) estimation, leading to unacceptable hardware implementation. The method in literature [7] is predigest compared to that in literature [6], and it is also for the mode of multi-carrier PN420.

The method presented in this paper can deal with both single-carrier and multi-carrier block transmissions, and for anyone of the three kinds of frame head modes which the DTMB system contains the method is available. In this algorithm we also adopt iterative method. It is different from method in [6] where the overlapping part of PN sequence and frame body are both used for channel estimation that our proposed algorithm just estimate CIR of the PN sequence. The difference from method in [7] is that our algorithm reconstructs frame body using the first iteration result of PN sequence CIR, but method in [7] uses the second iteration result. So our algorithm is simplified compared with all of the previously mentioned methods in algorithm. Furthermore our algorithm has been implemented in hardware.

The remaining paper is organized as follows. Section II briefly describes the DTMB system model. The iterative channel estimation algorithm and complexities of it and methods in [6] and [7] are introduced in Section III. Section IV presents its VLSI architecture and each sub-module hardware implementation strategy. We then give the results of its computer simulation and VLSI implementation in Section V. Finally we conclude this paper in Section VI.

II. SYSTEM MODEL FOR DTMB

The signal frame of DTMB system is composed by frame head and frame body. The standard defines three kinds of frame head mode (PN420, PN595 and PN945) to adapt to different situations. For mode PN420 and PN945, the frame head which is composed by preamble , PN sequence and postamble is posited in front of the frame body in the style of quasi-cyclic. The preamble and postamble are cyclic extension of PN sequence. The transmission power of frame head is 3dB higher than that of frame body. The PN595 mode using ten-order maximum length pseudo-random binary sequence, and PN595 sequence is the first 595 bit of the m-sequence whose
length is 1023. In this mode the transmission power of frame head and frame body is equal. Frame body contains 3780 symbols in which there are 3744 valid data and the remaining 36 data is Transmission Parameter Signaling (TPS). In multi-carrier transmission mode, the 3780 symbols are modulated in OFDM in 3780 sub-carriers and adjacent sub-carrier interval is 2kHz. For the single-carrier transmission mode, the symbols are not modulated in sub-carrier and bandwidth is 7.56MHz.

Figure 1 is the overall block diagram (including transmitter and receiver) of DTMB system. In transmitter, frame body forms after QAM constellation mapping, serial to parallel conversion and inserting TPS. For multi-carrier mode IFFT (Inverse Discrete Fourier Transform) modulation is needed. After parallel to serial conversion and inserting frame head a complete signal frame of DTMB is obtained. Then change it to radio frequency signal and sent it out. In receiver, after AD sampling, synchronization, serial to parallel conversion, channel estimation, PN remove and equalization the received signal becomes uncontaminated data in theory. Then via parallel to serial conversion, TPS remove and QAM constellation demapping the accurate data are obtained. The main difference between multi-carrier and single-carrier is the process of equalization, so the same method can be used in channel estimation.

We set multi-carrier mode as an example, for the $i$th transmitted symbol, the IFFT output is:

$$s_{i,k} = \frac{1}{\sqrt{N}} \sum_{n=0}^{N-1} S_{i,n} \exp(-\frac{2\pi kn}{N}), 0 \leq k < N$$

(1)

The transmission channel is modeled as a quasi-static $L$th order FIR filter, then the CIR of the $i$th symbol period can be expressed as $\{h_{i,k}\}_{k=0}^{L-1}$, We assume that $L$ is shorter than $M$ ($M$ represents PN length), so the lengths of tails frame head causes in frame body of the same signal frame and frame body causes in frame head of the next signal frame are shorter than PN length, as shown in figure 2(b).

### III. Iterative Channel Estimation Method

As shown in figure 2(c), the FB and FH are both contaminate by tails when transmission signals have been affected by multiple and long echoes. Then we need using the method of decision feedback interference cancellation and then reconstruct FB and FH to do channel estimation. We can change the local PN sequence so as to support three FB modes.

From figure 2 we can describe the received data as:

$$r_{i,k} = x_{i,k} + y_{i,k} + w_{i,k},$$

(2)

$N$ represents the length of frame body and $w_{i,k}$ represents the additive white Gaussian noise (AWGN) with variance $\sigma_w^2$. The detailed processes area as follows:

(1) For the beginning two signal frame, we only calculate CIR of FH and tails FH of frame 2 causes in FB of the same frame and don’t do equalization for FB data of frame 1. Converting the received FH data and PN sequence from time domain to frequency domain and do division, then after converting the diversion result back to timing domain we can get the estimation of CIR.

$$\{h_{i,k}\}_{k=0}^{L-1} = \text{IFFT}_{N} \{f_{i,k} \{r_{i,k}\}_{k=0}^{M-1} / f_{i,k} \{PN_{i,k}\}_{k=0}^{M-1}\} (i = 1, 2)$$

(3)

In equation (3), $\{r_{i,k}\}_{k=0}^{M-1}$ is the received FH data, $\{PN_{i,k}\}_{k=0}^{M-1}$ is PN sequence of the same frame. Before doing FFT, the data have to be extend to length of $N_i$ by filling 0 at the end.

After MMSE (Minimum Mean Square Error), we get the estimation value of CIR. Then calculate the effect of FH to FB by multiplying $\{h_{2,k}\}_{k=0}^{L-1}$ and PN sequence in frequency domain and the last L data of the multiplying result is tail (PN).
\begin{equation}
\{y_{i,k}\}_{k=0}^{N-1} = \text{ifft}_N\{h_{i,k}\}_{k=0}^{L-1} \ast \text{ifft}_N\{PN_{i,k}\}_{k=0}^{M-1}\} (i=2)
\end{equation}
\begin{equation}
\{\text{tail}(PN)_{i,k}\}_{k=0}^{L-1} = \{y_{i,k}\}_{k=N-L}^{N-1} \} (i=2)
\end{equation}

(2) From FB of the second frame, the processes are as follows:

1) Estimate CIRs of FB of frame i-1 and FH of frame i

2) Calculate tail (data) of FB of frame i:

3) Reconstruct FB of frame i-1 and do equalization:

4) Reconstruct FH of frame i:

5) Update FH CIR of frame i:

6) Update \{\text{tail}(PN)_{i,k}\}_{k=0}^{L-1} and reconstruct FH of frame i again:

7) Do step 5) again and the final \{h_{i,k}\}_{k=0}^{L-1} is get, then store it and go to the next frame process.

Table I shows the computational complexity comparison between the conventional method in [7] and the proposed scheme. As shown in this table, the proposed scheme has a much lower complexity than the conventional one.

\begin{table}[h]
\centering
\caption{Computation Complexity Comparison between the Conventional and Proposed Method}
\begin{tabular}{|c|c|c|}
\hline
\hline
N-point FFT/IFFT & 3 & 3 \\
N_:point FFT/IFFT & 14 & 12 \\
complex multiplication & 4N_1 & 3N_1 \\
complex division & N +2N_1 & N +2N_1 \\
\hline
\end{tabular}
\end{table}

IV. HARDWARE ARCHITECTURE

Figure 3 shows the hardware architecture where the dotted boxes represent that the modules are being reused. The entire structure includes top-level control module, FIFO module, N-point FFT/IFFT, N_:point FFT/IFFT, interpolation module, MMSE filtering module (ignored in figure 3) and reconstruction module.

According to the algorithm, firstly, run the interpolation module, then do N-point FFT to data \{h_{i-1,k}\}_{k=0}^{L-1} at the same time complete FB reconstruction by calculating the tail FB caused. Secondly run equalization module and do N_:point FFT to data \{h_{i-1,k}\}_{k=0}^{L-1}. After that, reconstruct FH of frame i, then estimate a new value of \{h_{i,k}\}_{k=0}^{L-1} and go to the second iteration. In the second iteration, calculate the tail of FH and
send it to the next frame process, then update \( \{h_{i,k}\}_{k=0}^{L-1} \) and also send it to the next frame process. The sub-modules will be presented respectively.

Top-level control module: This module is used to control the entire process of all modes with Finite State Machine (FSM). We adopt pipeline structure and process frame by frame.

FIFO module: There are two rams, one is used to receive and store data, and at the same time the other one is used to send data to process modules. So the reading clock is set to be quicker than the writing clock so as to meet the timing requirement.

N-point FFT/IFFT module: This module is mainly responsible for equalization. When doing complex division, we treat amplitude and phase balance respectively. The amplitude balance is done by look-up table and the phase balance by CORDIC module.

N\(_1\)-point FFT/IFFT module: It is used when calculating CIR of FH, tails and convolution of PN and CIR.

Interpolation module: It completes liner interpolation of CIRs.

MMSE filtering module: It is included in the N\(_1\)-point FFT/IFFT module, and is used to filter noise.

Reconstruct module: Its role is to remove the effects between FH and FB, thus to reduce contamination.

In order to reduce the complexity of hardware, some techniques are used which include area optimization and power optimization. The FFT/IFFT module occupies more areas and timing than anyone of the others, so we mainly treat with these modules. We can see in figure 3 that there are only three FFT/IFFT modules, because FFT and IFFT module can use the same one and we just need to add some control units. In order to decrease its power, clock gating is adopted which means that the clock of module will be closed at the free time.

Figure 4 shows the SNR performance of DTMB system over CDT8 channel at the same simulation parameters. For a SER of \( 4\times10^{-3} \), the SNR degradation of the performance based on method in [7] with our method is about 3 dB.

The design has been verified in FPGA. We use device EP2S130F1020C5 and it works over AWGN channel which means that the hardware architecture is available. To analyze its cost compiling has been done by Design Compiler (DC) of Synopsys with SMIC 0.13 standard CMOS cell library. Table IV shows the compiling results. In order to meet timing requirement, the conventional scheme has to use two N-point FFT/IFFT modules. The combinational logic area and memory area of one N-point FFT/IFFT are respectively about

![Fig. 3. Hardware structure](image-url)
55625.5μm² and 2267908.9μm². So the proposed hardware architecture saves at least 26.2% in area cost.

VI. CONCLUSION

In this paper, a full-mode resisting long echo channel estimation method for DTMB demodulator is developed and a low cost VLSI architecture is proposed. The tails of the FH and FB and CIRs are estimated and updated so that the residual ISI are removed iteratively. Analysis shows that the proposed method has a lower complexity compared with that of the reference methods. Although the SNR degradation of the proposed algorithm is slightly worse than the complex one, the cost in hardware of it is much smaller and accordingly the power will be reduced.

VII. REFERENCE


BIOGRAPHIES

Yunlong Ge received the BS degree from Tianjin University, P.R China, in 2009. He is currently working toward master degree in microelectronics at the ASIC & System State Key Lab of Fudan University. His main research interests include digital signal processing, OFDM systems and wireless transmission communications, in particular, VLSI architectures of channel estimation and equalization for HDTV.

Huxiong Xu received the BS degree from Fudan University, P.R China, in 2008. He is currently working toward master degree in microelectronics at the ASIC & System State Key Lab of Fudan University. His main research interests include digital signal processing, SDR and wireless transmission communications, in particular, channel estimation and equalization for HDTV.

Yun Chen received the B.S. and M.S. degrees in microelectronics from UESTC, China, in 2001 and 2004, respectively, and the PhD. degree from Fudan University in 2007. Dr. Chen is currently a lecturer with the State Key Laboratory of ASIC & System, Microelectronics Department, Fudan University, Shanghai, China. Her main research interests include digital signal processing, OFDM systems, and wireless transmission communications, in particular, channel estimation and equalization for HDTV.

Chen Chen received the BS degree from Fudan University, P.R China, in 2007. He is currently working toward master degree in microelectronics at the ASIC & System State Key Lab of Fudan University. His main research interests include digital signal processing, OFDM systems, and wireless transmission communications, in particular, channel estimation and equalization for HDTV.

Xiaoyang Zeng received the B.S. degree from Xiangtan University, China in 1992, and the Ph.D. degree from Changchun Institute of Optics and Fine Mechanics, Chinese Academy of Sciences in 2001. From 2001 to 2003, he worked as a post-doctor researcher at the State-Key Lab of ASIC & System, Fudan University, P.R. China. Then he joined the faculty of Department of Micro-electronics at Fudan University as an associate professor. His research interests include information security chip design, VLSI signal processing, and communication systems. Prof. Zeng is the Chair of Design-Contest of ASP-DAC 2004 and 2005, also the TPC member of several international conferences such as ASCON 2005 and A-SSCC 2006, etc.