AIP Applied Physics Letters

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Citation: Appl. Phys. Lett. **103**, 052104 (2013); doi: 10.1063/1.4816743
View online: http://dx.doi.org/10.1063/1.4816743
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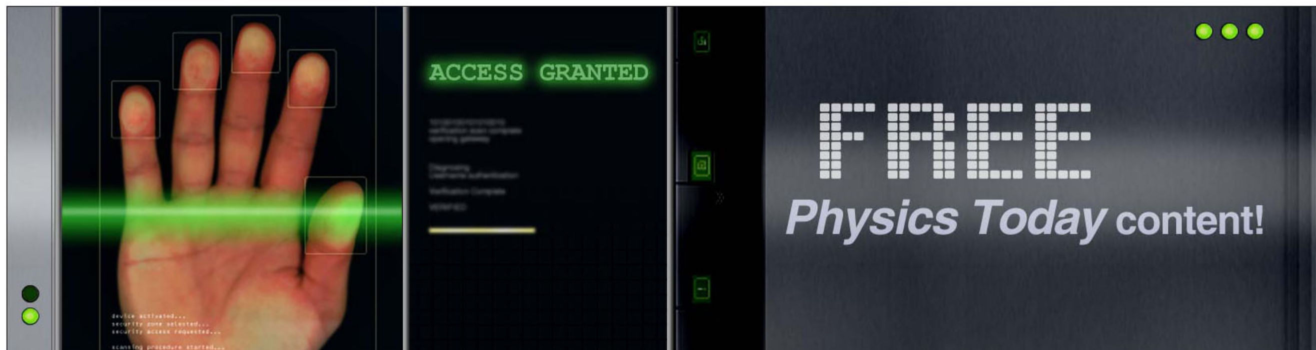

Strain mapping of Si devices with stress memorization processing

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(Received 7 April 2013; accepted 6 July 2013; published online 30 July 2013)

Dual lens dark field electron holography and Moiré fringe mapping from dark field scanning transmission electron microscopy are used to map strain distributions at high spatial resolution in Si devices processed with stress memorization techniques (SMT). It provides experimental evidence that strain in the Si channel is generated by dislocations resulting from SMT. The highest value of strain, up to 1.1% (1.9 GPa in stress) occurs at the Si surface along the channel direction: ⟨110⟩. An increase of ∼0.2% strain in the channel is observed after removing the poly-Si gate through the replacement high-k metal gate process. © *2013 AIP Publishing LLC*.
[http://dx.doi.org/10.1063/1.4816743]

In a complementary metal–oxide–semiconductor (CMOS) Si device, a gate on top of Si is used to control the on and off (open and close) conditions of the Si channel between the source and the drain. With semiconductor devices sizes decreasing into the nanometer scale, strain engineering in the Si channel becomes a critical part of improving performance for large scale integrated circuits.[1] One example of strain engineering is the stress memorization technique (SMT), which has been implemented in several generations of semiconductor technology to enhance NFET (Negative Channel Field Effect Transistor) device performance up to 23%.[2,3] The SMT approach involves amorphizing the Si source and drain regions as well as the poly Si gate region by implanting non-dopant elements and then annealing to recrystallize the amorphous Si into crystalline Si under a tensile strained, Si_3N_4 film, above the device. The stress is retained after the Si_3N_4 film is removed. However, the mechanism of how stress is memorized in the device is still under debate. Investigation of 2D strain distribution in Si at high spatial resolution will help to resolve the mechanisms.

Two methods have been recently developed with the transmission electron microscope to characterize 2D strain distributions in Si devices: dark field electron holography[4] and Moiré fringe analysis of high resolution dark field scanning transmission electron microscopy (HR-STEM) images. Dark field electron holography using dual lens operation provides 2D strain maps at high spatial resolution of up to 1 nm.[5,6] HR-STEM with Moiré fringe analysis provides visualization of the lattice displacement modulation. In this paper, we use dual lens dark field electron holography and HR-STEM with Moiré fringe analysis to investigate the source of strain responsible for the device enhancement. We also investigate how the different process steps influence the strain distribution.

From dark field electron holography, the normal component of strain along a specific direction in a crystalline material is measured according to the following equation:

$$\varepsilon_{ij} = \frac{d_{obj}^{(i)} - d_{ref}^{(i)}}{d_{ref}^{(i)}} \approx \frac{1}{2\pi g_{ref}^{(i)}} \frac{\partial \varphi^{(i)}}{\partial r_i}, \tag{1}$$

where i = j = x for the in-plane strain component along the channel direction, i = j = z for the in-plane-plane strain component perpendicular to channel direction, $g = 1/d$, d_{obj} is the lattice spacing in the strained region, d_{ref} is the unstrained lattice spacing, and $\varphi^{(i)}$ is the phase information extracted from the specific diffracted hologram.[4,7–9]

The Moiré fringe map of a STEM image is generated by artificially introducing a uniform lattice image overlapped on the measured one. The modulation of the Moiré fringe, D, is due to the small difference between the measured lattice, d_1, and a computer generated lattice, d_2, and it obeys the following equation:[10]

$$D = \frac{d_1 d_2}{|d_1 - d_2|}. \tag{2}$$

Using Eq. (2), one generates one equation in the strained (obj) region and another in the unstrained (ref) region. By assuming the ratio D_{ref}/d_{ref} is at least 10 and solving these two equations, one derives an expression for strain

$$\varepsilon_{ij} = \frac{d_{obj} - d_{ref}}{d_{ref}} \approx \frac{D_{obj} - D_{ref}}{D_{obj}} \frac{d_{ref}}{D_{ref}}. \tag{3}$$

This equation shows that the difference of a small lattice constant change (less than 2%) can be amplified by a factor of D_{ref}/d_{ref} through Moiré fringe mapping, at the expense of spatial resolution.

TEM samples are prepared by using an *in situ* focused ion beam method (FIB) to an approximate thickness of 150 nm. Dual lens dark field electron holograms were obtained on an FEI F20 TEM, with two objective lens settings of 70% and 80% for low and high magnification strain imaging, respectively.[5,6] The dark field hologram of the ⟨220⟩ diffracted beam (along the Si channel direction) was

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acquired using a 2k × 2k CCD camera. Atomic resolution dark field STEM was carried out on a FEI Titan fitted with a probe C_s corrector. The microscopes were operated at 200 keV. GEOMETRICAL PHASE ANALYSIS (GPA) software is used to extract strain information (lattice deformation) from the dark field electron holography and Moiré fringe map from HR-STEM images.[8,9]

The relevant processing steps applied to the Si devices described in this paper are: (1) poly-Si gate patterning; (2) spacer deposition on the side of poly-Si gate; (3) poly-Si gate removal; (4) high k metal gate deposition. SMT can be performed either after gate patterning or after the spacer process. In the study, the strain measurements are made at several key processing steps: before and after the poly-Si gate removal, and after metal gate deposition. Samples I and II underwent Si amorphization after the spacer process, followed by re-crystallization at 600 °C, but without the tensile strained Si_3N_4 film on top of the device to serve as control samples. Sample I was measured before poly-Si gate removal and sample II was characterized after metal gate deposition. SMT for samples III, IV, and V occurred after spacer deposition with the tensile Si_3N_4 film present during recrystallization. Samples III and V were measured before and after poly-Si gate removal, respectively, and the strain of sample IV after metal gate deposition. SMT for sample VI was processed after gate patterning, but before spacer deposition and strain was measured after metal gate deposition.

With SMT samples (sample III to VI), we observed two kinds of crystalline defects near the devices: those without stacking faults (minority) and those that contained stacking faults (majority). Burgers' circuit analyses of the HR-STEM images of defects without stacking faults revealed a perfect 60° dislocation (un-dissociated) with Burgers vector $\boldsymbol{b} = \langle 101 \rangle /2$ and lying parallel to the beam direction, $\boldsymbol{t} = \langle 1\bar{1}0 \rangle$. Those with stacking faults corresponding to a dissociated 60° dislocation: where the partial at the bottom of the stacking fault possesses a Burgers vector of $\langle 112 \rangle /6$ (90° partial) and that at the top of the stacking fault as $\langle 2\bar{1}1 \rangle /6$ (30° partial). The Burgers vector of bottom partial is contained within the TEM sample plane, while the top partial is oriented 30° from the direction perpendicular to the TEM sample. (It has been previously reported that under certain conditions, however rare, the un-dissociated dislocation moves along $\langle 110 \rangle$ into the channel region.[11])

Maps of strain along [110] of sample VI are contained in Figure 1: Fig. 1(a) is a low magnification map and Fig. 1(b) is a high magnification map. In Fig. 1(a), the device marked as 1 has one dislocation on the right side only, while devices 2 and 3 possess dislocations at both sides. The strain in device 1 appears to be approximately half of that in devices 2 and 3. In the high magnification map [Fig. 1(b)], the distance between two dislocations is ∼40 nm and their depth from the Si surface is ∼25 nm. The Si region immediately below the dislocation core is compressive, while that above is in tension. Close to the dislocation core (1–2 nm), both compressive and tensile strain reach values as high as 20%–40%. The high lattice displacements decay very quickly away from the dislocation core, with longer range, tensile deformation that emanates diagonally toward the channel [inserted figure in Fig. 1(b)]. In the case of devices with

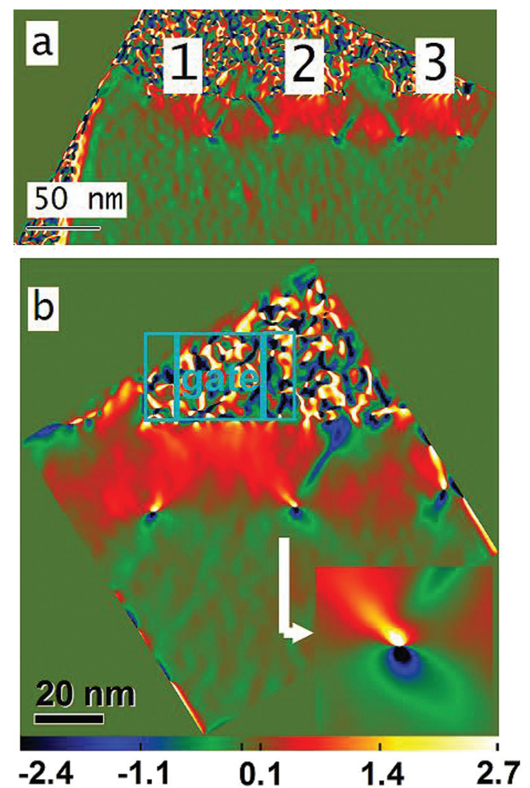

FIG. 1. (a) Strain map generated using electron holography at low magnification. Device 1 has a dislocation on one side (right side) only; while devices 2 and 3 possess dislocations on both sides. (b) Strain map at high magnification. The color bar has units of percent strain. The boxes (light blue) on the side of the gate box (light blue) correspond to the spacers. The inset is a higher magnification image (2.5×) of the right side dislocation core strain field.

dislocations on both sides, the superposition of strain fields in the channel region generate values as high as ∼1% directly under the gate. To the right side of the gate, a compressive strain line extends along $[11\bar{2}]$ and is probably a $[1\bar{1}0]$ projection of a (111) stacking fault. The tensile strain near and above this line is weaker than the one in the region under the gate. On the left of side of the gate, there is no similar defect, and the corresponding strain distribution is not symmetric with respect to the device center. To further illustrate the effect, a STEM image is used to obtain a Moiré fringe map, as shown in Fig. 2. Fig. 2(a) is the HR-STEM image. Using the GPA method, we generated Moiré fringe maps along $[11\bar{1}]$ as shown in Fig. 2(b). An extra $(11\bar{1})$ plane is observed below the fault on the left side while on the right side there appears a discontinuity in the Moire fringes across the (111) plane. The map of [111] is similar to the $[11\bar{1}]$ map, except the left and right defect profiles are reversed (not shown). The extra line is indicative of an extra atomic plane, which is not readily seen in the lattice image [Fig. 2(a)]. We generated two additional Moiré fringe maps with coarse and finer fringe spacing along [110] as Figs. 2(c) and 2(d), respectively. In both figures, there is an extra line below the dislocation. The expanded lattice in the channel region is shown by the increased separation of the Moiré fringes. The effect of lattice expansion is more visible in the coarse Moiré fringe map than in the finer fringe map, which is consistent with Eq. (3), where lattice expansion is magnified by a factor of D_{ref}/d_{ref}.

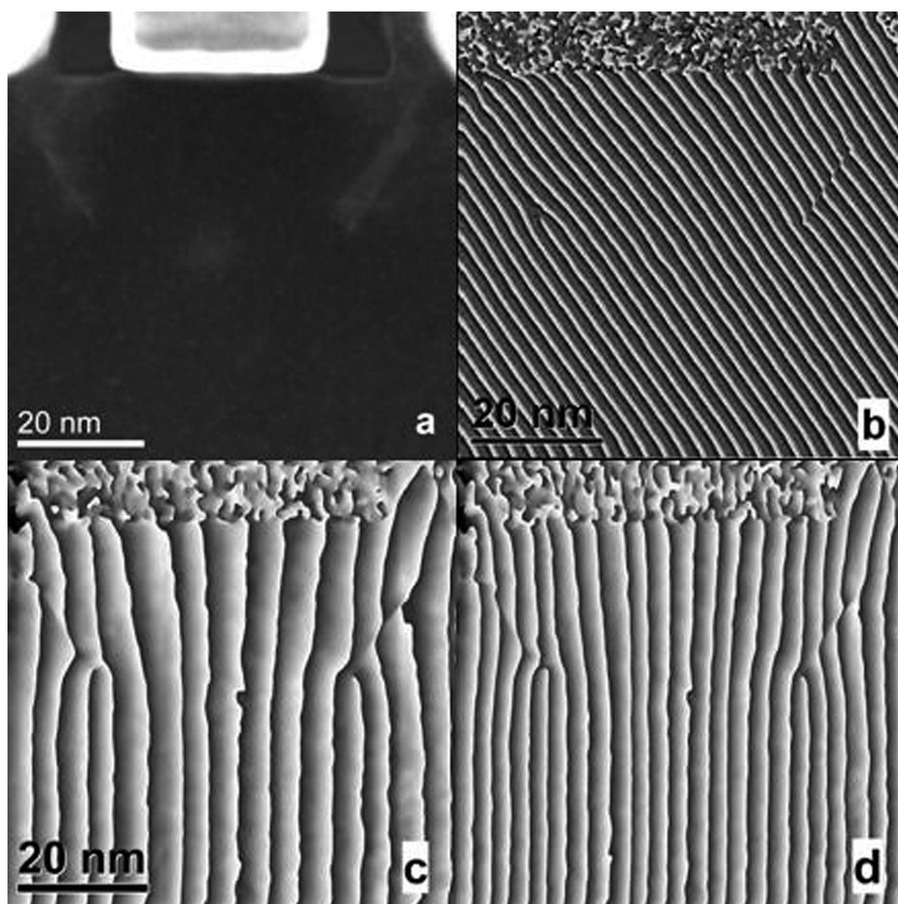

FIG. 2. (a) Atomic resolution dark field STEM image of a similar device as that in Fig. 1 with the identical processing condition. (b) [111] Moiré fringe map, where an extra line is observed normal to [111] below the left side dislocation core. (c) [220] Moiré fringe map generated from the STEM image with larger spacing. (d) [220] Moiré fringe map with finer spacing.

Figure 3 depicts the depth dependence of the strain along ⟨110⟩ extracted from the dark field electron holography maps as a function of distance below the Si surface directly under the gate. For the control samples without the Si_3N_4 layer above the device during re-crystallization, TEM images show no crystalline defects in source and drain regions. The in-plane strain in sample I is approximately zero at the Si surface, corresponding to the top of the channel region, and for sample II is ∼0.2%. When SMT is applied after spacer formation, the separation between the two dislocations under the gate for samples III, IV, and V is ∼50 nm with depths of about 30 nm. The strain at the top of the channel for samples III, IV, and V are approximately 0.53%, 0.68%, and 0.71%, respectively. When SMT was processed prior to the creation of the spacer (sample VI), the dislocations are generated closer to the gate with a separation of 40 nm and depth of 25 nm. The corresponding in-plane strain at the top of the Si channel is observed at 1.1%. This finding is consistent with Moiré fringe map measurements performed on sample VI. The variation in strain as a function of depth below the gate is determined by measuring the variation of the local Moiré fringe spacing using Eq. (3), which is shown in closed circles on Fig. 3. The measurements are summarized in Table I, along with separation between two dislocations under the gate and their depth from the top Si surface. The strain measured at different processing steps provides insight into the strain generation within NFET devices. For instance, the closer the dislocation is to the channel, the higher is the value of in-plane strain in the channel region, as shown in the comparison between samples IV and VI. Gate removal generates approximately 0.2% more strain, as shown by comparing samples 3 and 5 that underwent SMT (or sample I and II without SMT). The removal of the gate allows for additional elastic relaxation of the system inducing the additional deformation in the channel region.[12] The deposition of metal gates does not appear to significantly alter the strain as demonstrated by samples IV and V.

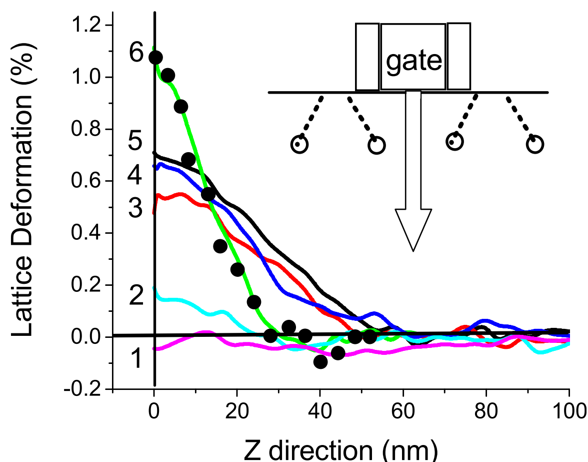

FIG. 3. In-plane strain distributions along [110] as a function of depth from the top Si surface at different processing steps. The detailed process conditions are listed in Table I. Closed circles correspond to the strain values calculated from the Moiré fringe map of Fig. 2(d) using Eq. (3). Dashed lines in the inset drawing represent stacking faults and circles at the end of dashed line are dislocations.

Earlier work on SMT suggested that the strain induced in the channel arises from re-crystallization of the poly-Si

TABLE I. Relevant processing steps associated with the samples under the investigation, dislocation position, and measured in-plane strain along ⟨110⟩ at the top Si surface.

Sample	SMT process	Strain measured	Dislocation Distance	Dislocation Depth	Strain (%)
I	No SMT	Before gate removal	No dislocation		~0
II	No SMT	After metal gate	No dislocation		0.20
III	After spacer	Before gate removal	50 nm	30 nm	0.53
IV	After spacer	After metal gate	50 nm	30 nm	0.68
V	After spacer	After gate removal	50 nm	30 nm	0.71
VI	Before spacer	After metal gate	40 nm	25 nm	1.1

gate.[13,14] However, recent publications have proposed the re-crystallization of the source/drain regions as the mechanism responsible for stress memorization.[2,15,16] Our experimental data provide evidence that the strain in the channel is created by the presence of dislocations in source/drain region generated during the SMT process. Device 1 in Fig. 1(a) clearly shows that a dislocation is the source of channel tensile strain under the gate, because little strain is observed in the channel region on the side without a dislocation (left side). The dislocation on the right side of the channel transmits approximately half of the strain onto the channel of the device: the strain in device 1 is approximately 0.5% compared with approximately 1% in both devices 2 and 3, where there is no missing dislocation on either side of the device. In the detailed map near the dislocation [inserted figure in Fig. 2(b)], a line of large strain (~2%) emanates from the bottom dislocation towards Si channel, providing additional evidence that strain in the channel is induced by the dislocation. The Moiré fringe map of Fig. 2(c) provides visual evidence that the dislocation is the source of tensile strain at the Si surface, where missing atomic planes above the two dislocations generate an in-plane tensile strain field between them. The data also show that the presence of the poly-Si gate actually restricts the elastic relaxation of the channel region, if it is not removed. This finding is contrary to the SMT mechanism proposed earlier.[13,14] The increase in strain at the Si surface after gate removal has been predicted in finite element modeling using an edge dislocation as a source.[15] Combining the previous modeling data[15] with our experimental observations, we conclude that the dislocations are the source of the tensile strain in the channel (either from the 90° partial dislocation or the 60° type dislocation generated through the SMT process). Assuming a uniaxial strain state in the channel and an effective Young's modulus along Si ⟨110⟩ of 169 GPa,[17] we calculate a maximum in-plane stress of 1.9 GPa at the Si surface for sample VI.

The observations of stacking faults generated during the SMT process are consistent with previous measurements on the re-crystallization of amorphized Si during solid phase epitaxy (SPE). It has been shown that in-plane tensile strain promotes the vertical growth front in Si {001} and compressive strain inhibits {001} growth.[18] Rudawski *et al*. reported that the state of in-plane strain modulated the appearance of stacking faults (termed mask-edge defects) by impacting the relative rates of the vertical growth front {001} to the lateral growth front {110}.[19] The proposed mechanism involved altering the angle at the bottom corner of the amorphized region between the {001} and {110} faces in the presence of Si_3N_4 film. In-plane tensile strain retarded the lateral growth front and increased the vertical growth front, creating a more obtuse bottom corner that suppressed defect formation. In contrast, in-plane compressive strain would lead to cusps at the intersection of the orthogonal growth fronts, accentuating the nucleation of stacking fault defects. During SMT, the tensile strained, Si_3N_4 liner materials actually induce a compensating, in-plane compressive strain in the underlying, amorphous Si, producing defects in the form of dissociated or un-dissociated 60° dislocations, as observed in samples III to VI. However, the re-crystallization of amorphous Si without the presence of overlying strained liner features (samples I and II) results in few such defects.

The results from dark field holography show a consistent picture with respect to the SMT processing. With device channels decreasing to as narrow as 30 nm (sample VI), high spatial resolution dark field holography with dual lens configuration is useful for the characterization of these kinds of devices. This method also generates a clear picture of the lattice displacement near the dislocation core. Moiré fringe maps generated from HR-STEM imaging provide a visual representation of the lattice displacement near and away from the dislocation core. We show that in Fig. 3 the strain obtained by dual lens dark field electron holography and by the Moiré fringe method is consistent. It is noted here that the strain maps derived by GPA software from the HR-STEM image has a similar strain value but with a lower signal-to-noise ratio than the one from dual lens dark field electron holography due to intrinsic scanning noise and therefore are not reported in the paper.

In summary, experimental strain mapping performed on Si devices that undergo SMT processing reveals that strain in the Si channel region is generated by the creation of dislocations during the re-crystallization of the adjacent source and drain regions. It is reported that poly-Si gate removal provides additional 0.2% in-plane tensile strain, while the incorporation of a replacement metal gate does not impose much additional strain.

We acknowledge the support from IBM managers: A. Katnani, M. Lagus, and A. C. Lamberti on the dual lens dark field electron holography development and valuable discussion on strain measurement with F. Baumann and P. Flaitz of IBM and D. Cooper of LETi in France. This work was performed by the Research Alliance Teams at various IBM Research and Development facilities.

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