A Smart Control Approach for Digitally Controlled Multiple-Output DC-DC Converter

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Abstract -- This paper presents a smart control approach for digitally controlled forward type multiple-output dc-dc converter. In this case, the central problem of design is how to decide the integral coefficient. Since the decision of integral coefficient depends on the static characteristics, the selected integral coefficient is not suitable to perform the superior dynamic characteristics. Then, it is important to set the suitable integral coefficient for not only static characteristics but also dynamic characteristics. As a result, overshoot and the convergence time of the output voltage are improved 30% and 30%. The overshoot of reactor current is improved 11%. Moreover, to achieve the improvement of the dynamic characteristic, the number of bits of the calculation part of the digital control circuit set enlarged. As a result, the overshoot and the convergence time of the output voltage are improved 78% and 30%. The overshoot of reactor current is improved 17%.

Index Terms-- Digital control, Forward type multiple-output dc-dc converter

I. INTRODUCTION

The saving energy in the power supply has been brought to public attention. A popular idea exists nowadays that the energy management is useful to reduce the total electric power consumption in switching power supply system. However, this technology is not widely used because the conventional analog controller is not able to connect the control network of the energy management power supply system easily. Therefore, since the digital control circuit is fundamentally consist of the digital signal one, the concern with the digital control for switching power supply has been growing to construct the digital interconnection energy management power supply system. Recently, a considerable number of studies have been made on a digital control [1], [2]. At a first step, it may be helpful to begin with a study of the approach for design of the digital control. The central problem of design for digital control circuit is how to decide the integral coefficient. Since the decision of integral coefficient depends on the static characteristics, the integral coefficient is not suitable to perform the superior dynamic characteristics. In this paper, the main circuit consists of the forward type multiple-output dc-dc converter [3], [4]. This circuit is a good example to examine a design of the digital control circuit for the dc-dc converter because that is widely used in the electrical and electronic systems.

This paper presents a smart control approach for digitally controlled multiple-output DC-DC converter. In this case, it is important to set the suitable integral coefficient for not only static characteristics but also dynamic characteristics. At first, we calculate the regulation range of input voltage and output current. It set the upper and lower ranges of input voltage and output current of regulation range. Next, we search the integral coefficient to satisfy the specific regulation range and then confirm the dynamic characteristic by the simulation. As a result, the overshoot and the convergence time of the output voltage are improved 30% and 30%. The overshoot of reactor current is improved 11%. Moreover, to achieve the improvement of the dynamic characteristic, the number of bits of the calculation part of the digital control circuit set enlarged. Therefore, the overshoot and the convergence time of the output voltage are improved 78% and 30% lastly. The overshoot of reactor current is improved 17%.

II. OPERATION PRINCIPLE

Figure 1 shows the forward type multi-output dc-dc converter. In the circuit, the reset winding $N_p 2$ is added to avoid the saturated flux. The turn ratio $N_p 1/ N_p 2$ is equal to unity. $E_i$ is the input voltage, $e_{o1}$ and $e_{o2}$ are the output voltages, respectively. $i_{o1}$ and $i_{o2}$ are the output currents. $i_{L1}$ and $i_{L2}$ are the reactor currents. $D_{11}$, $D_{12}$, $D_{21}$ and $D_{22}$ are the diodes. $C_1$ and $C_2$ are the output smoothing capacitors. $N_p 1$, $N_p 2$, $N_s 1$ and $N_s 2$ are the numbers of turn for the transformer T. $R_1$ and $R_2$ are the loads. $L$ is energy storage reactor with the cross regulation function. $N_{L1}$ and $N_{L2}$ are the number of turn for energy storage reactor L. The output voltage $e_{o1}$ is detected and is controlled. Another output voltage $e_{o2}$ is controlled by the cross regulation of the transformer T and reactor L. The following equation is related the turn ratio and output voltage.
Figure 2 shows the digital control circuit of forward type multi-output dc-dc converter. The output voltage $e_{o1}$ is the control target. $e_{o1}$ is sent to the A-D converter through the anti-aliasing filter and is converted into digital amount $N_n$. The relation between the input and output values of the A-D converter is given by Eq. (2) when it approximately shows the linear expression by considering the width of the quantization to be small.

$$\frac{N_{L2}}{N_{L1}} = \frac{E_{o2}^*}{E_{o1}^*}$$  \hspace{1cm} (1)

The numerical value equivalent to the width is turned on with $N_{T_{on}}$ and it's set in a PWM signal generation circuit.

$$N_{T_{on}} = \frac{N_{n+1}}{Q_{AD} - 1}$$  \hspace{1cm} (7)

The duty ratio $S_{T_{on}}/T_s$ is represented as follows;

$$S_{T_{on}}/T_s = \frac{N_{T_{on,n+1}}}{N_{T_s}}$$  \hspace{1cm} (8)

Next, the regulation characteristic of the output voltage is discussed using an ideal transformer. The on-time $T_{oni}$ in the steady-state is shown as follows;

$$T_{oni} = T_s\left(1 + \frac{r_{L1}}{R_1}\right)\frac{E_{o1}^*}{N_{sl}/N_{pl} E_i - r_p(E_{o1}/R_1 + I_{o2})}$$  \hspace{1cm} (9)

Therefore, to control the forward type multiple-output dc-dc converter, the on-time in which it tempers with $T_{oni}$, the rectification time $T_{c1}$ and $T_{c2}$ are needed. The range of the on/off ratio of switch $T_f$ where the overflow and the underflow with the integration control circuit are not caused is shown based on this expression (9) and expression (10) as follows.

$$T_{c1} = T_{c2} = \frac{N_{pl} L_1 I_{o1}}{N_{sl} E_i}$$  \hspace{1cm} (10)
The regulation range against input voltage is represented as follows;

\[
\frac{N_B - K_i \times (2^{Q_i-1} - 1)}{N_{TS}} < \frac{(I + \pi / R_i) E_{ol}^*}{N_{pl} E_{ol}} + \frac{N_{pl} E_{ol}}{N_{TS}} < \frac{N_B + K_i \times 2^{Q_i-1}}{N_{TS}}
\]

(11)

where

\[
a_1 = \frac{N_{pl}}{N_{ts}} Z_1
\]

(13)

\[
a_2 = \frac{N_{pl}}{N_{ts}} Z_2
\]

(14)

\[
b_{el} = \frac{L_1 I_{ol}}{I_1} + (1 + \pi L_1 / R_1) E_{ol}^* + r_p (I_{ol} + I_{o2}) Z_1
\]

(15)

\[
b_{e2} = \frac{L_1 I_{ol}}{I_1} + (1 + \pi L_1 / R_1) E_{ol}^* + r_p (I_{ol} + I_{o2}) Z_2
\]

(16)

\[
c = -\frac{L_1 I_{ol}}{I_1} r_p (I_{ol} + I_{o2})
\]

(17)

\[
Z_1 = \frac{N_B - K_i \times (2^{Q_i-1} - 1)}{N_{TS}}
\]

(18)

\[
Z_2 = \frac{N_B + K_i \times 2^{Q_i-1}}{N_{TS}}
\]

(19)

The regulation range against output current is represented as follows;

\[
\frac{b_{i1} + \sqrt{b_{i1}^2 - 4 a_i s_{i1}}}{2 a_i} < I_{o1} < \frac{b_{i2} + \sqrt{b_{i2}^2 - 4 a_i s_{i2}}}{2 a_i}
\]

(20)

where

\[
a = -\frac{N_{s1}}{N_{pl} E_i} r_p
\]

(21)

\[
b_{i1} = -\frac{N_{s1}}{N_{pl} E_i} \left( \frac{N_{s1}}{N_{pl}} E_i - r_p I_{ol} \right) - Z_1 r_p
\]

(22)

\[
b_{i2} = -\frac{N_{s1}}{N_{pl} E_i} \left( \frac{N_{s1}}{N_{pl}} E_i - r_p I_{ol} \right) - Z_2 r_p
\]

(23)

\[
c_{i1} = Z_1 \left( \frac{N_{s1}}{N_{pl}} E_i - r_p I_{ol} \right) - (1 + \pi L_1 / R_1) E_{ol}^*
\]

(24)

III. THE SMART APPROACH FOR DESIGN AND RESULT OF SIMULATION AND EXPERIMENT

The circuit parameters are \( C_1 = C_2 = 960 \mu F, N_{p1} : N_{p2} : N_{s1} : N_{s2} = 2 : 2 : 1 : 2, E_{ol}^* = 5V, E_{o2}^* = 10V \) and \( R_2 = 20\Omega \). The inductance \( L \) is 98\( \mu H \). Furthermore, \( Q_{AD} = 12\)bits, \( G_{AD} = 819V^{-1} \) and \( N_{TS} = 4000 \). The sampling frequency \( f_{smp} \) is equal to the switching frequency \( f_s \) and is 100kHz.

The digital PWM module is made from an Xilinx Vertex- II pro FPGA. Figure 3 shows the construction of digital PWM. It makes clock that moves four phases of 100MHz in the DCM (Digital Clock Manager). As a result, the counter with the performance of 400MHz becomes suitable [5], [6].

A. Static Characteristics

The regulation range against the output voltage and current is shown in Eqs. (12) and (20). As shown in these equations, the regulation range depends on \( K_I \) and \( Q_I \). In this case, the rating input voltage \( E_i^* \) is 45V and the specification of the regulation range of the output voltage is set from 33V to 57V. However, when the rating input voltage is 45V, the upper input voltage range is more over the specific regulation range as shown in Fig. 4(a). So, we search the new suitable rating input voltage 42V as shown in Fig. 4(b). Figure 5 shows the relationship between the number \( Q_i \) of bits of the calculation part and the digital integral coefficient \( K_{Imin} \). In this figure, the dotted line denotes the condition of \( E_i^* = 45V \) and the solid line shows the relationship in \( E_i^* = 42V \). It is seen that \( K_{Imin} \) in case of \( E_i^* = 42V \) is smaller than that in case of \( E_i^* = 45V \), and the integral coefficient can be selected small when the number of bits is large. Furthermore, the good regulation from no load to full load is obtained as shown in Fig. 6 because the mmf (magneto motive force) of the reactor \( L \) is continuous in Fig. 1 and regulation range is enough wide [7], [8].
B. Dynamic Characteristics

Figures 7, 8 and 9 show the simulated transient response when the load $R_1$ is step changed from 50Ω to 5Ω. In Fig. 7, the circuit parameters are same to Fig. 4(a). In Fig. 8 and 9, the circuit parameters are same to Fig. 4(b). The simulator is PSIM.

In Figs. 7, 8 and 9, $K_p$ is equal to 2, $K_D$ is equal to 2 and $K_I$ is changed as parameters. Figure 7 shows that the overshoot and undershoot of the output voltage $e_{o1}$ are over 2.8% and 4.5% in case of $K_I = 0.03$ and $Q_I = 15$bits. The convergence time $t_{st}$ that the output voltage $e_{o1}$ is settled within 1% is equal to 4.0ms. The overshoot of reactor current is over 97%. Figure 8 shows that the overshoot and undershoot of the output voltage $e_{o1}$ are over 2.1% and 4.6% in case of $K_I = 0.022$ and $Q_I = 15$bits. The convergence time $t_{st}$ that the output voltage $e_{o1}$ is settled within 1% is 3.1ms. The overshoot of reactor current is over 90%. Next, to achieve the improvement of the dynamic characteristic, the number of bits of the calculation part of the digital control circuit $Q_I$ set enlarged. Figure 9 shows that the overshoot and undershoot of the output voltage $e_{o1}$ is over 0.7% and 4.7% in case of $K_I = 0.011$ and $Q_I = 16$bits. The convergence time $t_{st}$ that the output voltage $e_{o1}$ is settled within 1% is 3.0ms. The overshoot of reactor current is over 77%.

It is seen that the overshoot, the convergence time $t_{st}$ of the output voltage $e_{o1}$ and the overshoot of reactor current $i_L$ are improved in case of the new suitable rating input voltage. Moreover, transient responses are improved when the number of bits of the calculation part of the digital control circuit $Q_I$ set enlarged.

Figures 10, 11 and 12 show the experimental transient response are step change the same as simulation.

Figure 10 shows that the overshoot and undershoot of the output voltage $e_{o1}$ is over 2.7%, 4.3% in case of $K_I = 0.03$ and $Q_I = 15$bits. The convergence time $t_{st}$ that the output voltage $e_{o1}$ is settled within 1% is 4.0ms. The overshoot of reactor current is over 97%. Figure 11 shows that the overshoot and undershoot of the output voltage $e_{o1}$ are over 1.9%, 4.1% in case of $K_I = 0.022$ and $Q_I = 15$bits. The convergence time $t_{st}$ that the output voltage $e_{o1}$ is settled within 1% is 3.2ms. The overshoot of reactor current is over 86%. Next, to achieve the improvement of the dynamic characteristic, the number of bits of the calculation part of the digital control circuit $Q_I$ set enlarged. Figure 12 shows that the overshoot and undershoot of the output voltage $e_{o1}$ are over 0.6% and 4.3% in case of $K_I = 0.011$ and $Q_I = 16$bits. The convergence time $t_{st}$ that the output voltage $e_{o1}$ is settled within 1% is 3.2ms. The overshoot of reactor current is over 81%.

It is seen that the transient response is improved as same as the simulated results.
Fig. 7 Transient response in case of $K_I=0.03$ and $Q_I=15$bits (Simulated results).

- Overshoot: 2.8%
- Undershoot: 4.5%
- $t_{st}: 4.0\text{ms}$

Fig. 8 Transient response in case of $K_I=0.022$ and $Q_I=15$bits (Simulated results).

- Overshoot: 2.1%
- Undershoot: 4.6%
- $t_{st}: 3.1\text{ms}$

Fig. 9 Transient response in case of $K_I=0.011$ and $Q_I=16$bits (Simulated results).

- Overshoot: 0.7%
- Undershoot: 4.7%
- $t_{st}: 3.1\text{ms}$

Fig. 10 Transient response in case of $K_I=0.03$ and $Q_I=15$bits (Experimental results).

- Overshoot: 77%
- $t_{st}: 3.0\text{ms}$
IV. CONCLUSION

The transient response to step change of the load is discussed in the digital control circuit for the forward type multi-output DC-DC converter. Moreover, it introduced the smart approach for design of digital control.

It is important to set the suitable integral coefficient for not only static characteristics but also dynamic characteristics. It seems that excellent characteristic is obtained when the new suitable rating input voltage is selected. As a result, overshoot and the convergence time of the output voltage are improved 30% and 30%. The overshoot of reactor current is improved 11%.

Moreover, to achieve the improvement of the dynamic characteristic, the number of bits of the calculation part of the digital control circuit set enlarged. Lastly, it is revealed that the overshoot and the convergence time of the output voltage are improved 78% and 30%. Furthermore, the overshoot of reactor current is improved 17%.

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