Al-alloyed local contacts for industrial PERC cells by local printing

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***Abstract* — In this paper, a detailed investigation of the Al-alloyed local rear contacts for industrial PERC cells is presented. Three types of voids and their influences to PERC cells are evaluated with 2D numerical device simulations. By a detailed study of the formation mechanism of local contacts, an effective method of two-step metallization is proposed to suppress the generation of voids. In step 1, the Al paste is locally printed to limit the lateral diffusion of Al into Si during the firing process. In step 2, a full-area metallization with low temperature firing is applied to connect all the rear local Al contacts. With this method, a clear decrease of the void density after an industrial firing process is demonstrated. Nearly 0% voids rate can be achieved if the design width of the Al contact is small enough. This can prevent the recombination of minority carriers at the rear side, and contribute to V_{oc} over 666 mV. Average cell efficiency of 20.26% and best efficiency of 20.50% are achieved in batch run in a pilot line. With advanced module technologies, a best module power of 326.3 W_p was achieved for a 60-cell-based module and independently confirmed.**

***Index Terms* — voids, PERC cell, metallization, screen printing.**

I. Introduction

Industrial PERC silicon solar cells with rear Al local contacts benefit both from a reduction of recombination at the rear side due to the surface passivation, and an improved carrier generation because of the better optical reflection from the rear side. However, during the fabrication of Al-alloyed local contacts, voids (also called cavities) are commonly observed [1-5].

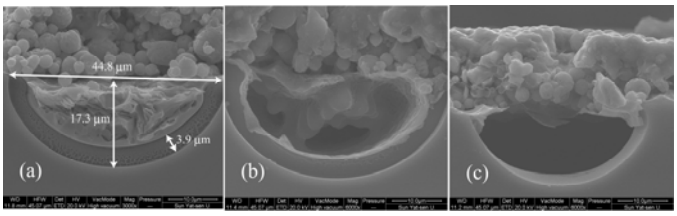

Fig. 1. SEM images for local BSFs fabricated with screen printing, (a) a contact with a thin BSF, (b) type 2 void: Al-p^+ layer and Al-Si eutetic is only partly connected; and (c) type 3 void: without BSF.

According to the SEM images shown in Fig. 1, voids can be cassified into three types: 1) Recombination voids: only a very thin Al-p^+ layer is formed, which causes a high amount of recombination at the contacts. 2) Resistive voids: the contact area between the Al-p^+ layer and the metal contact (Al-Si eutectic) is reduced, which increases the contact resistivity. 3) R&R voids: practically no Al-p^+ layer is formed. This leads to both high recombination and high resistive losses.

II. Numerical simulations

For resistive voids and R&R voids, we set up a 2D simulation domain containing 4 front contacts and 7 rear contacts, with the device simulator Sentaurus [6]. The front finger and rear line-contact spacings are assumed to be 1200 µm and 600 µm, respectively. For all the void simulations, a Cz *p*-type wafer base was chosen, with thickness of 180 µm and resistivity of 3 Ωcm. As shown in Fig. 2, the most severe reduction of the minority carrier density (electrons) appears near the voids, which becomes significant if the number of voids increases.

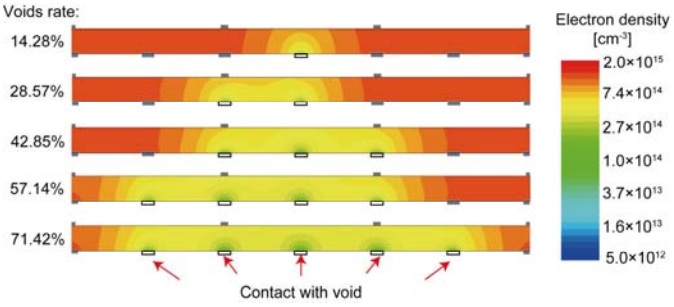

Fig. 2. Simulated electron density in the PERC cell with voids (without BSF) at an imposed voltage of 660 mV. The simulation domain contains 4 front contacts and 7 rear contacts. The grey contacts denote good contacts with BSF, while the empty contacts represent contacts containing void. The average minority carrier density decreases with increasing void rate.

Fig. 3 shows how resistive and R&R voids affect cell performance. The fraction of local BSFs that have void problem is varied from 15% to 60% (x-axis). For resistive voids, the dash curves show cell efficiency for a reduction of the contact area to 10%, 20% and 50%, respectively. For example, when 60% of the local contacts are type 2 voids, and only 10% of the BSF region is connected to the Al-Si eutetic, cell efficiency drops by 0.15% absolute. For the type 3 voids, when no Al-p^+ layer is formed, both cell efficiency and V_{oc} decrease dramatically as the voids density increases, as indicated bv the solid curve in Fig. 3. This has two reasons: first, the carriers near the void region suffer from the severe surface recombination. Second, the majority carriers need to travel a longer distance to another void-free contact to be collected, hence an addtional resistive loss is introduced. Therefore, the type 3 voids are very detrimental to the device performance and must be avoided [7].

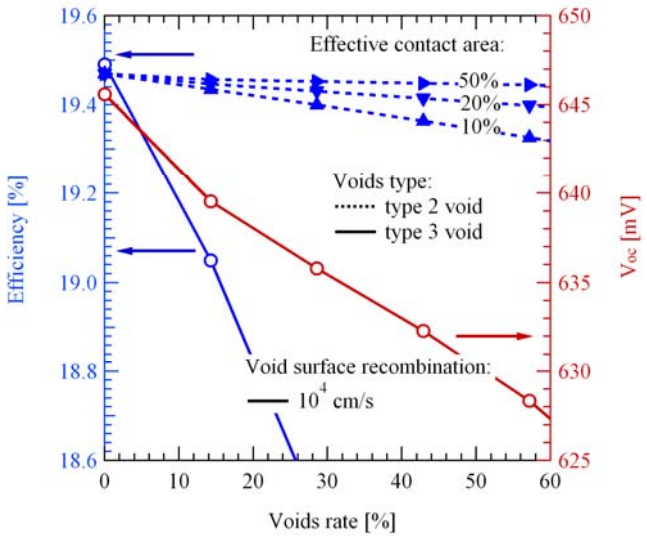

Fig. 3. Simulated cell efficiency (blue curves, left axis) and V_{oc} (red curve, right axis) as a function of void density, for voids with a BSF (dash curves) and voids without BSF (solid curve). For void with BSF, partial BSF is assumed to be contacted with the Al-Si eutetic, with a contact area of 10%, 20% and 50% of the whole LBSF surface, which increase the contact resistivity. For void without BSF (type 3), the surface recombination velocity is set to 10^4 cm/s.

III. EXPERIMENTS

The formation of voids can be explained by the Kirkendall effect [8], which is caused by the difference in diffusion velocity between materials. For instance, during the firing process, Si starts to diffuse into the Al layer and forms an Al-Si liquid state at 660°C. During the melting, Si dissolves into Al quicklier than Al diffuses into Si, which results in voids at the local contacts. During cooling down, Si atoms start to travel back from the Al-Si liquid into the local contacts when the solubility of Si in Al decreases. The Al-Si liquid starts to re-solidify when the temperature is lower than 577°C. If the re-solidification process is long enough, some Al atoms remain in the Si crystal lattice and replace the Si atoms as acceptors, while the Al-Si liquid solidifies as Al-Si eutetic layer. If the cooling is too quick, the Al-Si liquid will re-solidify in the Al matrix, so the voids in the local contacts are only partly or cannot filled in.

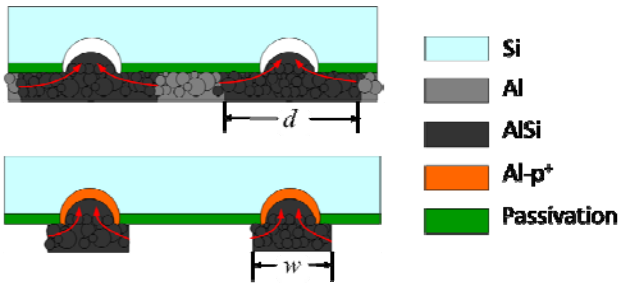

Fig. 4. Schematic diagram of contact formation for conventional full-area screen printing and local screen-printing

A. The local printing method

The key solution to suppress the formation of voids is to make sure that the concentration of Si in the Al-Si liquid at the local contact is sufficiently high before cooling, which will limit the further diffusion of Si into the Al-Si liquid. This can be accomplished by various approaches, i.e., by enlarging the local opening area [9], reducing the pitch of local contacts [9, 10], adding Si into the Al paste [4], or by adjusting the firing procedure [11]. In this paper, we propose to limit the diffusion of Si by a local printing method. As illustracted in Fig. 4, for the first step, the Al paste is printed locally on the local openings of the rear passivation layer. During firing, the diffusion length, especially the lateral diffusion length *d*, is highly limited by the width *w* of the printed Al. In the second step, a full-area metallization can be applied to connect all the local contacts by screen printing or evaporation to reduce the series reststance of the rear side. An annealing with a temperature lower than 660°C is necessary to ensure adheison between the local fingers and the second metal layer. The schematic diagram of the idea of local printing with comparison to full-area screen printing is illustrated in Fig. 4.

B. Experiment designs

The experiments were performed on 156×156 mm^2 quasi-square boron-doped Cz *p*-type wafers with 0.5 - 3 Ωcm resistivity. The surfaces of the wafer were alkaline polished and covered with passivation stacks. The line-shaped openings were formed with a green laser ablation of the passivation layers. In our experiments, the rear opening width and pitch were fixed to 40 µm and 1 mm, respectively. After alignment with screen printing, the Al pastes are locally printed to cover the openings. After drying, the samples were

sintered with a standard firing process. After that, the samples were cut into 1 cm long strips for measurement. After scratching the Al layer, the observation of voids was performed with a microscope. The cumulative length of voids is divided by the total length of the sample to yield the void rate. The voids rate is observed to decrease significantly when the design width is small enough, as illustrated in Fig. 5. This is because of the lateral diffusion of Si into Al-Si liquid is greatly limited by the printing width *w*. By reducing the design width to 30 µm, less than 1% void rate was detected.

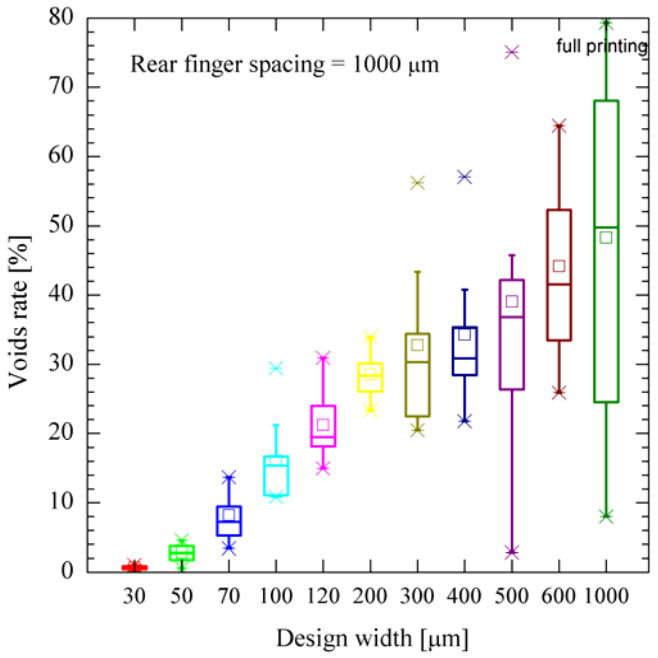

Fig. 5. Voids rate statistics as a function of the design width of the local opening, as determined by microscope for line-contacts. The opening width of the rear passivation layer is 40 µm, with a pitch of 1000 µm.

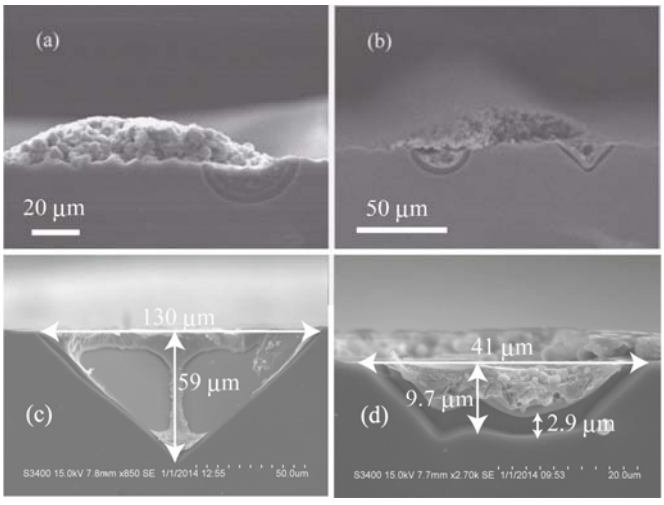

Fig. 6. SEM images of a local contact with (a) misalignment problem, (b) scatch during processing, (c) point-contact with full-area printing and (d) point-contact with local printing.

C. Point contacts

One of the problems of this local printing method is the alignment of the local printing to the openings. Fig. 6 (a) shows an example of a clear local BSF without void, when the printing paste partly covers the opening. Fig. 6 (b) shows another possible problem in manufacturing where two small local contacts are formed, the one with a triangle shape, being caused by scratch through the passivation layer during processing.

Point contact, instead of line contact, is a promising structure for high efficiency PERC cells. However, since the metallization area is reduced, point-contact PERC cells are more vulnerable to voids. Fig.6 (c) shows a void with a depth of about 60 µm for full-area printing point contacts, which may lead to cracks during the module fabrication. While with local printing, a good point contact less than 10 µm depth can be formed, as illustrated by Fig. 6 (d). With point contacts and local printing, V_{oc} than 666 mV were achieved experimentally, as shown in Fig. 7.

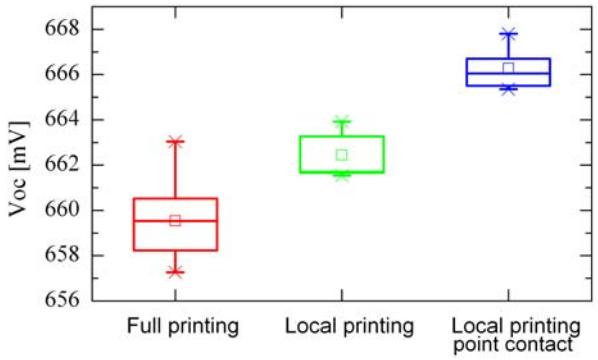

Fig. 7. V_{oc} distributions for line contacts with conventional metallization (red), and with local printing (green), and for point contact with local printing (blue).

D. Solar cell and module results

For the solar cells fabrication, 156×156 mm^2 quasi-square boron-doped *p*-type Cz wafers with resistivity from 0.5-3 Ωcm are used as substrates. In the front side, the selective emitter is covered with optimized double-layer SiN_x:H anti-reflection coatings to reduce the optical losses, while the 3 busbars (1.5 mm width) “H” pattern is applied for the front metallization. For the rear side, the surface is shiny polished and coated with passivation layers. After local opening of the rear dieletrical passivation layers by laser, the Al-paste is printed on the rear surface to form the local BSFs. The results of the solar cells which are fabricated in a pilot line, are shown in TABLE I. The average cell efficiency is 20.26% and

the best efficiency is 20.51%, with V_{oc} of 662 and 664 mV, respectively.

TABLE I
BATCH EXPERIMENT CELL RESULTS IN PILOT LINE

	Counts [pcs]	V_{oc} [mV]	J_{sc} [mA/cm2]	*FF* [%]	*Eff.* [%]
Avg.	437	662.0	39.04	78.54	20.26
Best	\	664.1	39.26	78.71	20.50

With the industrial PERC structure, *p*-type full square 156×156 mm^2 wafers are used for high power output module fabrication. With delicate designs to reduce the optical reflections as well as to optimize resistive loss in the module level, and combined with the latest advanced module technologies developed in the Trinasolar high-efficiency module team, module power over 320 W_p is demonstrated on 60-cell-based modules (120 half-cut cells), with the highest power of 326.3 W_p, which is independently confirmed by TÜV Reinland (Shanghai) Co., Ltd., as shown in TABLE II.

TABLE II
HIGH POWER 60-CELL-BASED MODULE RESULTS*

Module serial No.	V_{oc} [V]	I_{sc} [A]	*FF* [%]	P_{mpp} [W]
Z140329000001	78.69	5.304	77.0	321.3
Z140470800001	78.65	5.321	77.1	326.3

IV. CONCLUSIONS

A detailed study of the Al-alloyed local contacts for industiral PERC cells by commercial screen printing is presented. The voids in the local rear contacts are divided into three types. Numerical device simulations were performed to analyze the influence of voids. A two-step metallization method to suppress the generation of voids is proposed. A void density of less than 1% was demonstrated experimentally. The method can be used in the fabrication of point contact PERC cells. An open-circuit voltage greater than 666 mV was achieved, with a depth of local contact shallower than 10 µm. An average cell efficiency of 20.26% and best efficiency 20.50% are demonstrated in the pilot line. With the full square PERC cells, module power over 320 W_p is demonstrated on the 60-cell-based modules, with a best power of 326.3 W_p.

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