AN ASIC IMPLEMENTATION OF 16-BIT FIXED-POINT DIGITAL SIGNAL PROCESSOR

Xuan-Thuan NGUYEN[1, *], Trong-Tu BUI[1], Huu-Thuan HUYNH[1]
Cong-Kha PHAM[2], Duc-Hung LE[2]

[1]*The University of Science, Ho Chi Minh, Vietnam*
[2]*The University of Electro-Communications, Tokyo, Japan*

*Email: nxthuan@fetel.hcmus.edu.vn

Received: 15 July 2013, Accepted for publication: 16 October 2013

ABSTRACT

In this paper, an ASIC implementation of 16-bit fixed-point digital signal processor (DSP) is proposed. This DSP is based on the Harvard architecture and is composed of 16 24-bit general purpose registers together with 41 four-cycle instruction sets. The DSP hardware is designed by Verilog HDL, simulated by Modelsim, and verified in an FPGA of Altera. Subsequently, Synopsys tools including Design Compiler (DC), IC Compiler (ICC), PrimeTime etc. are employed to perform the ASIC design process. The 0.18μm fabricated chip, finally, is fully tested to prove the performance.

Keywords: DSP, ASIC implementation, FPGA implementation.

1. INTRODUCTION

Digital signal processing has become widely available in a large number of applications such as audio and speech signal processing [1], digital image processing [2], signal processing for communications [3], biomedical signal processing [4] etc. However, standard computers designed for general applications are not optimized for digital signal processing algorithms (i.e. digital filtering, Fourier analysis). Therefore, digital signal processors (DSP) [5, 6], kinds of specialized microprocessors, have been created to handle specific digital signal processing tasks. Currently, beside the purpose-built hardware such as Application-Specific Integrated Circuits (ASICs), there are additional technologies used for digital signal processing including more powerful general-purpose microprocessors, digital signal controllers, Field-Programmable Gate Arrays (FPGAs) etc.

Research and design on DSP architecture is highly desirable due to its vital role. Ishikawa T. et. al. [7] described a 16-bit fixed-point DSP for telecommunication applications such as modems or low-bit-rate speech CODECs. The DSP was fabricated with 0.5 μm CMOS process and achieve 80 MOPS-peak performance and 40 MIPS at 3.0 V. Kabuo H. et. al. [8] designed a

16-bit fixed-point DSP with optimized multi-accumulate (MAC) unit, memories, and instruction sets, which reduced the area and power consumption significantly. The fabricated 0.5 μm double-metal-layer CMOS process DSP can attain 80-MOPS-peak double speed MAC performance. O'Malley E. et. al. [9] proposed a novel and highly vertisale reduced instruction set (RISC) based fixed-point DSP which is optimized for digitally controlled switched mode power converters (SMPCs). The integrated circuit was built on a standard 0.35 μm digital CMOS process which can achieve 50 MIPS, occupy less than 1.5 mm^2, and dissipate approximately 5 mW at 3.3 V. Donghoon Lee et. al. [10] represented an FPGA implementation of 16-bit fixed-point DSP. The DSP included 211 instructions and 40-bit ALU, 6 level pipelines, 17-bit x 17-bit parallel multiplier for single-cycle MAC operation, 8 addressing modes, 8 auxiliary registers, 2 auxiliary register arithmetic units, 2 40-bit accumulators and 2 address generators. The DSP core carried out three test vector sets which are tested at FPGA at the 106 MHz clock rates.

This paper described an FPGA and ASIC implementation of 16-bit fixed-point DSP. This DSP achieves four clock cycles per instruction at the clock rate of 40 MHz and supports multiply accumulate (MAC) operations with 24-bit precision. The processor, initially, is designed by Verilog HDL and simulated by Modelsim. Subsequently, an audio processing system integrated with the DSP is constructed and verified in an FPGA of Altera. After successfully testing, the Synopsys tools including Design Compiler (DC), VCS, IC Compiler (ICC), Prime Time, Hercules, StarRC are utilized to obtain the synthesized circuit, circuit simulation and layout, circuit timing analysis, and the parasitic components, respectively. The DSP, then, is fabricated by a 0.18 μm CMOS technology. The designed chip operates on 1.8 V and dissipates 1.6 mW at 40 MHz.

The remainder of this paper is organized as follows. The DSP implementation containing the architecture and instruction sets is described fully in Section 2. The experimental results of FPGA and ASIC implementation of DSP are presented in Section 3. The conclusion, finally, is provided in Section 4.

2. IMPLEMENTATION

The DSP architecture supports separate instruction and data ports, classifying it as a Harvard architecture. The data port connects to both memory and peripheral components while the instruction port connects only to the memory components. The instruction and data memory size are 4 K x 16 bits and 64 K x 16 bits, respectively. Furthermore, the DSP has 16 24-bit general-purpose registers indexed from r0 to r15, which can be used in many arithmetic logic unit (ALU) operations, except for r0 which is not used as an operand. ALU operations take one or two inputs from registers, and store the results back in the registers with up to 24-bit precision. Although the control of subroutines is similar to other processors, a register (generally r0) must be dedicated to protecting the returning address. The same register, subsequently, can be utilized to return to the calling point.

The RISC-based architecture of DSP utilizes 2 24-bit buses, one for operands and one for results, as depicted in Fig. 1 When the DSP is restarted, 12-bit program counter (PC) is set to address 0. At the start of each instruction, PC is used to read an instruction from the memory as an address register. The 16-bit instruction is stored in IR and the PC is automatically incremented to point to the next instruction. The bank of registers that maintain the values of r0 to r15 is a memory with synchronous writing and asynchronous reading.

By using two different buses to exchange data to external elements (i.e. one to send data and one to receive them), the design avoids additional tri-state buffers that, indeed, are not necessary within the chip. Although having three or more buses can allow the processor to realize all the instruction operations in only one clock cycle, this DSP only employs two buses to avoid using dual-port memories for the bank of registers. Through these buses, rD and rS|T can be observed during the first- and last-two phases of each instruction cycle, respectively.

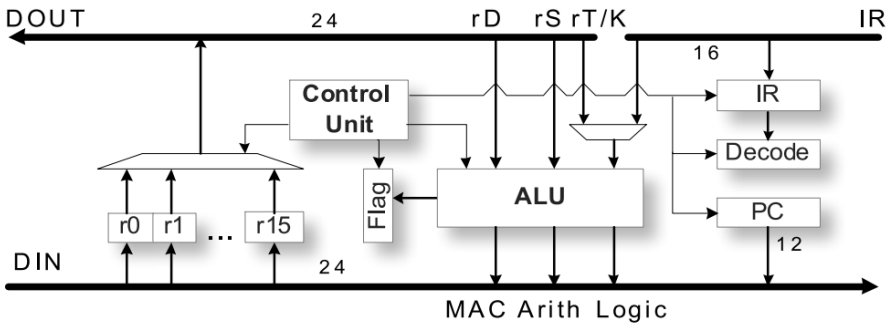


Figure 1. Detailed block diagram of DSP chip.

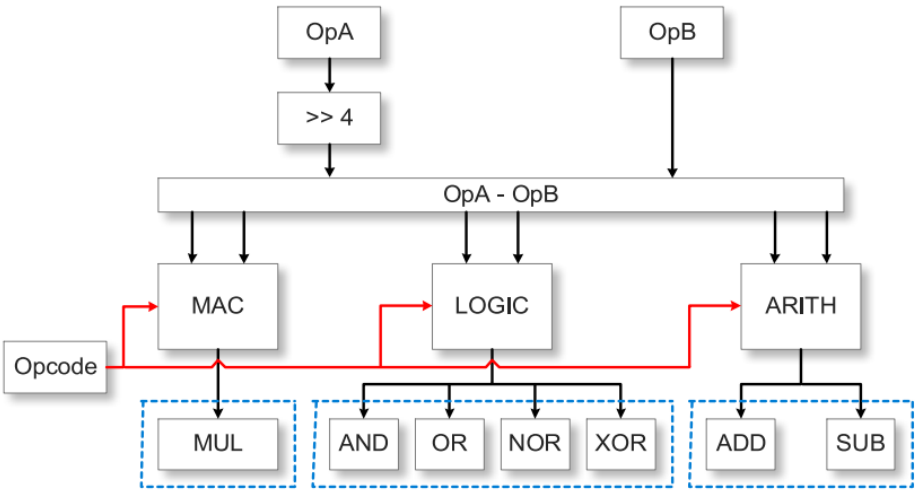


Figure 2. Block diagram of ALU.

The ALU, as depicted in Fig. 2, performs logic, arithmetic, and product operations. After each instruction, the zero (Z), sign (S), and overflow (V) flags are updated, which allows DSP to carry out the corresponding allocations and conditional jumps. It is worthy to notice that this processor does not require the carry flag (C) because of the single precision operations. The bus of results is dedicated to collecting the outputs of ALU and other sources (i.e. the external data upon reading from a port, the value of the PC when calling a subroutine etc.)

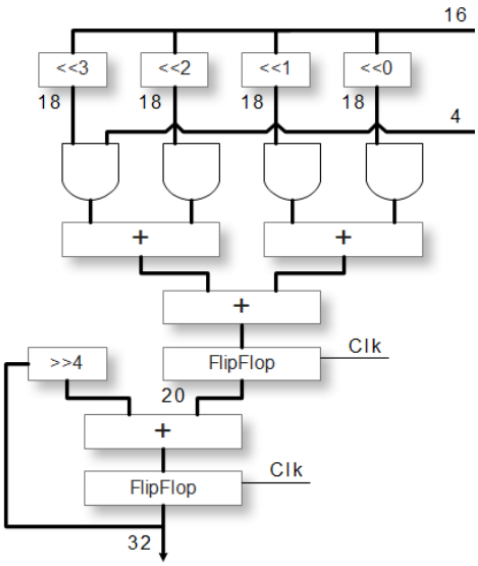
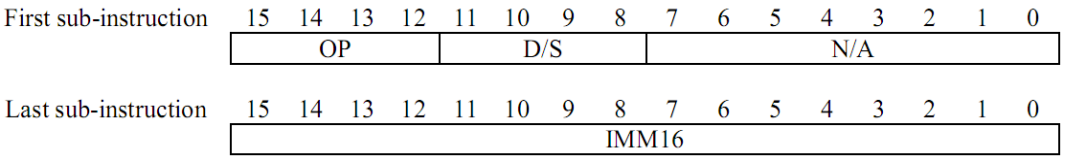


Figure 3. Block diagram of a multiplier.

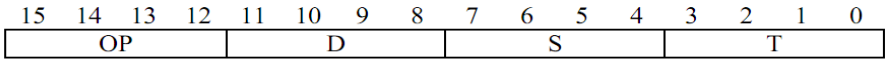
Furthermore, the central operation of this DSP is the multiplication, which operates on two 16-bit values and generates a 24-bit result. In other words, the operands and result are in 1.15 and 1.23 format, respectively. In order to build the multiplier, it has been decided to dividing the operation into four stages, multiplying in each step a 16-bit operand by another one of only four bits, emitting a 20-bit intermediate result. This operation can be made with only four adders and an intermediate segmentation register as shown simplified in Fig. 3. If the operation is implemented in a single clock cycle, 15 adders must be utilized, and the latency would have been greater due to the segmentation registers.

Instruction Sets: The DSP supports up to 41 instructions by combining 16 different opcodes with 8 flag types, which is divided into three types: I-type, R-type, and J-type.

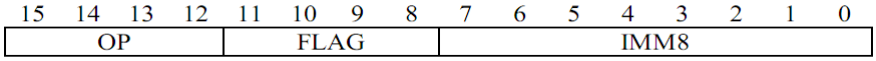
I-type: The defining characteristic of the I-type instruction word format is that it contains an immediate value embedded within the instruction word. I-type instructions words contain a 4-bit opcode field OP, a 4-bit register field D/S, and a 16-bit immediate data field IMM16. IMM16 is considered signed and unsigned comparisons. I-type instructions include load and store operations; its format is depicted as follows.



R-type: The defining characteristic of the R-type instruction word format is that all arguments and results are specified as registers. R-type instructions contain a 4-bit opcode field OP and three 4-bit register fields D, S, and T. Fields S and T specify the source operands, and field D specifies the destination register. R-type instructions include arithmetic and logical operations such as ADD; its format is illustrated as follows.



J-type: J-type instructions contain a 4-bit opcode field OP, 4-bit flag field FLAG, and 8-bit address field IMM8. J-type instructions include absolute jump such as CALL and conditional jumps; its format is shown as follows.



The most beneficial operation of this processor is the fixed-point product, with or without accumulation. In general, 2 16-bit normalized operands are taken, and a 24-bit normalized result is produced. All accumulations, additions, and subtractions are designed with a resolution of 24 bits. Another kind of product is also available, represented as rD = rS x rT, which allows to make displacements. The second operand is interpreted in 8.8 format so that any value can be multiplied by 1/128, 1/64, ..., 1/4, 1/2, 2, 4, ..., 32, 64, in addition to other intermediate values, resulting in the desired adjustment.

3. EXPERIMENTAL RESULTS

The proposed DSP, firstly, is implemented on an Altera DE2-115 development board equipped with a Cyclone IV EP4CE115 FPGA chip. The resource utilization consisting of the combinational functions, dedicated logic registers, memory bits etc. is shown in Table 1. The DSP maximum operating frequency is above 90 MHz according to the Altera TimeQuest Timing Analyzer.

Table 1. The resource utilization.

Device	Cyclone IV EP4CE115
ALUTs	663/114,480 (1%)
Registers	210/114,480 (1%)
Memory Bits	384/3,981,312 (1%)
Embedded Multiplier	0/532 (0%)
Maximum Frequency	94 MHz

Secondly, a full audio processing system is designed to verify the chip performance. The system is composed of an instruction memory and a data memory, which are used to store the instructions and data, respectively. A basic I/O module is integrated in the system to communicate with several external interfaces in the development board (i.e. switches, push buttons, and red leds). An audio controller, then, is attached to control the WM8731, i.e. an audio codec chip, so that the system can receive and transmit the sound data. Some basic digital signal processing algorithms, subsequently, are employed to verify the DSP performance.

The DSP, thirdly, is implemented as an ASIC. The HDL code is converted into RTL form and is synthesized by the DC. The VCS, then, is exploited to simulate the circuit function. After successful simulation, the ICC is utilized to obtain the circuit layout. A high overall yield and reliability verification of the design, subsequently, is achieved by Hercules, i.e. Design Rule Check (DRC) and Layout versus Schematic (LVS). Besides, StarRC is used to calculate the parasitic effects on both the designed devices and the required wiring interconnects of the circuit. Timing, signal integrity, power, and variation-aware analysis, then, are obtained by PrimeTime to reduce design risk and enhance design reliability.

A die photograph of DSP chip is shown in Fig. 4. The chip is fabricated in a 180-nm CMOS process with six metal layers. It costs 2411 cells and the layout area of 373.76 μm x 372.97 μm. The DSP is put on a socket which is connected to the FPGA board through general-purpose I/O extension as shown in Fig. 5. After the audio processing system is restarted, DSP chip loads the instructions and data stored in the internal memories of FPGA. The results, then, are sent back to data memory, or displayed on the leds, depend on the certain instructions. Altera SignalTap tool is utilized to observe and evaluate the waveforms. With the power supply of 1.8 V, the chip operates at the maximum frequency up to 40 MHz (cycle time of 25 ns). The measurement shows that the power dissipation at 40 MHz is 1.6 mW, which is suitable for audio signal processing. TABLE 2 summarizes the DSP features.

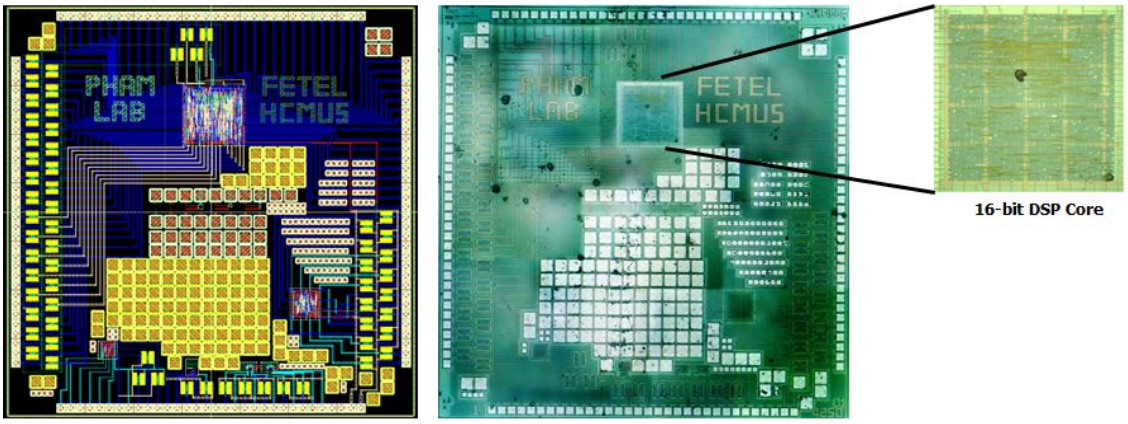


Figure 4. The DSP layout (a) Die photograph of DSP chip in IC Compiler (b) Die photograph of fabricated chip after tape-out (c) The 16-bit fixed-point DSP core.

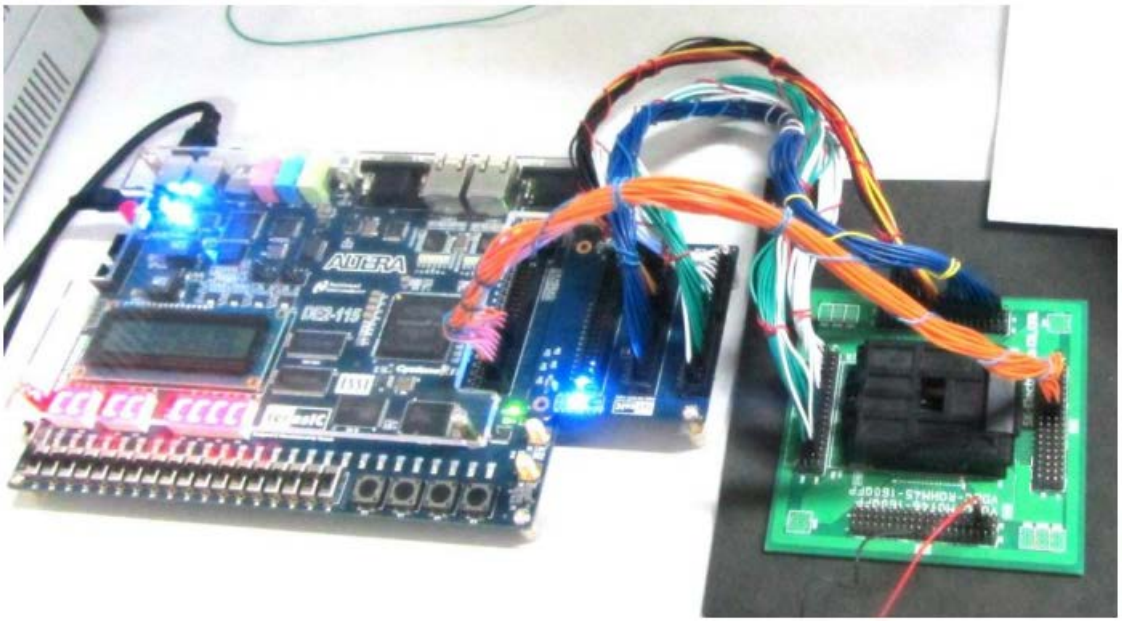


Figure 5. The proposed testing method.

Table 2. Specification of DSP chip.

Technology	180 nm CMOS/6 metal layers
Supply	1.8 V
Power Dissipation	1.6 mW @ 40 MHz
Cells Count	2411 cells
Layout Size	373.76 µm x 372.97 µm

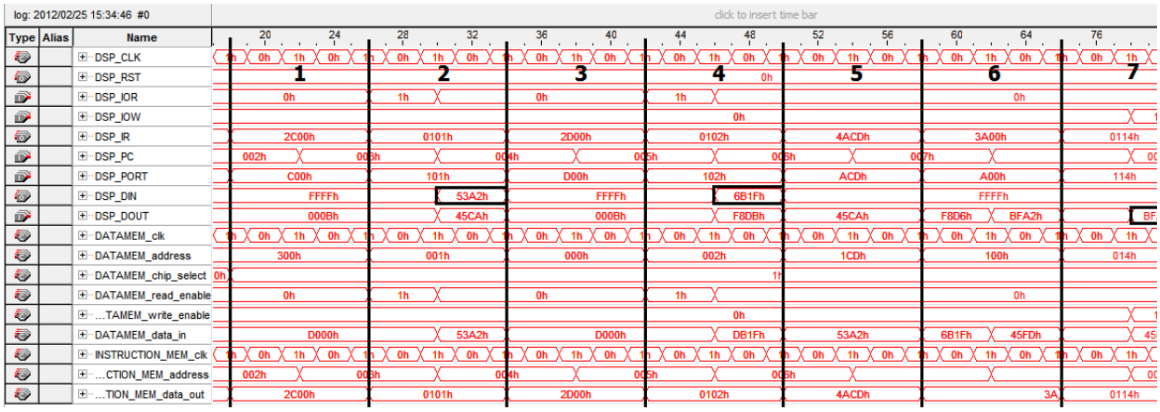


Figure 6. The waveform of normalized product.

One of the DSP function verifications, a normalized product 1.15*1.15, is illustrated in Fig. 6. In this experiment, seven instructions are utilized to load, compute the operands, and store the result back to memory. The first and the second operand are 0.6534 and 0.8369, respectively, which are expressed in fixed-point form as two hexadecimal numbers 0x53A2 and 0x6B1F. The product result is 0.5468, which is equivalent to 0x45FDAD.

In the beginning, 0x53A2 and 0x6B1F are stored in data memory. Instruction 1 (0x2C00) and 2 (0x0101) loads the value 0x53A2 from data memory to DSP chip through DIN port. Instruction 0x2C00 means that DSP reads data from external ADDR of 0x0101 and stores them to register rC. Instruction 0x2D00 and 0x0102, similarly, assign rD the value of ADDR of 0x0102. Instruction 0x4ACD performs the multiplication of register rC and rD and stores the result back to rA. The result, then, is moved to data memory by instruction 6 (0x3A00) and 7 (0x0114). Because output data width is only 16 bits, the result is modified as 0x45FD instead of 0x45FDAD. However, the final result is expressed as 0xBFA2 due to the little-endian format. The result proves that the DSP worked properly.

4. CONCLUSION

We have proposed an ASIC implementation of 16-bit fixed-point DSP. The chip supports up to 41 instructions due to the combination of opcodes and flags. The central operation of this chip is MAC instruction, which can be completed in four clock cycles. The DSP is verified properly in an FPGA for audio processing applications. After that, it is migrated to ASIC by using Synopsys tools. The test results show that the chip operates reliably at 1.8 V @ 40 MHz and the power dissipation is less than 1.6 mW, which is appropriate to audio applications. The

performance can be improved by using clock three synthesize techniques as well as low-power design techniques to enhance the speed and reduce the power dissipation.

Acknowledgement. This work is the cooperation between the University of Electro-Communications Tokyo (UEC) and the University of Science, Ho Chi Minh City. The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Inc. This work is also supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc., Synopsys.

REFERENCES

1. Roll T., Vepa L., Wuenschmann J., and Rothermel A., - Audio Signal Processing Adapted to Mobile Reception of DVB-T, IEEE Trans. Consumer Electronics **57** (4) (2011) 1899-1906.
2. Xuan-Thuan Nguyen, L.Hoai-Phong Nguyen, Trong-Tu Bui, and Huu-Thuan Huynh, - A DSP Implementation for Real-time Hand Gesture Recognition Applications, 12th IEEE Int. Symp. Signal Processing and Information Technology (ISSPIT), Dec. 2012.
3. Gatherer A., Stetzler T., McMahan M., and Auslander E., - DSP-based Architectures for Mobile Communications: Past, Present, and Future, IEEE Communications Magazine **38** (1) (2000) 84-90.
4. Yagi M., Shibata T., - An Image Representation Algorithm Compatible with Neural-Associative-Processor-Based Hardware Recognition Systems, IEEE Trans. Neural Networks **14** (5) (2003) 1144-1161.
5. B. Venkataranami, M. Bhaskar, - Digital Signal Processors, McGraw-Hill, 2002.
6. Keshab K. Parhi, - VLSI Digital Signal Processing Systems - Design and Implementation, John Wiley & Sons, Inc., 1999.
7. Ishikawa T., Suzuki H., Taki H., Homma K., Kabuol H., Okamotol M., Uedal K., Asah R., - A 16 bit Low-Power-Consumption Digital Signal Processor for Portable Terminals, 4th IEEE Int. Conf. Universal Personal Communications, Nov. 1995, pp. 798-802.
8. Kabuo H., Okamoto M., Tanaka I., Yasoshima H., Marui S., Yamasaki M, Sugimura T., Ueda K., Ishikawa T., Suzuki H., Asahi R., - An 80-MOPS-Peak High-Speed and Low-Power Consumption 16-bit Digital Signal Processor, IEEE Journal of Solid-State Circuits **31** (4) (1996) 494-530.
9. O'Malley E. , Rinne K., - A 16-bit fixed-point digital signal processor for digital power converter control, 20th Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Vol. 1, March 2005, pp. 50-56.
10. Donghoon Lee, Chanwon Ryu, Jusung Park, Kyunsoo Kwon, Wontae Choi, - Design and implementation of 16-bit fixed point digital signal processor, Int. SoC Design Conf. (ISOCC), Nov. 2008, pp. II-61 - II.64.