Electron beam lithography patterning of sub-10 nm line using hydrogen silsesquioxane for nanoscale device applications

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We investigated novel patterning techniques to produce ultrafine patterns for nanoscale devices. Hydrogen silsesquioxane (HSQ) was employed as a high-resolution negative tone inorganic electron beam resist. The nanoscale patterns with sub-10 nm linewidth were successfully formed. A trimming process of HSQ by the reactive ion etcher (RIE) played an important role for the formation of 5 nm nanowire patterns. Additionally, hybrid lithography was used to produce various device patterns as well as to minimize proximity effects of electron beam lithography (EBL). Finally, we successfully fabricated triple-gate metal oxide semiconductor field effect transistor (MOSFET) with a gate length of 6 nm by using the proposed patterning process. © 2005 American Vacuum Society. [DOI: 10.1116/1.2132328]

I. INTRODUCTION

Although the development of the semiconductor industry achieved remarkable outcomes in MOSFET technology during the last few decades, we are still faced with many technical challenges. Constant efforts are being focused on further scaling of MOSFETs. Since recent advances in electron beam lithography (EBL) permit a pattern size of several nanometers, MOSFETs with a very narrow channel and a fine gate length \( L_g \) have been successfully fabricated using silicon. As the device fabrication technology becomes more complex, a new approach is required to achieve extremely high accuracy patterns. The proximity effect increases with the complexity of the pattern shape in conventional EBL techniques. In addition, the fluctuation from beam source and scanning manner becomes more severe as the size of the beam source approaches to pattern size. The development of a new resist can provide a solution. It is reported that hydrogen silsesquioxane (HSQ) and calixarene resist (CAR) effectively eliminate fluctuations in the line patterning. Especially, HSQ has very interesting properties in device fabrication processes. HSQ is widely used as an interlayer dielectric material in integrated circuits with a low dielectric constant. Moreover, HSQ is also known as a high-resolution negative tone inorganic EBL resist. Even though HSQ can produce extremely fine line patterns of less than 10 nm width, the single HSQ line pattern with a small size is easily peeled from the wafers during the pattern development process.

In this study, we developed HSQ resist trimming and hybrid lithography techniques to scale down the gate line patterns to sub-10 nm with high accuracy and reproducibility. The proposed technique was employed to achieve a triple-gate MOSFET with gate length of 6 nm.

II. EXPERIMENT

Silicon wafers were spin coated with FOX-12 (Dow Corning), which is a HSQ solution in methyl isobutyl ketone (MIBK). A 100 nm thick HSQ layer was coated after spinning for 45 s at 5000 revolutions per minute (rpm). This

Fig. 1. SEM images of nanoscale pattern and etched profile of Si.
HSQ layer was prebaked on the hotplate at 120 °C for 2 min. And then exposed by a CRESTEC 9210 thermal field emission EBL system at 50 kV with 20 pA beam current to produce an ultrafine pattern less than 10 nm. Then this HSQ layer was developed in a 2.38% tetramethyl ammonium hydroxide (TMAH) solution by an immersion process at 20 °C for 3 min and rinsed in DI water for 30 s.

Hybrid lithography to reduce exposure time consists of EBL for small fine patterns and photolithography for large patterns. For formation of complicated patterns, the combination of negative and positive tone e-beam resist was used. The first EBL used an inorganic negative tone resist HSQ. The second EBL was carried out by using the methyl 2-methypropanoate (PMMA) as a positive resist on the HSQ nano pattern. The PMMA was prebaked at 170 °C for 3 min and exposed by the EBL system. The PMMA pattern was developed in a MIBK: isopropyl alcohol=1:3 diluted aqueous solution for 30 s and rinsed in deionized (DI) water for 30 s.

The triple-gate n-MOSFETs were fabricated on the p-type (100)UNIBOND silicon on insulator (SOI) wafers with a 100 nm top silicon layer and a 200 nm buried oxide layer. The top silicon layer was partially reduced to less than 20 nm by a wet etching process using TMAH 2.38%. Using hybrid lithography, active channel region was defined to produce a narrow multichannel of 10–40 nm width. The active layer was etched by using an inductively coupled plasma (ICP) etching system with the mixed gas of SF₆ and O₂. After mesa-isolation of an active layer, the gate oxide was grown by thermal oxidation and poly-Si was deposited by low pressure chemical vapor deposition (LPCVD). The gate pattern was defined by the combination of EBL and photolithography. An extremely narrow gate pattern was defined by the reactive ion etch (RIE) trimming of the HSQ inorganic e-beam resist. A novel plasma doping process with PH₃/H₂ was used to form Source/Drain extensions without an additional high temperature annealing process after gate stack formation. Finally, the current-voltage (I–V) characteristics of the fabricated triple-gate SOI MOSFETs with sub-10 nm gate length were measured.

III. RESULTS AND DISCUSSIONS

Figure 1 shows the SEM images of the HSQ patterns and the profile after Si was etched using the HSQ as a hard mask for RIE. Figure 1(a) shows the plane SEM image of multiline patterns with a 10 nm width and a 300 nm pitch. It is found in Fig. 1(b) that the HSQ patterns have a good vertical profile with high aspect ratio of about 10:1. In spite of the small size pattern, the HSQ resist has a high resistance against the dry etch process. Figure 1(c) is the scanning electron microscope (SEM) image of a pattern after Si etching by the ICP dry etching system using HSQ as a hard mask. The poly-Si gate shows a vertically etched profile with 13 nm width and 100 nm heights. However, because of the large aspect ratio, sub-10 nm patterns were often peeled off during development process. Figure 1(d) shows the collapsed of HSQ patterns less than 8 nm in width.

![Fig. 2. HSQ trimming rate as function of etching time in RIE. Top width is (a) 21 nm, (b) 17 nm, (c) 14 nm, (d) 9 nm, and (e) 5 nm.](image-url)
For further scaling down to sub 10 nm gate length, the trimming process is necessary to achieve an effective pattern formation. This attempt was carried out by using the RIE trimming of HSQ. Figure 2 shows the plane SEM images of the resist trimming process. Conventional trimming processes for the organic resist were carried out by using O₂ plasma etching. However, while O₂ plasma etching does not work for the HSQ resist, this etching should improve pattern roughness. Since the HSQ has the property of a thermal oxide, CF₄ plasma trimming instead of O₂ plasma was used. Figures 2(a)–2(e) show the results of CF₄ plasma trimming; width is (a) 21 nm, (b) 17 nm, (c) 14 nm, (d) 9 nm, and (e) 5 nm. In this manner, the ultrafine patterns of 5.3 nm widths were successfully obtained. Also, from the slope of Fig. 2(f), the optimized trimming rate was estimated to be 4 nm/min.

Figure 3 shows the cross-sectional SEM images of HSQ patterns after the trimming process. It is found that the slope of gate patterns was extremely fine by a vertical profile. Therefore, we consider that the trimming process serves a very effective resist process for nanoscale pattern generation and structure fabrication.

Figure 4 shows schematic illustrations of hybrid lithography; first exposure onto HSQ and inorganic negative tone e-beam resist, and second exposure onto PMMA organic positive tone e-beam resist. No chemical reaction between HSQ and PMMA was observed.

Figure 5 shows several hybrid lithography processes for fabrication of nanodevices. Figure 5(a) is the SEM image of channel patterns generated by the hybrid lithography method, a combination of HSQ and PMMA. Figure 5(b) shows the SEM image of hybrid lithography with HSQ and the AZ5214E photoresist for gate pattern. The combination of two different resists provides drastic reduction of exposure time in EBL. Also, the hybrid lithography provides not only a reduction of the proximity effect but also various kinds of device patterns.

In Fig. 6, conventional electron beam lithography is compared with the hybrid lithography. The active channel patterns were defined by conventional electron beam lithography. The channel width was reduced to sub-10 nm, as shown in Fig. 6(a). However, the conventional lithography was not able to generate complicated patterns because the overlap of
electron backscattering increases in the fine-channel region. The generated patterns were largely different from the designed patterns drawn by a dotted line, as shown in Fig. 6(a). These results indicate the limitation of proximity effect correction in single layer nano patterning. However, nanopatterning by using hybrid lithography with a combination of HSQ and PMMA revealed different results, as shown in Fig. 6(b), where the proximity effects of electron beam lithography were successfully minimized by the hybrid lithography. Figure 6(c) shows the fine channel region after dry etching by using the PMMA single layer as the etching mask. Although a Si channel of 10 nm width has been obtained by conventional EBL, the generated pattern showed an asymmetrical pattern shape (left and right side of the Si structure). However, Fig. 6(d) shows a well-defined Si channel after dry etching, where the hybrid pattern was used as the etching mask.

Figure 7 shows an image of triple-gate MOSFETs. As shown in Fig. 7(a), the multichannel region was defined less than 20 nm, which is the thinner relative to the top-Si layer.

![Image](https://via.placeholder.com/150)

**Fig. 7.** SEM image of fabricated triple-gate MOSFET with 6 nm gate length.

Figure 7(b) shows the cross-sectional TEM image of the channel with 11 nm width, 12 nm thickness ($T_{si}$), and 3.8 nm gate oxide thickness ($T_{gox}$). Figure 7(c) shows the cross-sectional TEM image of the 8 nm gate MOSFET with a 14 nm oxide sidewall and a 30 nm nitride sidewall.

Figure 8 shows the electrical characteristics of SOI MOSFETs with triple-gate structures, where $L_g=6$ nm. $W_{ch}=12$ nm, and $T_{si}=12$ nm. Figure 8(a) shows the poly-Si gate structure etched by ICP etcher using mixed gases SF$_6$ :O$_2$ =5:1. As a result, a triple-gate MOSFET with $L_g=6$ nm was successfully fabricated. Figure 8(b) shows the subthreshold slope (SS) and drain induced barrier lowering (DIBL) were 274 mV/dec and 360 mV/V, respectively. Although the 6 nm gate length of this device is extremely small, the operational characteristic shows a good subthreshold slope and large on/off current ratio. Moreover, it is found that the drain current versus drain voltage ($I_D-V_D$) characteristics of the n-MOSFET showed a suppressed short effect as shown in Fig. 8(c).

IV. CONCLUSION

Nanoscale fabrication techniques for aggressively scaled MOSFETs were investigated. We demonstrated that the inorganic negative tone resist HSQ can be used in a reproducible process with small linewidth fluctuation for 10 nm patterns. Also, we showed that the trimming process of HSQ is an effective pattern formation technique for scaling down to 5 nm. The proximity effect was effectively eliminated and the exposure time drastically decreased by using hybrid lithography. Based on these novel processes, triple-gate SOI MOSFETs were successfully fabricated with a 6 nm gate length. The electrical characteristics of a triple-gate SOI MOSFET with a 6 nm gate length revealed normal operation. Therefore, we expect that the proposed process can provide more reliable technology for nanoscale device fabrications of less than 10 nm.