Abstract

This paper presents our effort to predict IC, packaging, and board level reliability problems. Micro-electronic based reliability problems are driven by the mismatch between the different material properties, such as thermal expansion, hygro-swelling, and/or the degradation of interfacial strength. In the past, such reliability problems were treated separately, but recent development have made clear that total product reliability concerns the interaction of IC, package, and PCB. This paper presents parts of our strategy to assess this integrated reliability by combining experimental and numerical techniques.

1. Introduction

At present, thermo-mechanical reliability of IC’s, packages and PCBs is still one of the major concerns in the electronic industry. Based on root cause analyses from observed failures of micro-electronic components, it is found that these reliability problems are often triggered by loadings associated with manufacturing processes. Adapting product designs and processes by physics based design rules, models, experiments, etc. enable us to efficiently adapt the critical parameters. For example, during the backend processes (metal depositions, etching, and chemical vapor deposition) stresses are build-up in IC layer stacks and during packaging manufacturing processes (such as die-attach and molding), testing (temperature cycling, moisture assessment) and/or actual service, thermally induced deformations and stresses further develop in the IC layers and the surrounding packaging materials. These deformations and stresses can become critical for board assembly since they affect the solder mount attachment, which will provide the sole electrical/mechanical connection of the electronic component to the printed circuit board. Under worst-case conditions, the developed deformations and stresses may eventually endanger the targeted lifetime of the product. As such, the reliability of IC’s, packages and packages mounted on PCB’s is one of the concerns in the electronic industry. Given the major trends in the electronics industry, miniaturization and function integration, an increase of the density of interconnects but also an increase of power dissipation density (thus temperature) are to be expected.

As part of our strategy, nonlinear Finite Element techniques are combined with dedicated experiments needed to verify the models. These experiments concern certain IC designs tested in worst-case packages as well as board level temperature cycle and shock tests to assess acceleration factors for a given package family. When the simulation results agree with the experimental results for these cases, the reliable models can be applied for predictive modeling in a wider range of geometry, materials, processes, and failure modes wider parameter study. The need for an integrated approach to assess the reliability throughout the total micro-electronic based product needs our attention today [1]. Figure 1 shows the areas of product development where our predictive modeling strategies focus on, including some examples of challenges to ‘design for reliability’.

1. IC – package
- prevent delamination
- passivation crack
- reliable 1st level interconnections

2. Package – board
- minimize warpage
- reliable solder
- delamination

3. Total board
- prevent delamination
- reliable 1st & 2nd level interconnections
- warpage
- drop resistant

Figure 1: Focus areas for predictive modeling to support design for reliability.

This paper presents our effort to predict IC, packaging, and board level reliability problems. The following topics are described:
1. From IC to Package: typically denoted as 1st level reliability problems (type 1 in Figure 1).
2. From Package to PCB: typically denoted as 2nd level reliability problems (type 2 and 3 in Figure 1).

This paper discusses two examples of topic 1. The first example is about the interaction between IC diffusion layers and the package, which is described in Section 2. Figure 2a shows an example of the IC interconnect metal structure that is shifted by the surrounding package. The second example is about both package and board assembly effects on the wire reliability (see Figure 2b). Section 4 discusses the current board level reliability predictions for solder lifetime, which is an example of topic 2. Figure 3 shows a typical fatigue failure for a 2nd level interconnect.
2. From IC to Package

Integrated Circuit (IC) designers have to design robust metal interconnect layouts that guarantee reliability during waferfab processes, package assembly, qualification tests, board assembly, lifetime, etc. Figure 2b shows an example of a damaged metal interconnect line and cracked passivation layer that covers the metal. Specially designed IC/package samples are developed to observe passivation cracks and to verify crack predictions from simulations for Energy Release Rate crack energy predictions by J integral approach. The samples contain ICs with various test structures designed in the top metal level of the interconnect stack which are present in the corners of the IC. Figure 4 shows a typical corner structure of the interconnect metallization, further referred to as ‘test structure’. Among others, test structures contain bond pads (purple squares) and a metal power line (wide red line).

Six different test structures are defined with varying values for parameter ‘a’. The structures are referred to as S1 till S6 with increasing distance ‘a’ [1]. Our initial idea was to trigger failures in a structure by making ‘a’ small, and to obtain a safe structure by making ‘a’ large. The ICs are further assembled in modern plastic encapsulated packages, which finally undergo a standard Temperature Cycle Testing (TCT). At various stages in the assembly and testing processes, Scanning Acoustic Microscopy (SAM) analyses are performed to determine the amount of delamination at the IC/compound interface. After TCT, packages are decapped and various analyses are performed to observe failures such as pinhole analyses (passivation cracks), visual inspection (metal shift and passivation cracks), Scanning Electron Microscopy (SEM) & Focused Ion Beam (FIB) analyses (cross-sections).

Parametric Model

Figure 5 shows the parametric 3D model. Due to symmetry, ¼ of the package is modeled. The small structures on top of the silicon contain dielectrics, metal seal, metal bond pads, metal lines, and passivation. Figure 6 shows a magnification of the models cross-section. The passivation (blue) is covering the metallisation (orange) and is the same color as the substrate in this figure. A magnification is shown of the crack location and mesh. 3D models are developed to predict the distribution of J-values in the corners of the IC (3D effect).

Material Properties and Loadings

To obtain reliable models, reliable material models are vital. Because they are known to be strongly non-linear (depending on temperature, time, process conditions, etc) the materials are characterized. The molding compound is measured time and temperature dependent. For the thin film materials, warpage and indentation measurements performed. The materials are activated during the simulation steps in order to describe the reality as close as possible and predict the correct
stress history. The modeled temperature loading profile follows the manufacturing process. The wafer back-end processes are simplified as one cool down step from 450°C to RT with only the IC materials activated (substrate, interconnect metal layers, dielectric, and passivation). The simulated packaging processes are the molding and curing processes. During these processes no delamination is present (perfect adhesion between all materials). Delamination at the IC/compound interface is included during TCT and the effect of this delamination is predicted in the subsequent TCT processes. The amount of delamination is taken as an input parameter in the simulations, thus initiation and growth is not predicted. In this way, the consequences of realistic and observed delamination are predicted. Further model assumptions and simplifications are the following:

- The stress free state of the materials is set at its process temperatures.
- Intrinsic stresses in the dielectric and passivation layers are taken into account as initial stress state at 450°C.
- J-integral values are calculated in the top layer only for a constant crack length.

Meshing mm Scale and nm Scale in one Model

The ‘glued’ contact option is applied in order to use large elements in the silicon and small elements in thin film structures together in both 2D and 3D models. In the 2D model ‘glued’ contact is applied to mesh the crack tip independently of the rest of the model (see magnification in Figure 6). In the 3D model ‘glued’ contact is applied to allow a fine mesh in the corner metal layout together with a rough mesh in the rest of the model. The ‘glued’ contact option is applied to simulate perfect adhesion in the first processes. Subsequently, in the last TCT processes, ‘touching’ contact is activated for the passivation/compound interface to include delamination.

Results

Delamination is observed in the samples. From all experimental observations, delamination at IC/compound interface is found to be the major trigger for passivation crack and metal shift. Figure 7 shows two identical structures from, but with different amounts of delamination. The difference in delamination is obtained by applying different MSL preconditioning (Moisture Sensitivity Level) to the samples. It can be seen that with delamination (left figure) metal shift is clearly visible and without delamination (right picture) no metal shift can be observed.

The physics behind the mechanism is determined by the simulations and agrees with the experimental observations. Figure 8 shows the predicted failure mechanism where delamination of the IC/compound interface is of major influence on passivation cracking. The effects of various metal layout designs can now be analyzed for its effect on failures with or without the presence of delamination. Because delamination is the key factor causing passivation crack and metal shift, further results are given for delaminated cases only.

Figure 7: Comparison test structure S2 with delamination (left) and without delamination (right)

Figure 8: Compound (brown) pushing against the passivation (red).

Figure 9: Calculated J-values with allowable crack energy from the experimental observations.

By combining the simulation results with experimental observations, roughly a feeling for the allowable J-level of the passivation material is found. Figure 9 shows the predicted J-values for the test structures. Ranking the test structures from worst to best gives the following:

- S2, S1, S3, S4, S5, and S6.

The structures S2, S1, S3, and S4 consistently show failures to a different extent. For instance: structure S2 shows major cracking and metal shifting as can be seen in Figure 7. The structures S5 and S6 show no failures. Therefore, the calculated ranking and experimental ranking agree very well. It is stated that the ranking is done with similar amounts of delamination in the experiments and simulations. It can be
concluded that the simulations are able to predict passivation crack reliably. The simulation results show that the distance from the metal line to IC edge (a) has an important non-linear effect on the crack energy, which explains the ranking. This is visualized by S1 till S6 in Figure 9 having increasing ‘a’ respectively and S2 having the highest crack energy. From studies as discussed in this section we gain knowledge of the effect of IC design (interconnect metallisation placement) and packaging design (die thickness, compound) on reliability. The model can be used to optimize structures IC and package.

Conclusions IC Package Interaction

From the experimental observations and the simulation results it is concluded that delamination is the key trigger for passivation cracking and metal shift. Both in the experiments and from the simulations delamination is found to be the main cause for failures. With delaminated IC package interface, the IC metal layout has a major effect on passivation crack and metal shift. The simulations predicted failures agree with the experiments and show that IC interconnect metal layout can be optimized to prevent failures after packaging.

3. 1st Level interconnect reliability

This section describes an approach for qualitatively assessing wire stitch reliability in a plastic encapsulated package. Figure 10 shows the model containing a wire bonded package (die, die attach, wire, lead frame) solder and PCB (metal tracks, isolator) The developed model allows delaminating the compound/lead frame interface, around the stitch. This is an effective approach to analyzing and reducing the effect of delamination without having to predict the initiation of delamination [3]. To simulate the surrounding delamination around the stitch, a double mesh is applied for the ‘wire mesh’ location. One meshed wire represents the wire stiffness to predict stitch forces correctly and is connected to the compound as the wire was embedded. A 2nd mesh ‘behind’ the wire represents the compound stiffness and is continuously connected with the rest of the compound.

Special prototype samples were assembled and analysed for the amount of delamination. The amount of delamination found in the samples (see Figure 11) was used in the models to analyze the effect of delamination.

Figure 10: 2D parametric model of ½ QFN geometry.

Figure 11: Red areas in this SAM analyses (Scanning Acoustic Microscopy) represent compound/lead frame delamination.

Time- and Temperature-Dependent Material Properties

Time- and temperature-dependent material properties are taken into account in the material models if necessary:

- The silicon die is modeled with isotropic elastic properties [4].
- The moulding compound and die attach are modeled with visco-elastic properties [4]. The PCB is modeled as a visco-elastic orthotropic material.
- The solder material model is an elastic-plastic model without creep.

Figure 12: Pull and shear forces on the stitch.

Loading & results

The summation of forces working on the stitch attached to the lead frame is used to assess the wire loading, see Figure 12. Figure 13 shows the calculated wire loading after different process steps.

- After molding the package is finished (0h product at 25°C) we normalized the force being 1.
- After board assembly, again 25°C, the stitch forces increase with about 55%. The increase is caused by different thermal expansion of the board, which effects the shearing on the delaminated compound/lead frame interface during cooling down.
- During Board Level Reliability testing the wire loading increases again at lower temperatures due to the larger temperature decrease in the cycling test.
The effects of package size is analysed to predict the effects of board assembly for (future) bigger packages. The larger dimensions between solder pads are expected to give a larger force loading (CTE x l) to the package. Whether delamination in a big package will increase stitch forces more compared to a small package is shown in Figure 14. For the smaller package a large effect of delamination of is found after moulding (about a factor 3.5). If delamination occurs during board assembly, stitch forces increase about a factor of 2. Note that all the forces without delamination are normalised being 1. In the bigger package, delamination has a smaller increase because the bigger package bending releases some shearing effect and because the position of the stitch compared to the delamination is more optimal. The difference in shear movement of compound and lead frame is a complex combination of uniform length difference between the 2 materials, package bending, and position & length of delamination.

Figure 14: Wire loading comparison delaminated and non-delaminated compound/lead frame

**Conclusions**

The wire modeling approach obtains following conclusions:

- Delamination at compound/lead frame triggers shearing off the wire stitch.
- The developed model can be used to predict whether design changes can prevent delamination or reduce wire failures when delamination is present.
- Different other design/processes are evaluated for the effect on wire failures, such as package sizes, compound materials, board designs, and lead free solders.

By optimizing package design, board level failures can be reduced.

### 4. 2nd Level interconnect assessment

Traditional (BLR) Board Level Reliability prediction is developed in the early 90’s [5, 6]. It is based on global-local techniques combined with substructures. It has proven to attain an accuracy of approx. 25% deviation between predicted versus measured Mean Time To Failure (MTTF) for PbSn [5] and approx. 50% for Pb-free [6] solders. This deviation is mainly caused by the technique that is used, which limits to the following:

- The geometry of the solders is simplified as block shaped joints. It is known that the shape of the solder ball has an impact on the life time [7].
- Only in the local model, the critical joint has non-linear material behavior. All other materials are linear, time and temperature independent.
- Molding compounds behave strongly time and temperature dependent [8, 4], and this stress history is neglected.

To overcome these above limitation, we propose an updated, innovative approach to simulate BLR, which is described below with a BGA256 carrier product.

Figure 15: FE model for the BGA family containing PCB ( ), solder ( ), substrate ( ), solder mask ( ), IC ( ) and compound ( ).

The 3D parametric model of the BGA is shown in Figure 15. Due to symmetry, only ¼ is modeled. The model has some specific features:

- Parametric model makes it possible to mesh the complete BGA family automatically.
- Shape of critical solder joint determined with surface evolver.
- Non-critical solder joints modeled with beams to minimize the number of elements.
- Contact bodies used to reduce the number of elements by using different mesh sizes.
- Time and temperature material properties to model realistic behavior.

**Parametric Model**

The geometry of the model is completely parametric. All geometrical properties can be changed, like pitch, standoff height, die size, die thickness, etc. and the complete BGA family can be automatically meshed, which allows to calculate the total BGA package family design space and use RMS - DOE techniques to interpolate between the calibrated points.
Shape of Critical Solder Joint

To correctly model the shape of the solder ball, Surface Evolver [9] is used. Surface Evolver is an interactive program for the modeling of liquid surfaces shaped by various forces and constraints. The predicted solder ball shape is compared with measured ball shape from the measurements. The results are listed in Table 1, for the ball diameter; solder height when placed on the BGA; maximum ball width when soldered on the PCB. Generally, the predicted shape is in close correlation with the measured values. The evolver geometry is implemented in the commercially available FE software Marc/Mentat using specially written procedure files: Evolver points and surface mesh are written into ASCII files; these points are read by Marc/Mentat; a 2D mesh is made from the points on Y=0; this mesh is expanded to a 3D mesh by rotation.

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Evolver</th>
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<tbody>
<tr>
<td>Ball diameter</td>
<td>0.76 mm</td>
</tr>
<tr>
<td>Soldered height on BGA</td>
<td>0.625 mm</td>
</tr>
<tr>
<td>Soldered on PCB max. width</td>
<td>0.81 mm</td>
</tr>
</tbody>
</table>

Beam Elements for Non-Critical Solder Joints

Beam elements are used for the non-critical solder balls [10, 11]. Non-linear beams with circular cross section are used, having six dof’s and calculated equivalent Poisson ratio and Young’s modulus. Separate test FE models are used to determine the equivalent solder ball stiffness, see Figure 16. This figure shows two FE models to compare the influence of the beams to the stress / strain response of the critical joint. Figure 16 shows the resulting equivalent strains in the critical joint. This figure clearly shows that there is no significant difference in creep strain response between both FE models.

Contact Bodies

Contact bodies are used to allow for different mesh sizes for the package, PCB, and the critical solder joint. So the number of elements used can be reduced. As such, a very efficient (in terms of low CPU usage) FE modeling procedure is created.

Time- and Temperature-Dependent Material Properties

For all materials, time- and temperature-dependent material properties are used:

- The silicon die with anisotropic properties [4].
- The molding compound, die/attach, FR4 with viscoelastic properties [4]. The PCB is modeled as a viscoelastic orthotropic material.
- The solder material with creep behavior [12], according to:

\[
\dot{\gamma}_{\text{creep}} = \frac{C_{\text{hlit}}}{T_d} \tau^{n_{\text{all}}} e^{-\frac{Q_a}{RT}} + \frac{C_{\text{hlit}}}{T} \tau^{n_{\text{all}}} e^{-\frac{Q_a}{RT}} \quad (1)
\]

With the following parameter settings:

Region | C | n | d_p [m] | Qa [eV]
-------|---|---|---------|---
II | 1.39e-6 | 1.96 | 7.66E-11 | 0.50
III | 2.38e3 | 7.1 | -- | 0.84

Results

The BGA 256 is subjected to two different thermo cycle tests. Figure 17 shows the creep curves of the critical solder ball for the two tests and Figure 18 shows the normalized N50% for the tests and the simulations. A maximum deviation of 15% is found.

![Figure 17: Averaged accumulated inelastic strain in solder ball as function of time. □□ for test 1 and ▲▲ for test 2.](image)
Figure 18: Cycles to failure for experiments (hatched red) and simulations (blue) on TCT and TST. The results are normalized to test 1.

Conclusions

Board Level Reliability prediction is traditionally based on global-local techniques combined with substructures. It has some disadvantages regarding simplification of the geometry and the non-time dependent and non-temperature dependent material properties for most of the used materials. In this section we have demonstrated our new technique for board level reliability prediction, that takes into account the right solder shapes or an equivalent stiffness, it is able to handle non-linear material properties and it is efficient in calculation time due to the use of beam elements and contact bodies. This approach has shown to be efficient and accurate. As a carrier product a BGA 256 was used and it was experimentally and numerically subjected to different tests.

5. Conclusions

This paper showed three examples of reliability assessments on 1st and 2nd level interconnects by combining experiments and simulations. Experiments are needed to develop reliable models. Using the reliable models with an integrated approach for 1st and 2nd level reliability assessment, complete (future) product families can be analyzed during the processing history. Such an integrated modeling approach proves to be an efficient method to prevent reliability problems prior to physical prototyping of real products. This approach is becoming more advantageous with higher technological product complexity and reliability requirements in the overlap areas (Figure 1), especially with products not being developed at one organization at one site.

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References