Temperature Dependence of Hot-Carrier-Induced Degradation in 0.1 μm SOI nMOSFETs With Thin Oxide

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Abstract—This letter investigates hot-carrier-induced degradation on 0.1 μm partially depleted silicon-on-insulator (SOI) nMOSFETs at various ambient temperatures. The thermal impact on device degradation was investigated with respect to body-contact nMOSFETs (BC-SOI) and floating-body SOI nMOSFETs (FB-SOI). Experimental results show that hot-carrier-induced degradation on drive capacity of FB-SOI devices exhibits inverse temperature dependence compared to that of BC-SOI devices. This is attributed to the floating-body effect (FBE) and parasitic bipolar transistor (PBT) effect.

Index Terms—Floating-body effect (FBE), hot-carrier-induced degradation, parasitic bipolar transistor (PBT) effect, partially depleted silicon-on-insulator (SOI).

I. INTRODUCTION

SILICON-ON-INSULATOR (SOI) MOSFETs are attractive since they provide full dielectric isolation and reduced junction capacitance as compared to bulk-Si MOSFET. Partially depleted SOI (PD-SOI) devices, in which threshold voltages are decoupled from silicon film thicknesses [1], are preferable for high-performance applications because of their better scalability and manufacturability. However, the large drop in threshold voltage at high drain biases due to the floating-body effect (FBE) remains a critical issue for PD-SOI device implementation. The body-contact (BC) configuration is one of the most effective and practical methods of suppressing the FBE [2]. However as technology was scaled down to the deep sub-micron regime, SOI MOSFETs also suffer from hot-carrier-effects (HCE). Thus, a study of hot-carrier injection was needed to predict the long-term reliability of devices. The relevant operation regimes for HCE in conventional bulk-Si devices are the maximum substrate current (I_S = I_D/2) and the maximum gate current (I_G = I_D). HCE in SOI devices is more complex than in bulk devices because of the parasitic bipolar transistor effect (PBT) and FBE [3]. Recent studies have shown that operation at higher chip temperature (T = 55–85 °C) naturally ameliorates the FBE [4], and that SOI devices are of interest for high-temperature applications because of the inherent reduction in junction leakage current relative to bulk-Si devices [5]. Some works have studied the high temperature reliability of SOI devices [6] and [7], but there are few studies on the impact of ambient temperature on hot-carrier-induced degradation for 0.1 μm SOI device with thin oxide (~2 nm). In the present study, hot-carrier-induced degradation of 0.1 μm partially depleted SOI nMOSFET performance at various temperatures was investigated with respect to body-contact SOI (BC-SOI) nMOSFETs and floating-body SOI nMOSFETs (FB-SOI).

II. EXPERIMENTS

PD-SOI CMOSFET devices on Implanted OXygen (SIMOX) SOI substrates were fabricated with 190 nm thick Si active layers, 150 nm thick buried oxide (BOX), and 2 nm nitride gate oxides using the 0.1 μm process with composite oxide/SiN spacers and A5+-implanted source/drain junctions. After CoSi2 salicidation, the devices were metalized using a typical backend flow. To investigate the HCE, device stressing and measurements were performed on probe stations using various drain voltages (V_D = 1.2–2.4 V), gate voltages (V_G = 0–2.4 V) and temperatures (25–125 °C) with 100 min stress time. Three repeat measurements on hot-carrier-induced device degradation were performed for each CMOSFET.

III. RESULTS AND DISCUSSION

Fig. 1 shows the temperature dependence of 0.1 μm BC-SOI device saturated drain current (I_Dsat) degradation when stressed by constant drain voltage (V_D = 2.4 V) and various gate stress conditions. T-gate structures [8] were used for the BC-SOI devices with contact terminals placed in the channel-width direction on the source side or the drain side. In 0.1 μm BC-SOI devices at room temperature, maximum hot-carrier-induced I_Dsat degradation (measured at V_D = V_G = 1.2 V) occurred at V_G = V_D = 2.4 V stressing, due to channel hot electrons being confined more closely to the Si surface leading to greater damage to the Si surface at higher V_G [9]. In general, when a transistor is stressed by hot carrier injection, the maximum transconductance (G_mmax) degradation is mainly associated with the trapped charges and the creation of defects at the Si/SiO2 interface [3]. In this work, hot-carrier-induced G_mmax degradation was more significant as gate voltage increase. The reduction of the
device dimensions causing an increase of electric field in the transistors could aggravate the HCE. This high field provides enough energy to the channel carriers and enhances the impact ionization rate, increasing interface defects. However, the literature shows that channel holes are created in thin-oxide nMOSFETs ($t_{ox} < 3\,\text{nm}$) at larger $V_G$ due to valence-band electron tunneling [10]. These generated channel holes provide for recombination with electrons in the channel and transfer their excess energy to other conduction electrons, accelerating hot-electron-tail and interface-trap generation rates, resulting in maximum $I_{D\text{sat}}$ degradation at $V_G = V_D$. When the stress gate voltage larger than $V_D = 24\,\text{V}$, $I_{D\text{sat}}$ degradation will be more serious due presumably to higher valence-band electron tunneling. As ambient temperature was increased, $I_{D\text{sat}}$ degradation was suppressed (especially at $V_G = V_D/2$) due to the occurrence of phonon scattering, reducing channel electron mobility and impact ionization rates. Thus for BC-SOI nMOSFETs at high temperature, maximum $I_{D\text{sat}}$ degradation always occurred when $V_G = V_D$. It is believed that at higher ambient temperatures, generation of many electron–hole pair enhances electron tunneling and increases generated channel hole at higher $V_G$; thus, increased interface states occur resulting in maximum $I_{D\text{sat}}$ degradation.

In $0.1\,\mu\text{m}$ FB-SOI nMOSFETs at room temperature, electron and hole injection occurred at low gate voltages ($V_G\sim V_T$) due to the parasitic bipolar effect (PBT) [3]. Under PBT influence, hot holes are generated by impact ionization, resulting in generation of many interface states. Bipolar injection induces more interface states than pure electron injection; therefore, hot-carrier-induced $I_{D\text{sat}}$ degradation in FB-SOI devices is enhanced, as shown in Fig. 2. Furthermore, the hot-carrier-induced $I_{D\text{sat}}$ degradation at maximum $I_{sub}$ ($V_G = V_D/2$) stress is more serious than that at maximum $I_G$ stress ($V_G = V_D$). It is assumed that holes generated by impact ionization cause FBE, resulting in body–source barrier lowering and allows injection of many electrons into channels and tunneling to gates; thus, fewer channel holes are generated to recombine with channel electrons, reducing hot-carrier-induced interface trap generation rates and suppressing the $I_{D\text{sat}}$ degradation at $V_G = V_D$. When the temperature was elevated ($\sim 125\,\text{°C}$), the FBE becomes less severe due to the weak temperature dependence of body to source bias [8]. This fact might be also due to self-heating effect which makes more phonons available for scattering, shortening the mean free path and affecting ballistic-transport characteristics of the carriers flight across the channel [11]. For FB-SOI device at high temperature, the FBE was not apparent. Thus, maximum $I_{D\text{sat}}$ degradation always occurs at $V_G = V_D$ stressing. Increased interface states occur at high temperature due to electron–hole generation, increasing electron tunneling and generated channel hole, resulting in maximum $I_{D\text{sat}}$ degradation. Owing to the suppression of FBE at high temperature, the hot-carrier-induced $I_{D\text{sat}}$ degradation at $V_G = V_D$ in FB-SOI devices was inversely temperature-dependent compared to BC-SOI devices.

Fig. 3 shows the respective $I_D-V_G$ characteristics of $0.1\,\mu\text{m}$ BC-SOI nMOSFETs before and after stress ($V_G = V_D$) at different ambient temperatures. After 100 min stressing at room temperature, BC-SOI nMOSFETs shows reduced subthreshold behavior and larger gate-induced drain leakage (GIDL) measured at $V_G = 0.6\,\text{V}$. It has been reported that GIDL is a direct result of the generation of interface states; thus, maximum $I_{D\text{sat}}$ degradation corresponds to the maximum increase in interface state [12]. As ambient temperature increased, device subthreshold slopes deteriorated and GIDL increased due to electron–hole generation, which reduced threshold voltage ($V_T$) and increased $I_{D\text{sat}}$ ($I_D(V_D = V_G = 0)$ and off-state.
leakage ($I_{D}(@V_G = 0)$). However, the $I_{D_{sat}}$ was also significantly degraded after hot carrier stressing due to higher valence-band electron tunneling; thus, the total $I_{D_{sat}}$ degradation is the result of reduce-$V_T$-induced $I_{D_{sat}}$ enhancement and hot-carrier-induced $I_{D_{sat}}$ degradation. For FB-SOI nMOSFETs after $V_G = V_D$ stressing at room temperature, device subthreshold slope was deteriorated and substrate-to-drain potentials were also reduced due to FBE; thus, GIDL decreased as gate stress increased, as shown in Fig. 4. With FBE in FB-SOI nMOSFETs, fewer channel holes are generated for recombination with electrons in the channel, resulting in lower interface trap generation rates at $V_G = V_D$; thus, the hot-carrier-induced $I_{D_{sat}}$ degradation is not apparent. However, increasing ambient temperature suppresses FBE, so the $I_{D_{sat}}$ degradation of stressed FB-SOI nMOSFETs at high temperature exhibits worse subthreshold slope and larger GIDL. It is believed that more interface states occur at high temperature, resulting in maximum $I_{D_{sat}}$ degradation at $V_G = V_D$. Therefore, in stressed FB-SOI nMOSFETs, maximum $I_{D_{sat}}$ degradation increases with increasing ambient temperature.

IV. CONCLUSION

This letter analyzes hot-carrier-induced degradation on 0.1 $\mu$m partially depleted SOI nMOSFETs at various temperatures. Interface defects caused by higher valence-band electron tunneling were the major factor on maximum hot-carrier-induced $I_{D_{sat}}$ degradation of BC-SOI nMOSFETs at room temperature when $V_G = V_D$. While on FB-SOI devices, FBE suppressed holes created during valence-band electron tunneling at room temperature, and maximum $I_{D_{sat}}$ degradation occurred when $V_G \sim V_T$ due to PBT. As the temperature was increased, maximum $I_{D_{sat}}$ degradation occurred when $V_G = V_D$ in both SOI nMOSFETs. Owing to FBE, hot-carrier-induced drive capacity degradation of FB-SOI devices exhibited an inverse temperature dependence compared to that of BC-SOI devices.

ACKNOWLEDGMENT

The authors would like to thank the staff members of the TSMC Device Engineering Division for their helpful comments.

REFERENCES