Single-Phase Uninterruptible Power Supply Based on Z-Source Inverter

Zhi Jian Zhou, Xing Zhang, Po Xu, and Weixiang X. Shen, *Member, IEEE*

***Abstract*—This paper presents a new topology of uninterruptible power supply (UPS) by using a Z-source inverter, where a symmetrical LC network is employed to couple the main power circuit of an inverter to a battery bank. With this new topology, the proposed UPS can maintain the desired ac output voltage at the significant voltage drop of the battery bank with high efficiency, low harmonics, fast response, and good steady-state performance in comparison with traditional UPSs. The simulation and experimental results of a 3-kW UPS with the new topology confirm its validity.**

***Index Terms*—Dual loops, shoot-through, uninterruptible power supply (UPS), Z-source inverter.**

I. Introduction

UNINTERRUPTIBLE power supplies (UPSs) are widely used to supply critical loads, such as airline computers and life-support systems in hospitals [1]–[5], providing protection against power failure or anomalies of power-line voltage [6]. In general, there are two types of traditional single-phase UPSs. The first one couples a battery bank to a half- or full-bridge inverter with a low-frequency transformer [7], as shown in Fig. 1(a). In this type of UPSs, the ac output voltage is higher than that of the battery bank; thus, a step-up transformer is required to boost voltage. Due to the presence of the step-up transformer, the inverter current is much higher than the load current, causing high current stress on the switches of the inverter. The transformer also increases the weight, volume, and cost of the system. The second one couples a battery bank to a dc/dc booster with a half- or full-bridge inverter [8], [9], as shown in Fig. 1(b). In this type of UPSs, the additional booster is needed, leading to high cost and low efficiency. The controlling of the switches in the booster also complicates the system. Furthermore, the dead time in the pulsewidth-modulation (PWM) signals to prevent the upper and lower switches at the same phase leg from shooting through has to be provided in the aforementioned two types of UPSs, and it distorts the voltage waveform of the ac output voltage.

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Z. J. Zhou is with Delta Electronics, Shanghai, China (e-mail: bonwe_2001@163.com).

X. Zhang is with the School of Electrical Engineering and Automation, Hefei University of Technology, Hefei, Anhui, China (e-mail: honglf@ustc.edu.cn).

P. Xu is with the Hefei Sungrow Power Supply Company, Hefei, Anhui, China (e-mail: xupo_dldz@163.com).

W. X. Shen is with the School of Engineering, Monash University Malaysia, Bandar Sunway 46150, Malaysia (e-mail: shen.wei.xiang@eng.monash.edu.my).

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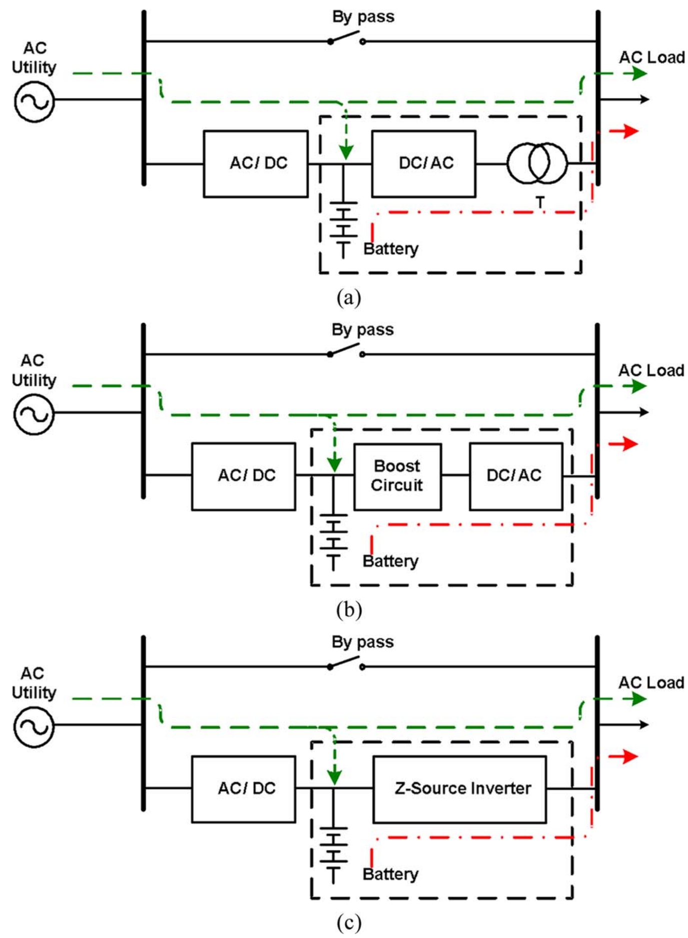


Fig. 1. Topologies of UPS. (a) DC/AC inverter + transformer. (b) DC/DC booster + DC/AC inverter. (c) Z-source inverter.

In this paper, a new topology of the UPS is proposed by using a Z-source inverter [10]–[13]. With this new topology, the proposed UPS offers the following advantages over the traditional UPSs: 1) The dc/dc booster and the inverter have been combined into one single-stage power conversion; 2) the distortion of the ac output-voltage waveform is reduced in the absence of dead time in the PWM signals; and 3) the system has achieved fast transient response and good steady-state performance by adopting dual-loop control [14]–[19].

II. System Configuration and Operating Principle

Fig. 1(c) shows a new topology of the UPS with a Z-source inverter. In the normal operation, the rectifier provides power

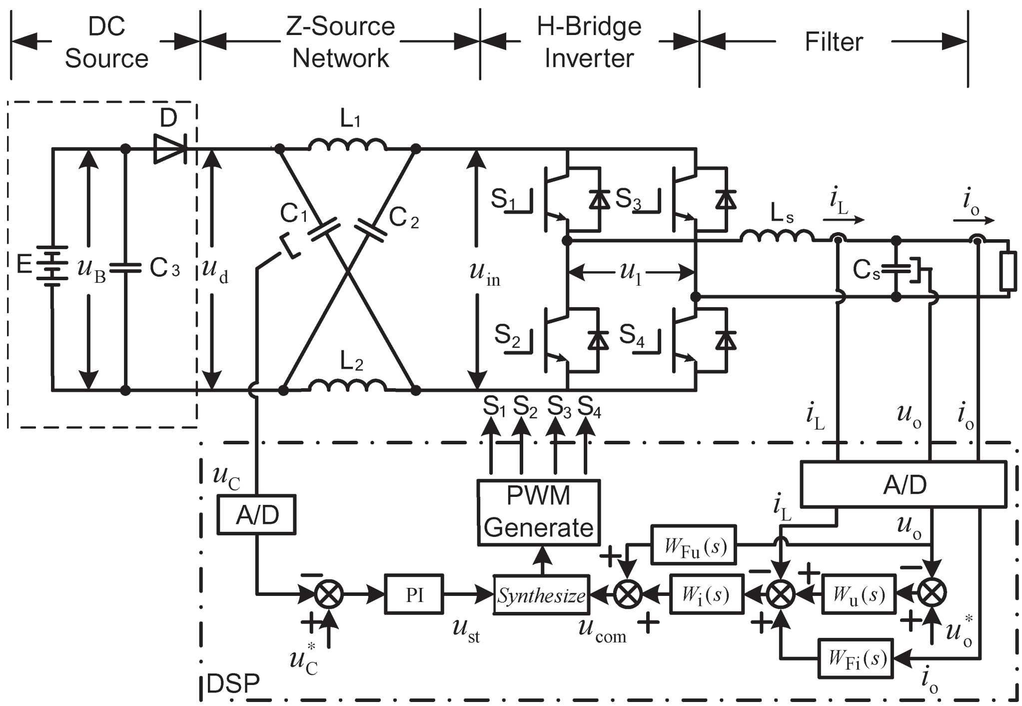


Fig. 2. Z-source inverter for the proposed UPS.

TABLE I
SWITCHING STATES AND VECTOR REPRESENTATIONS OF THE Z-SOURCE INVERTER

Switching States	S_1	S_2	S_3	S_4
Active {1 0}	1	0	0	1
Active {0 1}	0	1	1	0
null {0 0}	0	1	0	1
null {1 1}	1	0	1	0
Shoot through	1	1	0	1
Shoot through	1	1	1	0
Shoot through	0	1	1	1
Shoot through	1	0	1	1
Shoot through	1	1	1	1

to the inverter. In the case of power outage, the battery bank supplies the inverter, as shown in Fig. 2. It consists of a dc source (E, C_3, and D), a Z-source symmetrical network ($L_1 = L_2$ and $C_1 = C_2$), an H-bridge inverter (S_1–S_4), and a filter (L_s and C_s).

Table I shows a total of nine switching states and their vector representations, where the switching function S_x ($x = 1, 2, 3, \text{or } 4$) is defined as 1 when switch S_x turns on and as 0 when switch S_x turns off. Thus, when two active vectors ({1 0}, {0 1}) are taken, the battery bank voltage is applied to the load through two inductances (L_1 and L_2); when two null vectors ({0 0}, {1 1}) are taken, the load terminal is shorted by either the upper or lower two switches; when the shoot-through zero vectors are taken, the load is shorted by the upper and lower switches at the same phase leg. These zero vectors are allowed in the Z-source inverter, whereas they are forbidden in the voltage source inverter. Because of this unique feature of the Z-source inverter, the proposed UPS can generate the desired ac output voltage u_o, regardless of the battery bank voltage u_B, by using the shoot-through zero vectors.

As shown in Fig. 2, the voltage equations of the Z-source inverter [10], [20] can be written as

$$u_{C1} = u_{C2} = u_C \quad u_{L1} = u_{L2} = u_L. \tag{1}$$

When the Z-source inverter is working in nonshoot-through states during time interval T_1, the diode D is on, and the H-bridge inverter can be considered as a current source i_{in}. Consequently, the equivalent circuit of the Z-source inverter at nonshoot-through states is shown in Fig. 3(a), and its voltage equations are

$$u_B = u_d = u_C + u_L \tag{2}$$

$$u_{in} = u_C - u_L. \tag{3}$$

Substituting (2) into (3) yields

$$u_{in} = 2u_C - u_B. \tag{4}$$

When the Z-source inverter is working in shoot-through states during time interval T_0, where $T_0 = T_s - T_1$, and T_s is the switching period, the diode D is off, and the H-bridge inverter can be considered as a short circuit. As a result, the equivalent circuit of the Z-source inverter at shoot-through states is shown in Fig. 3(b), and its voltage equations are

$$u_C = u_L \quad u_{in} = 0. \tag{5}$$

It is recognized that the average voltage of inductor L_1 (or L_2) over one switching period in steady-state operation is zero

$$(u_B - u_C)T_1 + u_C T_0 = 0 \tag{6}$$

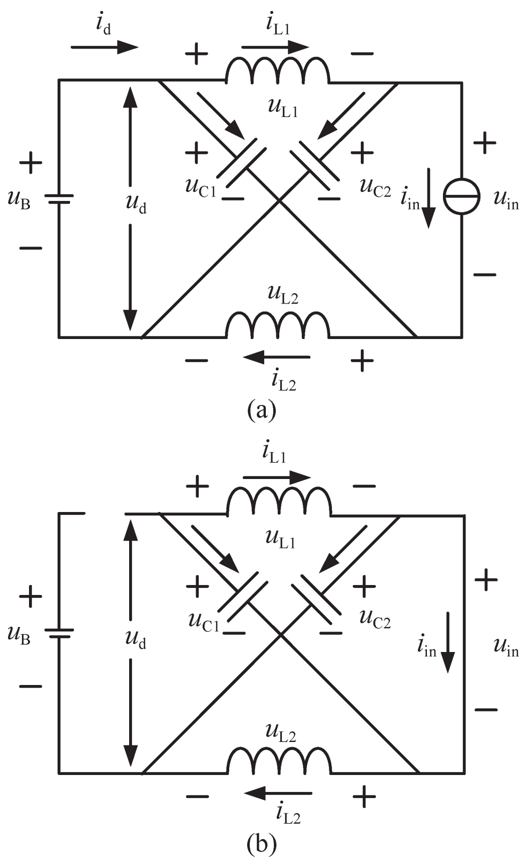


Fig. 3. Equivalent circuit of the Z-source inverter. (a) Nonshoot-through state. (b) Shoot-through state.

or

$$u_C = \frac{T_1}{T_1 - T_0} u_B. \tag{7}$$

Substituting (7) into (4) gives

$$u_{in} = \frac{T_s}{T_1 - T_0} u_B = B u_B \tag{8}$$

where

$$B = \frac{T_s}{T_1 - T_0} > 1 \tag{9}$$

with B being the boost factor. If the voltage across the inductor L_s is ignored, the output peak voltage is

$$u_{om} \approx u_{1m} = m u_{in} = m B u_B \tag{10}$$

where u_{1m} is the peak value of fundamental voltage of the H-bridge inverter and m is modulation index $(m \le 1)$. Thus, the appropriate selection of the booster factor and the modulation index can obtain the desired ac output voltage regardless of the battery bank voltage.

III. Control Principle of the Proposed UPS With the Z-Source Inverter

Fig. 4 shows the dual-loop control in the proposed UPS with the Z-source inverter, namely, the control of inductor current i_L in the inner loop and output voltage u_o in the outer loop [21]–[25], where $K_{PWM}/(sT_s + 1)$ is the transfer function of the H-bridge inverter and K_{PWM} is the average voltage gain viewed from dc link which can be expressed by

$$K_{PWM} = \frac{1 - \frac{T_0}{T_s}}{1 - \frac{2T_0}{T_s}} u_B = \frac{1 - d}{1 - 2d} u_B \tag{11}$$

where $d = T_0/T_s$ is the shoot-through duty ratio [10]. Due to high system switching frequency $f_s (f_s = 1/T_s)$, the capacitor voltage of the Z-source inverter is considered constant in one switching period, which is equal to the average input voltage of the Z-source network u_d, and thus, the gain K_{PWM} is constant as well.

A. Current Inner Loop

In Fig. 4, the output voltage u_o is regarded as a disturbance to the current inner loop.

To smooth the output voltage, a voltage feedforward control is adopted

$$u_o W_{Fu}(s) \cdot \frac{(1 - d) u_B}{(1 - 2d)(sT_s + 1)} - u_o = 0 \tag{12}$$

where $W_{Fu}(s)$ is the transfer function of the voltage feedforward controller. As the bandwidth of the inner loop (f_i) is designed to be much lower than the system switching frequency, namely, $|sT_s|_{s=j\omega_i} \ll 1$, $W_{Fu}(s)$ can be found from (12) as

$$W_{Fu}(s) \approx \frac{1 - 2d}{(1 - d) u_B}. \tag{13}$$

On the other hand, the voltage across the inductor L_s can be written as

$$u_{L_s} = u_1 - u_o = u_{com} \frac{(1 - d) u_B}{(1 - 2d)(sT_s + 1)} - u_o \tag{14}$$

where u_{com} is the PWM vectors. According to (13) and (14), the block diagram of the inner loop can be reduced to Fig. 5, and its open-loop transfer function is

$$W_{oi}(s) = W_i(s) \frac{(1 - d) u_B}{s(1 - 2d)(sT_s + 1) L_s} \tag{15}$$

where $W_i(s)$ is the transfer function of the inner loop controller. $W_i(s)$ is chosen as the constant value to make $W_{oi}(s)$ as a type-1 system which has good tracking capability [26]

$$W_i(s) = K_i \tag{16}$$

where K_i is the gain of the proportion controller. Furthermore, the underdamped state is designed for this two-order inner

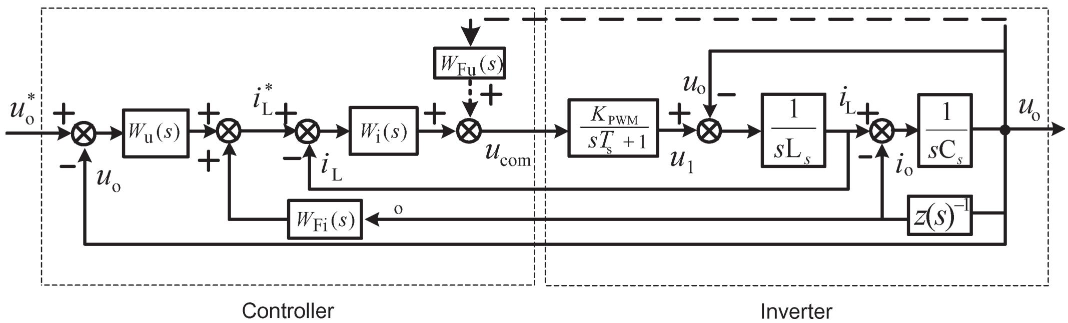


Fig. 4. Control system of the Z-source inverter for the proposed UPS.

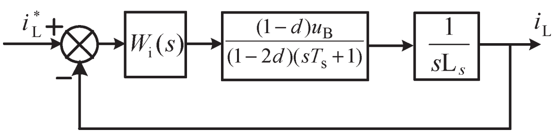


Fig. 5. Block diagram of the inner loop.

TABLE II
PARAMETERS OF THE SIMULATION MODEL

u_o^* (V)	L_S (mH)	C_s (μF)	K_i	K_1	τ_1	d	K_{PWM}	f_s (KHz)
220	1.5	5	0.029	0.013	0.0012	0.12	350	10

TABLE III
STEP RESPONSE OF THE INNER LOOP

K_i	ζ_i	f_{ni} (Hz)	t_s (ms)	σ_i	t_r (ms)	γ_i
0.0429	0.5	1590	0.81	16.3%	0.16	51.8°
0.0296	0.6	1320	0.71	9.3%	0.22	59.3°

loop system to achieve fast response. The tradeoff between the generation of high-order harmonics and the tracking speed of the reference current is made to choose the bandwidth of the inner loop (f_i). From the practical engineering point of view, it can be approximately selected as the natural frequency of the inner loop (f_{ni}) in the range of $10f_0$ to $f_s/5$. The parameters for step response, namely, settle time $(t_s) > 2$ ms, current overshoot $(\sigma_i) < 10\%$, and rise time $(t_r) > 0.3$ ms, are suggested as the criteria to evaluate the tracking performance of the inner loop [26]. Tables II and III show the parameters in the simulation model and the step response of the inner loop, respectively, where ζ_i is the damping ratio and γ_i is the phase margin. It can be seen that the step response of the inner loop meets the criteria when the gain of the proportion controller is 0.0296.

B. Output-Voltage Outer Loop

In Fig. 6, the control of the outer voltage loop has taken the inner current loop into account, where $z(s)$ is an equivalent output impedance. Consider that the current feedforward control of the inner loop has eliminated the load current disturbance

$$i_o W_{Fi}(s) W_{ci}(s) - i_o = 0 \tag{17}$$

where i_o is the load current, $W_{Fi}(s)$ is the transfer function of the current feedforward controller, $W_{ci}(s)$ is the closed-loop

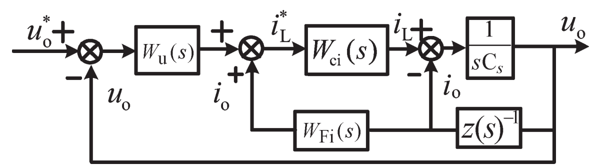


Fig. 6. Block diagram of the outer loop.

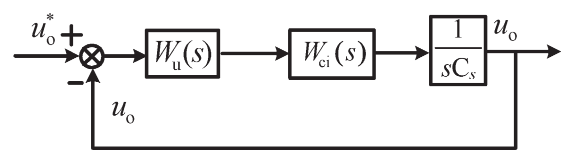


Fig. 7. Simplified block diagram of the outer loop.

transfer function of the inner loop. Because the bandwidth of the outer loop is designed to be much lower than that of the inner loop, the inner loop has faster tracking capability than the outer loop. As a result, the current gain $W_{ci}(s)$ of the inner loop can be approximately equal to one

$$W_{ci}(s) \approx 1. \tag{18}$$

Substituting (18) into (17) and solving (17) yield

$$W_{Fi}(s) \approx 1. \tag{19}$$

From (18) and (19), the block diagram of the outer voltage loop can be simplified to Fig. 7, and its open-loop transfer function is

$$W_{ou}(s) = W_u(s) W_{ci}(s) \frac{1}{sC_s} \tag{20}$$

where $W_u(s)$ is the transfer function of the outer loop controller.

The proportional–integral (PI) controller is adopted to control the outer loop. Substituting (15) and (18) into (20) gives

$$W_{ou}(s) = K_1 \left(\frac{\tau_1 s + 1}{\tau_1 s}\right) \frac{K}{T_s} \frac{1}{\left(s^2 + \frac{s}{T_s} + \frac{K}{T_s}\right) sC_s} \tag{21}$$

where $K = (1-d)K_i u_B/(1-2d)L_s$, and τ_1 and K_1 are the proportional and integral coefficients, respectively. Equation (21) shows that the outer loop is a high-order system. As the bandwidth of the voltage loop (f_u) is much lower

TABLE IV
STEP RESPONSE OF THE OUTER LOOP

K_1	τ_1	ζ_u	f_{nu} (Hz)	t_s (ms)	σ_u	t_r (ms)
0.013	0.0012	0.9	440	3.05	26.6%	0.449

TABLE V
SPECIFICATIONS OF A 3-kW UPS WITH THE Z-SOURCE INVERTER

u_B	u_o	C_1 (C_2)	C_3	L_1 (L_2)	L_S	C_s
360V	220V	1500 μF	1000 μF	2mH	1.5mH	5 μF

than the system switching frequency, namely, $|s^2|_{s=j\omega_u} \ll |s/T_s|_{s=j\omega_u}$, (21) can be simplified to

$$W_{ou}(s) \approx K_1 \left(\frac{\tau_1 s + 1}{\tau_1 s}\right) \frac{K}{s(s+K)C_s}. \tag{22}$$

From the practical engineering point of view, the bandwidth of the outer loop f_u is chosen to be in the range of $(1/5–1/3)f_i$, and similarly, the natural frequency of the outer loop f_{nu} is chosen to be $f_{ni}/3$. In addition, the damping ratio of the outer loop ζ_u is set to 0.9. Table IV summarizes the step response of the outer loop, where σ_u is the voltage overshoot.

C. Shoot-Through Zero-Vector Control

As mentioned earlier, the shoot-through zero vectors are allowed in the Z-source inverter. These zero vectors can be controlled to boost the capacitor voltage in the Z-source network, maintaining the desired level of the average input voltage of the Z-source inverter. As shown in Fig. 2, when the battery bank voltage drops significantly under heavy load, the capacitor voltage of the Z-source inverter drops significantly as well; thus, the voltage difference between the reference u_C^* and the actual capacitor voltage u_C is sent to the PI controller which generates the shoot-through zero vectors [27]. The PWM signals with the synthesis of the shoot-through zero vectors u_{st}'s and the PWM vectors u_{com}'s [20] control the Z-source inverter to achieve the desired ac output voltage u_o.

IV. SIMULATION AND EXPERIMENTAL RESULTS

The simulation model and the experimental setup of a 3-kW UPS with the Z-source inverter have been developed to confirm its validity. The technical specifications of the proposed UPS are shown in Table V, where the battery has the normal voltage of 12 V and the normal capacity of 12 A · h. Thirty batteries are connected in series in the proposed UPS, so the normal voltage of the battery bank is 360 V. Both the simulation and the experimentation have been carried out. The results are shown hereafter.

A. Simulation Results

Fig. 8(a) and (b) shows the output voltages and currents, respectively, of the proposed UPS with the Z-source inverter when both pure resistive and nonlinear loads are suddenly applied. In the steady state, the total harmonic distortion (THD) of the output voltage is less than 1% under the pure resistive load, whereas the THD of the output voltage is less than 3% under the nonlinear load. Fig. 9(a) and (b) shows the output voltages for both the traditional UPS with the voltage source inverter and the proposed UPS with the Z-source inverter, respectively, when the battery bank voltage declines by 20% of its normal voltage. The waveform distortion can be observed for the traditional UPS, whereas the sinusoidal waveform can be kept for the proposed UPS. Fig. 9(c) further shows the strong regulation capability of the proposed UPS at the voltage drop of 50%. It should be noted that the capacitor voltage of the Z-source inverter can be much higher than the battery bank voltage by controlling the shoot-through zero vectors, as shown in Fig. 9(b) and (c).

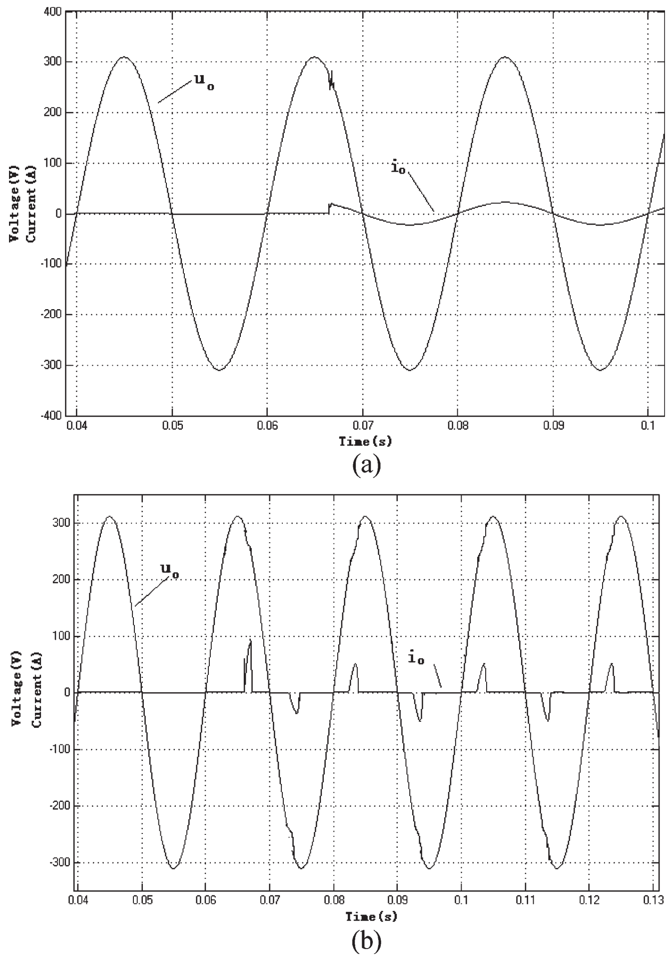
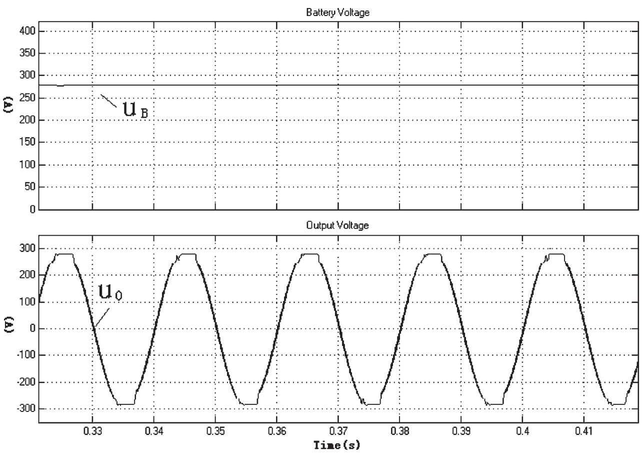


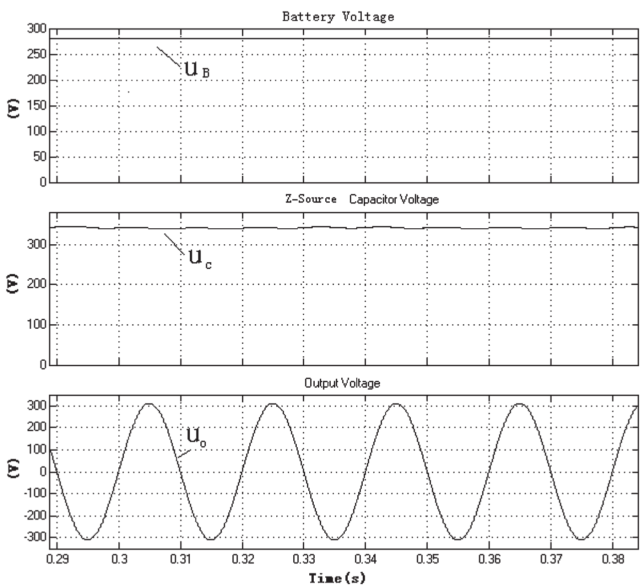
Fig. 8. Simulation results of the proposed UPS. (a) Pure resistive load. (b) Nonlinear load.

B. Experimental Results

Fig. 10(a) and (b) shows the output voltages and currents, respectively, of the proposed UPS with the Z-source inverter under both pure resistive and nonlinear loads. In the steady state, the THD of the output voltage is less than 2% for the pure resistive load, whereas the THD of the output voltage is less than 4% for the nonlinear load.



(a)



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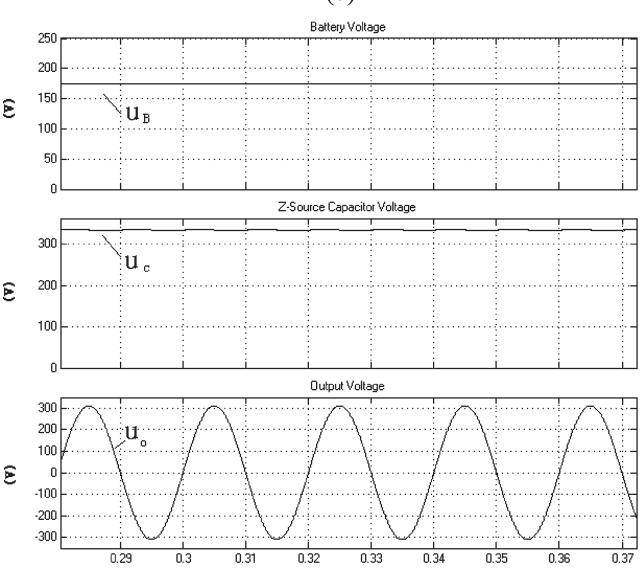
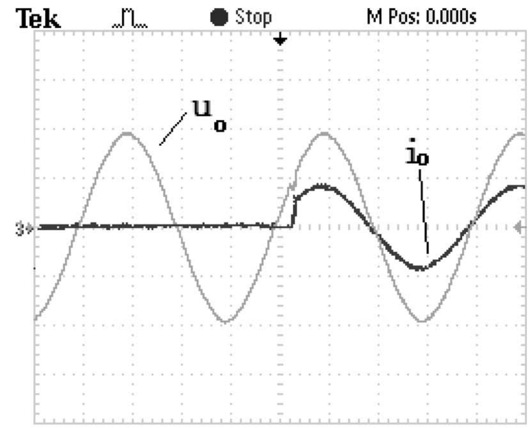


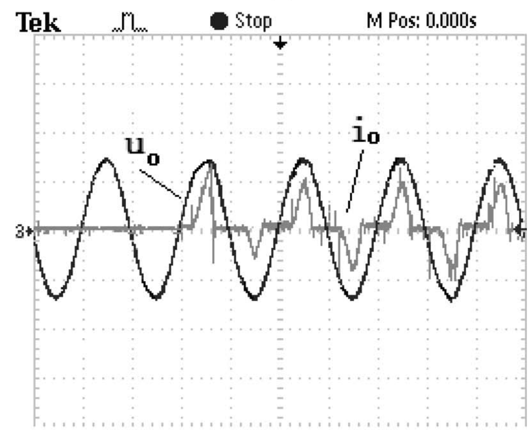
(c)

Fig. 9. Simulation results. (a) Traditional UPS when the battery bank voltage declines by 20%. (b) Proposed UPS when the battery bank voltage declines by 20%. (c) Proposed UPS when the battery bank voltage declines by 50%.



(u_o : 150V/div, i_L : 15A/div, time: 5ms/div)

(a)



(u_o : 200V/div, i_L : 15A/div, time: 10ms/div)

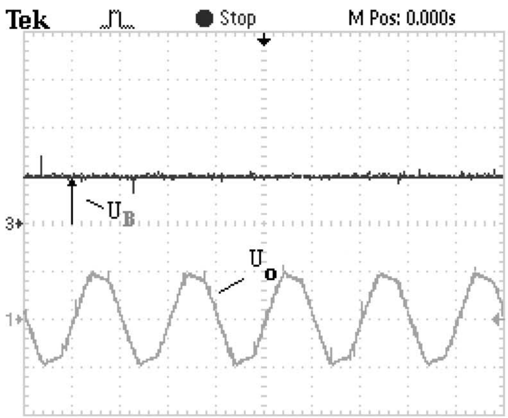
(b)

Fig. 10. Experimental results of the proposed UPS. (a) Pure resistive load. (b) Nonlinear load.

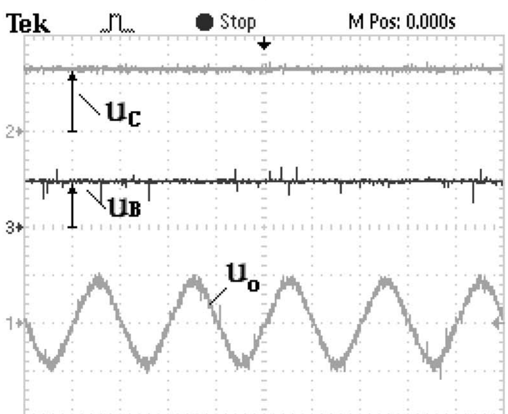
Fig. 11(a) and (b) shows the output voltages for both traditional and proposed UPSs, respectively, when the battery bank voltage sags by 20% of the rated voltage. Similar to the simulation results, the waveform distortion is obvious for the tradition UPS, whereas the sinusoidal waveform can be maintained for the proposed UPS. Fig. 11(c) further shows the strong regulation capability of the proposed UPS at the voltage drop of 50%. It can be observed that the capacity voltage of the Z-source inverter can be much higher than the battery bank voltage by controlling the shoot-through zero vectors in Fig. 11(b) and (c). The efficiencies between the proposed UPS with the Z-source inverter and the traditional UPS with the dc/dc booster and the voltage source inverter in Fig. 1(b) have been compared in Fig. 12. The proposed UPS is more efficient than the traditional UPS.

V. Conclusion

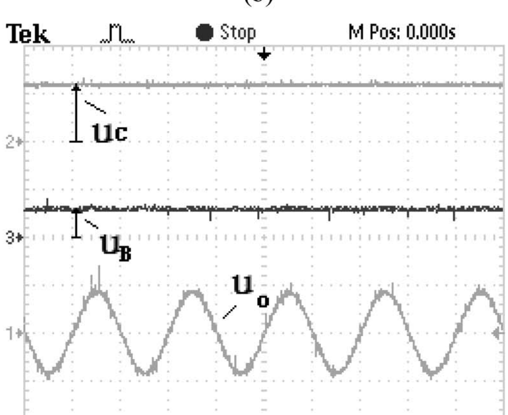
In this paper, a new topology of the UPS with the Z-source inverter has been presented. Compared with traditional UPSs, the proposed UPS shows the strong regulation capability to maintain the desired ac output voltage at 50% voltage sag of the battery bank with high efficiency, low harmonics, fast response,



(a)



(b)



(c)

Fig. 11. Experimental results. (a) Traditional UPS when the battery bank voltage declines by 20%. (b) Proposed UPS when the battery bank voltage declines by 20%. (c) Proposed UPS when the battery bank voltage declines by 50% (u_C: 300 V/div, u_B: 300 V/div, u_o: 300 V/div, and time: 10 ms/div).

and good steady-state performance. All these advantages were verified by simulation and experimental results of a 3-kW UPS with the new topology.

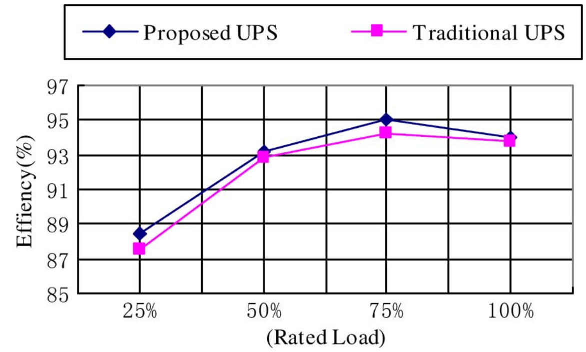


Fig. 12. Comparison of efficiencies between proposed and traditional UPSs.

REFERENCES

[1] R. Krishnan and S. Srinivasan, "Topologies for uninterruptible power supplies," in *Proc. IEEE Int. Symp. Ind. Electron.*, Budapest, Hungary, 1993, pp. 122–127.

[2] M. S. Racine, J. D. Parham, and M. H. Rashid, "An overview of uninterruptible power supplies," in *Proc. 37th Annu. North Amer. Power Symp.*, Oct. 23–25, 2005, pp. 159–164.

[3] H. Pinheiro and P. Jain, "Comparison of UPS topologies based on high frequency transformers for powering the emerging hybrid fiber–coaxial networks," in *Proc. 21st Int. Telecommun. Energy Conf.*, Copenhagen, Denmark, 1999, pp. 2–11.

[4] J. M. Guerrero, L. Garcia de Vicuna, J. Matas, M. Castilla, and J. Miret, "Output impedance design of parallel-connected UPS inverters with wireless load-sharing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1126–1135, Aug. 2005.

[5] A. Fernandez, J. Sebastian, M. M. Hernando, J. A. Martin-Ramos, and J. Corral, "Multiple output AC/DC converter with an internal DC UPS," *IEEE Trans. Ind. Electron.*, vol. 53, no. 1, pp. 296–304, Feb. 2006.

[6] J. M. Guerrero, L. Garcia de Vicuna, and J. Uceda, "Uninterruptible power supply systems provide protection," *IEEE Ind. Electron. Mag.*, vol. 1, no. 1, pp. 28–38, Spring 2007.

[7] P. K. Jain, J. R. Espinoza, and H. Jin, "Performance of a single-stage UPS system for single-phase trapezoidal-shaped AC-voltage supplies," *IEEE Trans. Power Electron.*, vol. 13, no. 5, pp. 912–923, Sep. 1998.

[8] C. G. C. Brancol, C. M. T. Cruz, R. P. Torrico-Bascope, F. L. M. Antunes, and L. H. S. C. Barreto, "A transformerless single phase on-line UPS with 110V/220V input output voltage," in *Proc. 21st Annu. IEEE Conf. Expo. Appl. Power Electron.*, Mar. 19–23, 2006, pp. 348–354.

[9] C.-H. Lai and Y.-Y. Tzou, "DSP-embedded UPS controller for high-performance single-phase on-line UPS systems," in *Proc. 28th IEEE Annu. Conf. Ind. Electron. Soc.*, Nov. 5–8, 2002, vol. 1, pp. 268–273.

[10] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar./Apr. 2003.

[11] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of traditional inverters and Z-source inverter," in *Proc. IEEE 36th Power Electron. Spec. Conf.*, Sep. 11–14, 2005, pp. 1692–1698.

[12] F. Z. Peng, X. M. Yuan, X. P. Fang, and Z. M. Qian, "Z-source inverter for adjustable speed drives," *IEEE Power Electron Lett.*, vol. 1, no. 2, pp. 33–35, Jun. 2003.

[13] K. Holland, M. Shen, and F. Z. Peng, "Z-source inverter control for traction drive of fuel cell–battery hybrid vehicles," in *Proc. 40th Annu. Meeting Ind. Appl.*, Oct. 2–6, 2005, vol. 3, pp. 1651–1656.

[14] A. Kawamura, R. Chuarayapratip, and T. Haneysoshi, "Deadbeat control of PWM inverter with modified pulse patterns for uninterruptible power supply," *IEEE Trans. Ind. Electron.*, vol. 35, no. 2, pp. 295–300, May 1988.

[15] M. J. Ryan, W. E. Brumsickle, and R. D. Lorenz, "Control topology options for single-phase UPS inverters," *IEEE Trans. Ind. Appl.*, vol. 33, no. 2, pp. 493–501, Mar./Apr. 1997.

[16] P. Mattavelli, "An improved deadbeat control for UPS using disturbance observers," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 206–212, Feb. 2005.

[17] A. Von Jouanne, P. N. Enjeti, and D. J. Lucas, "DSP control of high power UPS systems feeding nonlinear loads," *IEEE Trans. Ind. Electron.*, vol. 43, no. 1, pp. 121–125, Feb. 1996.

[18] C. J. Gajanayake, D. M. Vilathgamuwa, and P. C. Loh, "Development of a comprehensive model and a multiloop controller for Z-source inverter DG systems," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2352–2359, Aug. 2007.

[19] G. Escobar, A. A. Valdez, J. Leyva-Ramos, and P. Mattavelli, "Repetitive-based controller for a UPS inverter to compensate unbalance and harmonic distortion," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 504–510, Feb. 2007.

[20] P. C. Loh, D. M. Vilathgamuwa, Y. S. Lai, G. T. Chua, and Y. W. Li, "Pulse-width modulation of Z-source inverters," in *Conf. Rec. 39th IEEE IAS Annu. Meeting*, Oct. 3–7, 2004, vol. 1, pp. 148–155.

[21] C. J. Gajanayake, D. M. Vilathgamuwa, and P. C. Loh, “Modeling and design of multi-loop closed loop controller for Z-source inverter for distributed generation,” in *Proc. IEEE 37th Power Electron. Spec. Conf.*, Jun. 2006, pp. 1353–1359.

[22] T.-Q. Vinh, T.-W. Chun, J.-R. Ahn, and H.-H. Lee, “Algorithms for controlling both the DC boost and AC output voltage of Z-source inverter,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2745–2750, Aug. 2007.

[23] N. Abdel-Rahim and J. E. Quaicoe, “Analysis and design of a multiple feedback loop control strategy for single-phase voltage-source UPS inverters,” *IEEE Trans. Power Electron.*, vol. 11, no. 4, pp. 532–541, Jul. 1996.

[24] R. Parikh and R. Krishnan, “Modeling, simulation and analysis of an uninterruptible power supply,” in *Proc. 20th Int. Conf. Ind. Electron., Control Instrum.*, Sep. 5–9, 1994, vol. 1, pp. 485–490.

[25] A. Moriyama, I. Ando, and I. Takahashi, “Sinusoidal voltage control of a single phase uninterruptible power supply by a high gain PI circuit,” in *Proc. 24th Annu. Conf. IEEE Ind. Electron. Soc.*, Aug. 31–Sep. 4, 1998, vol. 1, pp. 574–579.

[26] C. K. Benjamin and G. Farid, *Automatic Control System*, 8th ed. New York: Wiley, Dec. 2003.

[27] P. C. Loh, D. M. Vilathgamuwa, C. J. Gajanayake, Y. R. Lim, and C. W. Teo, “Transient modeling and analysis of pulse-width modulated Z-source inverter,” in *Conf. Rec. 40th IEEE IAS Annu. Meeting*, Oct. 2–6, 2005, vol. 4, pp. 2782–2789.

Zhi Jian Zhou received the B.E. and M.E. degrees in power electronics from Hefei University of Technology, Hefei, China, in 2004 and 2007, respectively.

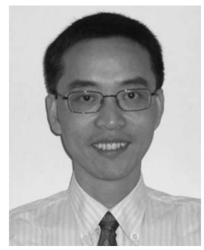
He joined Delta Electronics, Shanghai, China, in 2007, and has been an Electronics Engineer since then. His research interests include UPS systems, renewable energy technology, and power electronics.

Xing Zhang received the B.Sc. (Eng.), M.Sc. (Eng.), and Ph.D. degrees from Hefei University of Technology, Hefei, China, in 1984, 1990, and 2003, respectively.

Since 1984, he has been with the School of Electrical Engineering and Automation, Hefei University of Technology, where, since 2004, he has been a Professor. His research interests include renewable energy applications, power electronics, and automation systems.

Po Xu received the B.Eng. degree in power systems and the Ph.D. degree in power electronics from Hefei University of Technology, Hefei, China, in 2001 and 2006, respectively.

He is currently with Hefei Sungrow Power Supply Company, Ltd., Hefei. His research interests include control strategy techniques on grid-connected inverters and their applications in renewable energy systems.



Weixiang X. Shen (S’00–M’02) received the B.Eng. degree in electrical engineering from Anhui Institute of Mechanical and Electrical Engineering, Wuhu, China, in 1985, the M.Eng. degree in automatic control from Shanghai Jiaotong University, Shanghai, China, in 1990, and the Ph.D. degree in electrical engineering from The University of Hong Kong, Hong Kong, in 2002.

He was with the Department of Electrical Engineering, Hefei University of Technology, Hefei, China, in 1990, and was an Associate Professor from 1995 to 1998. He was also a Visiting Scholar with the University of Stuttgart, Stuttgart, Germany, from 1993 to 1994, and a Lecturer with Ngee Ann Polytechnic, Singapore, from 2002 to 2003. Currently, he is a Senior Lecturer with Monash University Malaysia, Bandar Sunway, Malaysia. His research interests include renewable energy technology, battery modeling and charging technology, power electronics, and power system.