COMMUNICATION

Multibit Storage of Organic Thin-Film Field-Effect Transistors

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The logic circuit and the memory circuit are the basic cells in normal electronic products. All the developments of these cells are driven by the market requirement for low cost. For the memory cells, the traditional way of achieving low cost per bit is by scaling size or multilevel storage, and great developments have been achieved in these areas.[1–4] The multibit storage is more and more attracting research attention due to the scaling method limited by photolithography.[1] The future goal of the memory cell is to obtain multibit information from a small cell by generating 2^n threshold-voltage (V_{th}) levels for n bits per cell.[2]

Comparing with inorganic fields, the memory devices based on organic materials have also been greatly developed in many types, such as organic bistable devices,[5] organic–inorganic hybrid ones,[6] and organic thin-film field-effect transistors (OTFTs) with memory effect.[7–12] Among these memory types, the OTFTs with memory effect attracted most attention due to their light weight, flexibility, applicability to large-area devices, bis-functionality, and lower cost.[12–15] Several methods have been developed in OTFTs to realize the memory effect, such as using ferroelectric fluoropolymers[7] or appropriate polymeric-gate electret layers (such as polyvinylacohol (PVA),[10] poly(α-methylstyrene) (PαMS),[12] etc.). In spite of a few methods that have been used to obtain memory effect in OTFTs, most work was focused on the one-bit storage (with 0, or 1 state). As yet, there are no reports published on multibit storage, and the performing program of the multibit storage has not been reported in OTFTs. Therefore, achieving multibit storage is still a great challenge, and will have a great effect on multifunctional OTFTs applications. Furthermore, the details of the operation mechanism are not well understood, although they are very important for achieving high-performance OTFTs with multibit storage ability.

In this communication we introduce the multibit-storage concept in OTFTs, and show a possible way to realize it in a single OTFT. A top-contact OTFT was built on a SiO_2/Si platform. The source (S) and drain (D) electrodes were produced by high-vacuum evaporation of Au. The organic semiconductor pentacene (or copper phthalocyaine (CuPc)) was used as the active layer, and deposited on the polystyrene (PS, or polymethylmethacrylate (PMMA))-modified SiO_2 dielectric layer (see Fig. 1a). The output and transfer characteristics of the pentacene-based OFETs with PS-modified SiO_2 layer are shown in Figure 1b and c, respectively. The devices with the additional PS layer showed a good p-type OFET behavior, with a mobility of $0.52\,cm^2\,V^{-1}\,s^{-1}$, a threshold voltage of −20 V, and an on/off ratio of 10^6.

The choosing of materials is also crucial for multifunctional devices, since they have to be at least bifunctional ones. Among a variety of organic semiconductors, pentacene (or CuPc) is a promising material for various optical and electrical applications, and has been the focus of active research.[16a,b] Unfortunately, only little work has been published on such organic thin-film phototransistors used in data storage.[16c] It is well known that optical materials can generate excitons by light emission. For OTFTs, the photo-generated excitons can be separated by applying appropriate gate voltage to generate holes and electrons. Therefore, we use a thin common-polymer layer to modify the SiO_2 surface as high-energy-electrons tunneling layer (or hot-electrons injecting layer) and the barrier layer to hold the low-energy electrons tunneling back. Figure 2a shows the transfer curves for the pentacene-based OTFTs with the PS-modified SiO_2 dielectric layer under visible-light illumination of $1\,mW\,cm^{-2}$ (visible-light spectroscopy, see Supporting Information, Fig. S1). The maximum drain current, V_{th} value, and magnitude of the field-effect onset voltage (V_{onset}) are strongly related to the starting value of the sweeping gate voltage ($V_{GS,Start}$). The entire transfer curve was substantially shifted in the positive direction when a positive $V_{GS,Start}$ increases from 20 V to 80 V. As a result, the V_{th} and V_{onset} were changed by more than about 55 V. A series of changes in V_{onset} were observed with increasing the magnitude of $V_{GS,\,Start}$ (see Fig. S2a, Supporting Information). The corresponding current-levels variation at $V_{GS} = 0$ V, $V_{DS} = -60$ V, was shown in Figure 2b during the positive process. When the visible light is turned off after scanning gate voltage under light illumination, the transfer curve steadily sustained at the shifted position sweeps without illumination during subsequent V_{GS}.

Moreover, we can obtain another 7 V_{th} levels just by using the gate-voltage program of $V_{GS,Pro} = -50$ V, −70 V, −100 V, −120 V, −150 V, −170 V, −200 V, $V_{DS} = 0$ V and $t = 1\,\mu s$ (see Fig. 3a and b). The corresponding log plot of I_{DS} versus V_{GS} is shown in Figure S2b of the Supporting Information. The V_{th} shift shows a linear tendency in Figure 3b, which is different from previously reported results.[12,17] The corresponding current levels variation

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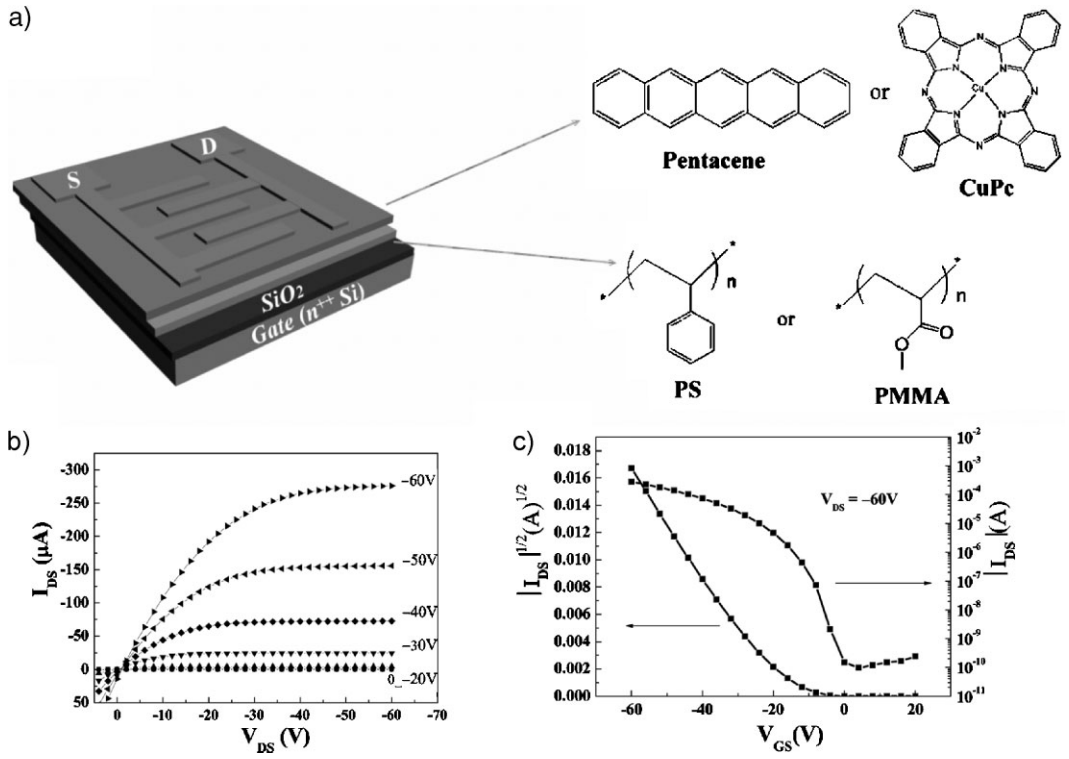

Figure 1. a) Cross-sectional view of the device presented in this study and molecular structures of pentacene, CuPc, PS, and PMMA. b) Output and c) transfer characteristics of the pentacene-based OTFTs with the PS-modified SiO_2 dielectric layer.

at $V_{GS} = 0$ V, $V_{DS} = -60$ V, and $V_{GS} = -50$ V, $V_{DS} = -60$ V are shown in Figure 3c during the negative process. Meanwhile, the stored holes can still be erased by the light-assisted program (see Figs. 3d and S2c, Supporting Information), and the corresponding log plot of I_{DS} versus V_{GS} is shown in Figure S2d of the Supporting Information. It is clear that some of the stored holes are very sensitive to the visible light. Similar phenomena were also seen in the devices based on CuPc with PS-modifying layers (see Supporting Information Fig. S3). The OTFTs with PMMA show almost the same electric properties for both pentacene- and CuPc-based devices (see Supporting Information Figs. S4 and S5). However, it is interesting to note that the holes stored in pentacene and CuPc OTFTs with PMMA show a higher resistance in visible light than PS (see Supporting Information Figs. S4 and S5). The devices show high performance (pentacene: $\mu > 0.5\,cm^2\,V^{-1}\,s^{-1}$, $I_{on}/I_{off} > 10^6$; CuPc: $\mu > 0.01\,cm^2\,V^{-1}\,s^{-1}$, $I_{on}/I_{off} > 10^4$) at room temperature and a series of V_{th} shifts in a large scale (over 100 V). The detailed performance of the OTFTs with different semiconductor and polymer layers are shown in Table S1 (see Supporting Information). All the phenomena demonstrated that our program is a feasible way to achieve multilevel V_{th} with single OTFTs, which is the precondition of realizing multibit storage in a single cell. However, the voltage program of $V_{GS,Pro} = 200$ V, $V_{DS} = 0$ V, t = 1 μs has little effect on the transfer-curve state with the PS- or PMMA-modified cells in our experiment. It is to say that the barrier for electron injection is too high to surmount just by voltage effect in our devices, a result similar to that previously reported for PS-modified devices.[12] Interestingly, we found another way to obtain positive V_{th} shifts. When we use a program with top-light irradiation and large positive gate-voltage pulses in a longer time (~1 ms), the devices can also reach positive V_{th} shifts. Meanwhile, the *I–V* characteristics of the devices based on pentacene with no modifying layers are shown in Figure S6 of the Supporting Information. It is clear that V_{th} assumes relatively smaller shifts, from −12.7 V to 7.1 V, than the polymer-modified ones when the light program was performed. Moreover, the voltage program ($V_{GS} = -150$ V, −200 V, $V_{DS} = 0$ V and $t = 1$ μs) had little effect on V_{th} and V_{on} shifts, indicating that the trapped electrons cannot be released due to the high carrier barrier of SiO_2 under that condition. Therefore, the polymer layer plays an important role in the memory effect.

To realize multibit storage, control over different V_{th} levels, long retention time, and certain on/off current ratios are needed.[12,17] For practical applications of memory devices, the retention times of ON and OFF current states are very important. Four states of the retention characteristics of the OTFTs based on PS are shown in Figure 4. The current was measured at $V_{DS} = -60$ V and $V_{GS} = 0$ V using a light-assisted program (start scanning $V_{GS,start} = 40$ V, 60 V, 80 V, $V_{DS} = -60$ V (ON state)), and $V_{GS,Pro} = -150$ V, $V_{DS} = 0$ V, $t = 1$ μs (OFF state) without light. The retention time is defined to be in the ON-state current until the device current reaches 50% of the initial value. The retention time was therefore estimated from the measured data to be more than 250 h, one of the best results in OTFTs with memory effect at room temperature (20 °C). It is well known that the temperature has an important effect on the signal stage for inorganic memory devices. In order to investigate the temperature effect on the organic memory devices, we measure another three different retention times, at 40 °C, 50 °C, and 60 °C (a LTS hot stage was

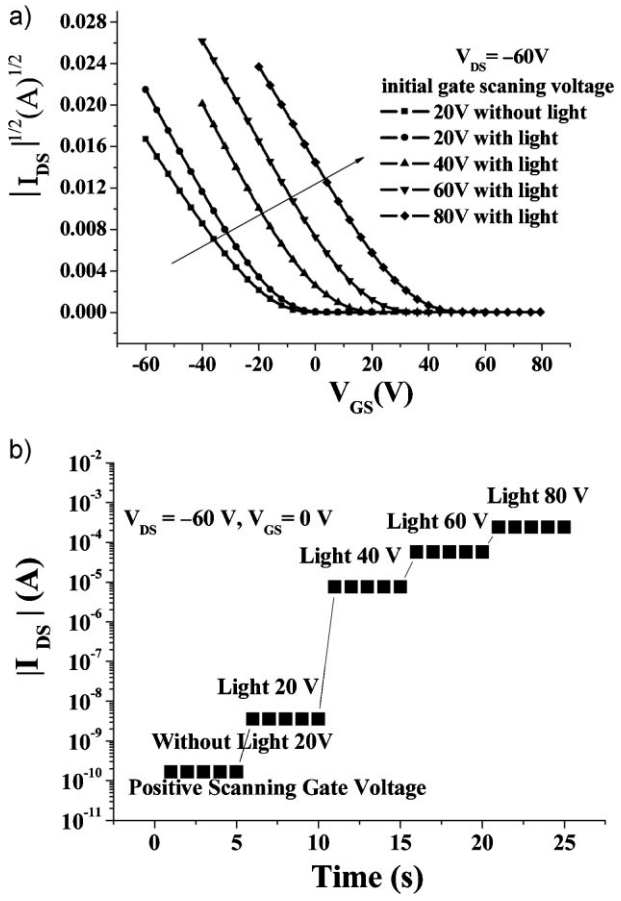

Figure 2. *I*–*V* characteristics of devices with the light-assisted program (the initial scanning gate voltages is $V_{GS,Start} = 20$ V, 40 V, 60 V, 80 V, $V_{DS} = -60$ V, and with the visible light increased with the arrowhead). a) $|I_{DS}|^{1/2}$ versus V_{GS} and b) the corresponding different current levels at $V_{GS} = 0$ V and $V_{DS} = -60$ V in the process for pentacene FET with PS modifying layer.

used to control the temperature, see Fig. S7 of the Supporting Information). It is clear that the working temperature for the devices should be below 60 °C. The long retention time and slight hysteresis behavior of the transfer curve without light (not shown here) at room temperature demonstrated that there were almost no charges transferring from the surface between the organic semiconductor and polymer.[12,18] If we consider the stability of each V_{th} level, and consider the stable $V_{th} = (32.5 \pm 1.5)$ V as signal ''00'', we will achieve another three stable signals, that is, $V_{th} = (14.0 \pm 1.0)$ V as ''01'', $V_{th} = (-7.1 \pm 1.0)$ V as ''10'', or $V_{th} = (-22.4 \pm 1.0)$ V as ''11'', by different $V_{Program}$, respectively (see Table 1). Meanwhile, we can obtain different almost-reversible stable V_{th} levels using different $V_{Light\text{-}assisted}$. The different and stable V_{th} levels demonstrated two-bits storage in single OTFT. Furthermore, in order to study the cyclability of the devices, we optimized the operating programs, and the cycling test was performed using light-assisted pulse-voltage process (see Fig. S8, Supporting Information). Although degradation was observed, our devices still achieved 100 times cyclability.

Although the exact mechanism for the charge storage in the thin polymer layer or the surface between the polymer and SiO_2 is not precisely understood, we offer possible models of electrons (Fig. 5a) and holes (Fig. 5b) being transferred and trapped between the semiconductor and the polymer under different programs to explain the phenomena in our devices. Figure 5c shows a possible mechanism of charge generation in the devices through a light-assisted mechanism with a power of 1 mW cm^{-2}. The light-sensitive organic semiconductors can generate excitons on the film surface and body when the photon energy is absorbed by these semiconductors. The higher-energy excitons would be easily separated from electrons in the materials. Finally, the electrons surmount the barrier of the semiconductor and polymer surface, and are trapped in the polymer layer or the surface between the polymer and the SiO_2 under a vertical transverse electric field.[19] Therefore, the semiconductor, polymer thickness, and surface quality will affect the carrier accumulation and charge tunneling. AFM studies show the high quality of the surfaces of the polymers with different thicknesses (see Fig. S9, Supporting Information). Increasing polymer thickness (15 nm, 30 nm, 60 nm) only increased the positive voltage needed for the same positive V_{th} shift, and had no obvious effect on the negative V_{th} shift. Meanwhile, no obvious effects were observed on our memory devices with the organic-semiconductor thickness for 30, 50, and 100 nm (semiconductor thicknesses commonly used in OTFTs without weakening their performances). Under those conditions, we used the devices with 50 nm pentacene and 10 nm polymer as samples to show the mechanism. With the irradiated visible light, the excitons were separated by the appropriate positive gate voltage, and the number of the electrons increased with the positive voltage increasing. The separated electrons were then injected and stored into the polymer layer or into the surface between the polymer layer and SiO_2. However, if there is no visible light, no obvious positive V_{th} shift is observed in our devices using $V_{GS,Start}$ (such as $V_{GS,Start} = 80$ V) and $V_{DS} = -60$ V. Meanwhile, if the positive voltage is not large enough (light-assisted transfer curve with $V_{GS,Start} = 20$ V, in Fig. 2a), the electrons cannot surmount the enhancing barriers (generated from the electrons repulsion) anymore. The stored electrons cannot be released for a long time, due to the high barrier formed by the polymer modifying layers. If the last light-assisted-program transfer curve was taken as the original state of the devices, multilevel V_{th} would be achieved only with a fast negative voltage program (about 1 μs). We would still be able to inject holes in the modifying layer of the devices using a larger negative-voltage program, due to the relatively lower energy barrier the holes would need to surmount. We would then be able to perform the light-assisted program again, and recover the devices to their original states.

In conclusion, a multibit storage OTFTs based on pentacene or CuPc were fabricated using PS or PMMA modifying layers through light-assisted programs. The devices showed excellent multibit storage ability, with 2 bits data storage in a single OTFT, high mobility (pentacene: $\mu > 0.5$ cm^2 V^{-1} s^{-1}; CuPc: $\mu > 0.01$ cm^2 V^{-1} s^{-1}), reversible V_{th} shifts with electrical and light-assisted programming, and long retention times (more than 250 h). These characteristics are believed to originate from the use of optical and electrical organic semiconductors, from performing the appropriate write and erase programs, and from the charge-storage ability of the polymer (or the surface between the polymer and SiO_2). After further investigation and optimization,

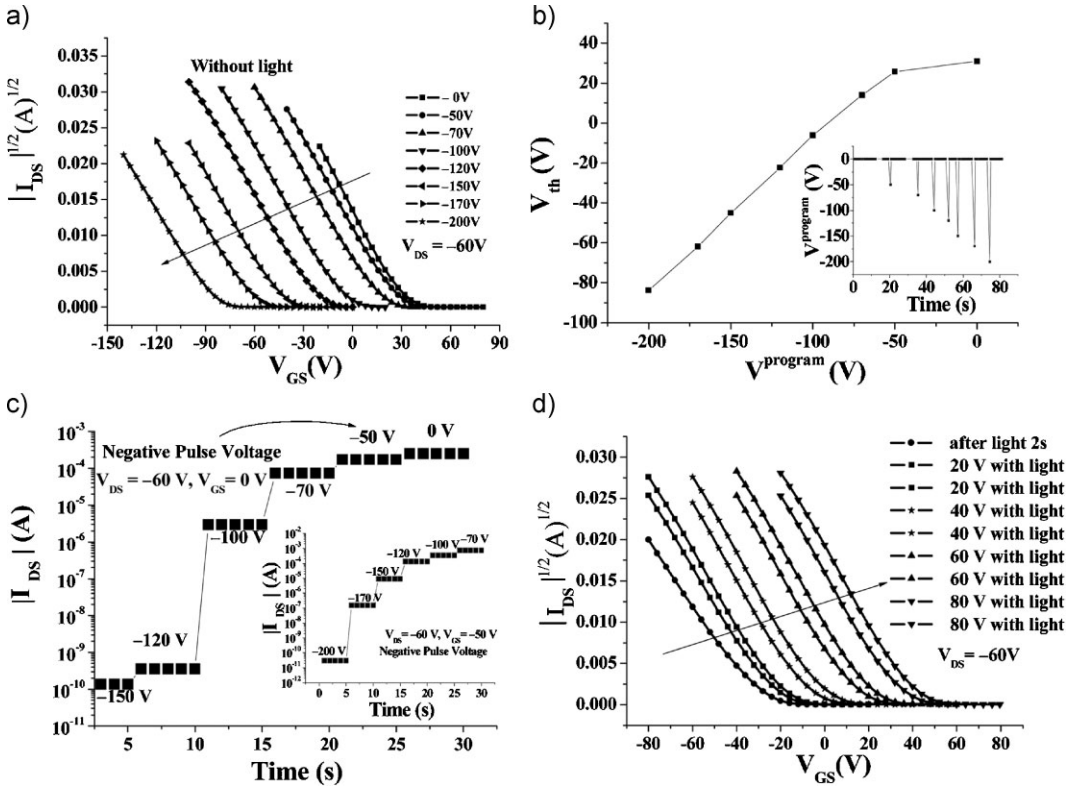

Figure 3. *I*–*V* characteristics of the devices based on pentacene with PS modifying layers. a) Different transfer curves of the devices using the voltage program ($V_{GS,Pro}$ = −50 V, −70 V, −100 V, −120 V, −150 V, −170 V, −200 V, V_{DS} = 0 V, t = 1 μs) without light, b) the corresponding threshold voltages (V_{th}, the inset plot with a different voltage program was performed for 1 μs during the measure process), and c) the corresponding different current levels at V_{GS} = 0 V, V_{DS} = −60 V and V_{GS} = −50 V, V_{DS} = −60 V (inset graph) in the process. d) Transfer curves of different light-assisted programs ($V_{GS,Start}$ = 20 V, 40 V, 60 V, 80 V, V_{DS} = −60 V under visible light emission).

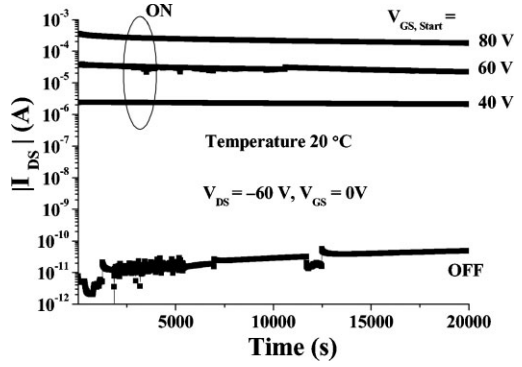

Figure 4. Current based on V_{DS} = −60 V and V_{GS} = 0 V with light-assisted start scanning of $V_{GS,Start}$ = 40 V, 60 V, 80 V and V_{DS} = −60 V (ON state), and $V_{GS,Pro}$ = −150 V, V_{DS} = 0 V, and t = 1 μs (OFF state) without light at room temperature.

the OTFTs can be potentially applied in low-cost, lightweight, and high-density-bits storage devices.

Experimental

OFET devices were fabricated with a top-contact configuration. A heavily doped n-type Si wafer and a layer of dry oxidized SiO_2 300 nm thick were used as a gate electrode and gate dielectric layers, respectively. The substrates were cleaned in water, deionized water, alcohol, and rinsed in acetone. The PS (or PMMA)-modifying layer was then prepared from a PS (or PMMA) solution in toluene by spin-coating on the surface of SiO_2. The thickness of the PS (or PMMA) film was measured using an Ambios Technology XP-2 surface profilometer. The Pentacene (or CuPc) was deposited onto the SiO_2 dielectric layer and the PS (or PMMA)/SiO_2 bilayers by high-vacuum evaporation at room temperature. The source–drain (*S*–*D*) gold contacts were thermally evaporated through a shadow mask. The channel length and width were 0.05 and 3 mm, respectively. For comparison, the devices with the same thickness of organic semiconductor and the same *L* and *W* were fabricated on the SiO_2/Si substrates without and with polymer modification. The electrical characteristics of the OFETs were measured using a Keithley 4200 SCS semiconductor parameter analyzer under ambient conditions at room temperature. The mobility of the OFETs in the saturation region was extracted from the following equation:

$$I_{DS} = \frac{W}{2L}\mu C_i(V_{GS} - V_{th})^2 \quad (1)$$

where C_i is the capacitance per unit area of the gate dielectric layer, V_{th} is the threshold voltage, and *L* and *W* are the channel length and width, respectively. The V_{th} of the device was determined by extrapolating the $(II_{DS,sat}I)^{1/2}$ versus V_{GS} plot to I_{DS} = 0.

In the bilayer insulators, the modifying PS (or PMMA) layer acts as a part of the dielectric layer during the operation. The capacitance (C_i) of the devices can be calculated using the following equation:

$$\frac{1}{C_i} = \frac{1}{C_d} + \frac{1}{C_m} = \frac{t_d}{\varepsilon_0\varepsilon_d} + \frac{t_m}{\varepsilon_0\varepsilon_m} \quad (2)$$

Table 1. Detailed information of the different voltage programs and the corresponding states based on pentacene with PS modifying layers.

$V_{Program}$	$V_{GS,Pro}$ ($V_{DS} = 0$ V, $t = 1$ μs)			
(V)	0	−70	−100	−120
V_{th} (V)	31.0	14.0	−6.1	−22.4
I_{DS} (A) ($V_{GS} = 0$V)	$(1.3 \pm 1.0) \times 10^{-4}$	$(3.1 \pm 1.0) \times 10^{-5}$	$(1.4 \pm 1.0) \times 10^{-6}$	$(6.0 \pm 5.0) \times 10^{-10}$
$V_{Light\text{-}assisted}$	$V_{GS,Start}$			
(V)	80	60	40	20
V_{th} (V)	33.7	14.0	−8.0	−22.3
I_{DS} (A) ($V_{GS} = 0$ V)	$(2.5 \pm 1.5) \times 10^{-4}$	$(4.5 \pm 1.0) \times 10^{-5}$	$(3.8 \pm 0.5) \times 10^{-6}$	$(8.1 \pm 5.0) \times 10^{-10}$
states	00	01	10	11

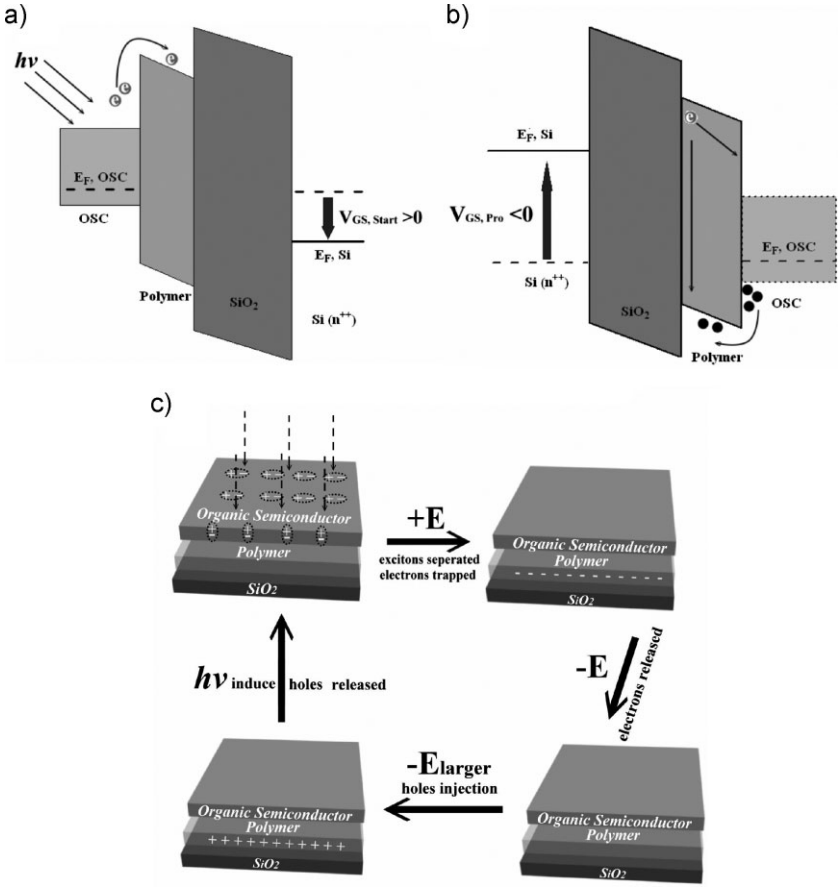

Figure 5. a) Model for electron transfer and trapping between the organic semiconductor and the polymer and b) model for hole transfer and trapping between the organic semiconductor and the polymer, where E_F,osc, E_F,Si, $V_{GS,Start}$, and $V_{GS,Pro}$ are the Fermi energies of the organic semiconductor and the silicon, the starting V_{GS}, and the gate voltage program of V_{GS}, respectively. c) Cartoon of the possible mechanism of the charge generation and complexation in the devices with the light-assisted program (E is the transverse electric field).

where t_m and t_d are the thicknesses of the PS (or PMMA) modifying layer and SiO_2 dielectric layer, respectively; and ε_m and ε_d are the dielectric constants of the modifying layer and dielectric layer, respectively.

Visible light was irradiated through a filter and the light spectroscopy was measured using a Photo Research PR-650 spectrophotometer. The illumination power was measured using a Newport 2385-C Si photodetector with a calibration module. AFM images were obtained using a Nanoscope IIIa AFM (Digital Instruments) in tapping mode.

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