A CMOS linear-in-dB VGA and AGC loop for telecommunication applications

V. Kalenteridis a,*, L. Mountrichas a, S. Vlassis b, S. Siskos a

Abstract

In this paper, an Automatic Gain Control (AGC) loop which is based on a linear-in-dB Variable Gain Amplifier (VGA) is proposed. The VGA structure is based on simple nMOS differential pairs with variable tail currents. The linear-in-dB gain tuning schema is designed using a novel exponential current generator which also offers temperature compensation of the VGA’s gain. The gain of the VGA is tuned by a control voltage with gain range about 28 dB with ±1 dB linearity error. The worst cases of the VGA gain, over process and temperature corners, are ±1.54 dB and ±2.45 dB for maximum and minimum gain setting, respectively. The proposed implementation is designed in a CMOS 90 nm triple-well process with 1.2 V supply voltage.

Keywords: AGC loop
CMOS linear-in-dB VGA
Exponential current generator

1. Introduction

Automatic Gain Control (AGC) loops are used in many modern telecommunication systems such as RF transceivers, where the amplitude of an incoming signal can be varied over a wide dynamic range [1–3]. The main goal of the AGC loops is to detect signal variations due to various effects, such as signal fading and provide relatively constant output amplitude or signal strength so that circuits following the AGC circuit require less dynamic range.

One of the key circuit elements involved in an AGC loop system is the variable gain amplifier (VGA) [4–7]. In wireless radios, a VGA is utilised in the receiver chain in order to achieve gain tunability using a control signal. Since the input power level of a receiver is varied by two or three orders of magnitude, thus the receiver’s gain range should cover this extremely input power range. The common way to achieve this is to make the gain a linear-in-dB function of the control signal. An advantageous result of this is that the settling time of the AGC loop is almost independent from the received power level [8]. A linear-in-dB function can be obtained by using MOS transistor operating in subthreshold region exploiting its exponential input characteristic [9,10], or pseudo-exponential functions with relatively small linearity error [13–16]. Among the most important requirements of a VGA is the temperature stability. Unfortunately, the usage of the exponential input characteristics of MOS in weak inversion has the disadvantage of strong temperature dependency which is mainly caused by the thermal voltage [4,5,11–13,15].

In this work, a linear-in-dB VGA with temperature compensation is presented, based on the pseudo exponential function $I_0e^{-\frac{V_{gc}}{V_{ref}}}$ with a linearity error $\pm 0.5$ dB in the temperature range of $0$–$80$ °C. This VGA is integrated as a part of a complete AGC loop which contains essential building blocks such as the peak detector, and the error integrator. The AGC loop is capable of monitoring input amplitude changes at the order of magnitude of 30 dB with 0.6 μs settling time.

2. VGA and exponential current generator

2.1. Principle of operation

The implementation of the current generator is based on the Taylor’s series expansion of the exponential function

$$I_{exp} = I_0e^{-\frac{V_{gc}}{V_{ref}}} = I_0\left[1 - \frac{a}{1!}\left(\frac{V_{gc}}{V_{ref}}\right) + \frac{a^2}{2!}\left(\frac{V_{gc}}{V_{ref}}\right)^2 - \ldots + \frac{a^n}{n!}\left(\frac{V_{gc}}{V_{ref}}\right)^n\right]$$

(1)

where $I_0$ is a constant current, $a$ is a constant factor, $V_{gc}$ is the control voltage and $V_{ref}$ is a reference voltage. Taking only the first and second order terms and assuming that the higher order terms are neglected, Eq. (1) is simplified as:

$$I_{exp} \approx I_0\left[1 - a\left(\frac{V_{gc}}{V_{ref}}\right) + \frac{a^2}{2}\left(\frac{V_{gc}}{V_{ref}}\right)^2\right]$$

(2)

The above simplification is valid only for small values of the ratio $V_{gc}/V_{ref}$. As the ratio $V_{gc}/V_{ref}$ becomes larger, then the higher
order terms value are not negligible and the approximation error increases. Eq. (2) can be rewritten in a more convenient form as:

$$I_{\text{exp}} \approx I_2 \left[ 1 + \left( 1 - \frac{V_{Vg}}{V_{\text{REF}}} \right)^2 \right]$$

(3)

The last equation will be implemented using the proposed exponential current generator.

2.2. Circuit of exponential current generator

According to Eq. (3), it is obvious that a voltage squarer is required due to the second term inside the bracket. The proposed voltage squarer which will be used for the circuit implementation is shown in Fig. 1.

It has a very simple structure since it consists of only three PMOS (M3–M5) and two NMOS (M1–M2) transistors. Transistors M3 and M5 have equal aspect ratio (W/L), while transistor M4 has double aspect ratio as of M3, M5. Two identical poly-silicon resistors form a voltage divider producing the appropriate gate voltage of transistor M4. Since these resistors exhibit very low temperature coefficient (~10 ppm/°C), due to their inherent manufacturing characteristics provided by the used process, they do not contribute significantly to VGA gain range due to temperature variations. Taking into consideration that PMOS transistors M3, M4 and M5 operate in the saturation region, their drain currents $I_{d3}$, $I_{d4}$ and $I_{d5}$ will be given by

$$I_{d3} = \frac{k_p}{2} \left( V_{Vg} - V_S - V_T \right)^2$$

(4)

$$I_{d4} = \frac{k_p}{2} \left( \frac{V_{Vg} + V_{\text{REF}}}{2} - V_S - V_T \right)^2$$

(5)

$$I_{d5} = \frac{k_p}{2} \left( V_{\text{REF}} - V_S - V_T \right)^2$$

(6)

where $I_{d4}$ is the drain current of the $i$th transistor, $V_T$ the threshold voltage of the PMOS transistors, $k_p = \frac{1}{2} \mu C_{\text{ox}} W/L$, and $V_S$ the voltage at their common source node. As it is shown in Fig. 1, the current $I_{d4}$ is mirrored to the output node through current mirror M1–M2. At the output node the current $I_{d4}$ is subtracted from the current summation $I_{d3} + I_{d5}$ producing the output current $I_{\text{out}}$. Based on Eqs. (4)–(6) the output current will be given by

$$I_{\text{out}} = (I_{d3} + I_{d5}) - I_{d4} = \frac{k_p}{2} \left( \frac{V_{Vg}}{V_{\text{REF}}} - V_{\text{REF}} \right)^2$$

(7)

where $k_p = 4k_p = k_p = 4k_p$. Eq. (7) shows that the output current is proportional to the square of the difference of the voltages, $V_{Vg}$ and $V_{\text{REF}}$. Since all PMOS transistors should be in saturation region, the control voltage $V_{Vg}$ is limited in the following range:

$$V_{Vg} \leq V_{dd} - V_{\text{sat},ib}$$

(8)

where $V_{dd}$ is the voltage supply and $V_{\text{sat},ib}$ is the saturation voltage of the tail current source. Also, the minimum allowable voltage supply is equal to $V_{CS} + 2V_{DS}$ making the circuit capable for low voltage operation.

The proposed exponential current generator is shown in Fig. 2. It is composed by two voltage squarers, connecting in such a way that the sum of their output currents $I_1$ and $I_2$ produce the final exponential current $I_{\text{exp}}$. The left squarer has two input voltages, one is the gain control voltage $V_{Vg}$ and the other one a constant reference voltage $V_{\text{REF}}$. Note that $V_{CM}$ in Fig. 2 indicates the input common-mode voltage level. Therefore, according to Eq. (7), the current $I_1$ will be equal to:

$$I_1 = \frac{k_p}{2} \left( \frac{V_{Vg}}{V_{\text{REF}}} \right)^2$$

(9)

For the squarer block at the right, which has only the reference voltage $V_{\text{REF}}$ as input, the corresponding output current $I_2$ will be:

$$I_2 = \frac{k_p}{2} \frac{V_{\text{REF}}^2}{V_{\text{REF}}^2}$$

(10)

The final exponential output current generated in the current summing node, is given by:

$$I_{\text{exp}} = I_1 + I_2 = \frac{k_p}{2} V_{\text{REF}} \left[ 1 + \left( 1 - \frac{V_{Vg}}{V_{\text{REF}}} \right)^2 \right]$$

(11)

Since, Eqs. (3) and (11) have similar form, the current $I_{\text{exp}}$ approximates an exponential function and is given by:

$$I_{\text{exp}} \approx \frac{k_p}{2} V_{\text{REF}}^2 \times e^{\frac{V_{Vg}}{V_{\text{REF}}}}$$

(12)

where

$$\left( \frac{k_p}{2} \right) V_{\text{REF}}^2 = I_0$$

2.3. Variable gain amplifier

In this paragraph the exponential current generator is used for gain control of a VGA with linear-in-dB function. The configuration of the VGA, with one amplification stage, connected with the exponential current generator is shown in Fig. 3. Each stage of the VGA consists of two cascade CMOS differential amplifiers with...
resistive loads. Transistors \( M_{n1}, M_{n2} \) and \( M_{n3} \) form a current mirror for biasing and controlling each differential amplifier.

The exponential current \( I_{\text{exp}} \) feeds each stage, through \( M_{p1}, M_{p2}, M_{n4} \) current mirror, forming the tail current of each stage. The transconductances \( g_{m4} \) and \( g_{m5} \) of the input differential pair transistors \( M_{q1,4b} \) and \( M_{q1,5b} \), respectively, is proportional to the square root of the tail current. Thus

\[
g_m = \sqrt{k_t I_{\text{exp}}} \quad (13)
\]

and the voltage gain of the first differential amplifier is given by

\[
A_1 = g_m R \quad (14)
\]

Since the differential amplifiers are identical, which in turn means that \( g_{m4} = g_{m5} = g_m \), the overall gain of one stage of the VGA can be written as follows:

\[
A_1 = A_{v1} \times A_{v2} = g_m^2 R^2 \quad (15)
\]

Based on Eqs. (12), (13) and (15) the gain will be equal to

\[
A_1 = k_p k_n R^2 V_{\text{REF}}^2 \times e^{-\frac{V_{r}}{V_{T}}} \quad (16)
\]

indicating the exponential gain variation versus control voltage \( V_{r} \).

2.4. Temperature compensation of the VGA

One of the most critical requirements for a variable gain amplifier is the temperature stabilization. The exponential current generator produces a current with strong temperature dependence, due to the mobility in term \( k_n = \mu_n C_{ox} \) as it is depicted by Eq. (11). Moreover it is obvious that a strong temperature variation holds for the VGA gain from Eq. (16). The gain is proportional to the product of the mobility terms \( \mu_n \) and \( \mu_p \) which in turn depend on temperature by the relation \( T^{-2} \), where \( \alpha \) is a factor almost equal to 1.5. According to this it is clear that an increment/decrement in temperature \( T \) results to a decrement/increment of the VGA gain \( A_1 \), which in its turn leads to a shifted VGA linear-in-dB gain curve up or down from the nominal one at room temperature. In order to stabilize the VGA gain over temperature, it is necessary for the slope of term \( V_{\text{REF}}^2 \) to compensate the temperature dependence of term \( k_n k_p \) meaning:

\[
\frac{\partial}{\partial T} \left( V_{\text{REF}}^2 \times e^{-\frac{V_{r}}{V_{T}}} \right) = \frac{\partial (k_n k_p)}{\partial T} \quad (17)
\]

Matlab processing of Eqs. (16) and (17) indicates the need of a positive slope for term \( V_{\text{REF}} \), which can be approximated by a linear equation at the known form of

\[
V_{\text{REF}} = \alpha + \beta T \quad (18)
\]

where \( \alpha \) and \( \beta \) are constant and slope factor, respectively. The appropriate value of \( \beta \) has been obtained by iterative simulations based on the VGA gain performance.

According to the previous analysis, it is necessary to add a circuit component in order to provide positive slope for \( V_{\text{REF}} \). For this reason a modified constant-\( g_m \) circuit block has been designed as illustrated in Fig. 4. Transistors \( M_{p1}, M_{p2}, M_{n1} \) and \( M_{n2} \) consist of the core of the constant-\( g_m \) circuit, operating in saturation region. Since the used CMOS technology is a triple-well process offering both \( p- \) and \( n- \)well transistors, \( M_{n1} \) was built in its own well in order to avoid body effect and thus has the same threshold voltage as \( M_{n2} \).

An external accurate resistor \( R \) with satisfactory stability over process/temperature is used to ensure the adequate operation of the constant-\( g_m \) circuit, due to the lack of integrated resistors with very low temperature coefficient in the majority of the modern sub-micron processes. The differential amplifier block \( \text{Amp} \) is used to force the drain voltages of \( M_{p1} \) and \( M_{p2} \) to be equal, forcing the currents \( I_1 \) and \( I_2 \) between the two branches to be equal too. Although voltage \( V_a \) at drain node of \( M_{n2} \) appears to have the desirable positive slope factor, it has to be level shifted to bias properly the transistor gates inside the exponential current generator. For this reason transistor \( M_{p4} \) is placed at the output branch of the constant-\( g_m \) block, where its gate is tied to the diode connected transistor \( M_{n2} \). Transistor \( M_{p3} \) acts as a current source to provide the appropriate bias current for the \( M_{p4} \). Finally, the output voltage \( V_{\text{REF}} \) is generated at the source terminal of \( M_{p4} \), which is connected in a source follower configuration (level shifter) to compensate the VGA gain variations.

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3. AGC loop design

The role of the AGC loop is to provide constant output power regards to the incoming signal variations of the receiver. The proposed AGC loop architecture, consisting of an exponential current generator, a variable gain amplifier (VGA), a power detector and a loop filter, is shown in Fig. 5.

The circuit structure of the power detector is the same one as the simple squarer circuit, used for the exponential current generator implementation. It is fed by the output signal of the VGA and generates a current \( I_{pd} \) proportional to the square of the VGA output voltage \( V_o \), as given by:

\[
I_{pd} = k_p(V_o)^2
\]

where \( k_p = \mu_p C_{ox}(W/L) \) of the pmos transistor inside the peak detector. Moreover a second squarer circuit is used to generate a current \( I_{rms} \) that is proportional to the square of a reference voltage \( V_{rms} \):

\[
I_{rms} = k_p(V_{rms})^2
\]

The two currents of Eqs. (19) and (20) are mirrored and finally subtracted at the node which is the inverting input of an operational amplifier, connected as integrator. The error current \( i_{er} = I_{rms} - I_{pd} \) is integrated by the filter, producing the control voltage \( V_{gc} \) of the exponential current generator. The error current becomes approximately equal to zero due to loop dynamic, resulting to

\[
V_o = V_{rms}
\]

The last equation states that the output voltage amplitude of the VGA is locked at the desired reference voltage.

The opamp based integrator (loop filter) used is a typical two stage Miller compensated amplifier and is shown at transistor level in Fig. 6. Transistors \( M_{n1,2} \) form a current mirror for biasing the first stage, consisting of the differential pair \( M_{n3,4} \) and \( M_{p1,2} \) as active loads. The second output stage consists of \( M_{p3-M_{n5}} \) in a push-pull configuration for rail-to-rail output voltage swing. Given that the exponential current generator operates for a limited input voltage range, the output voltage levels of the integrator must be changed between 350 mV and 750 mV. For this reason two diode connected transistors \( M_{p4-M_{n6}} \) are added playing the role of the output voltage limiter. When \( V_{out} \) tends to go high (1.2 V) \( M_{n6} \) is activated draining current from \( M_{p3} \) effectively lowering the output voltage to 750 mV. In the opposite case, when \( V_{out} \) tends to go low (0 V) \( M_{p4} \) is activated injecting current to \( M_{n6} \) raising the output voltage to 350 mV. Appropriate sizing of transistor \( M_{p4} \) and \( M_{n6} \) specifies the lower and upper output voltage of the opamp. In addition a set of Monte Carlo simulations has to be performed regarding to the matching of transistors \( M_{p3} \) and \( M_{n5} \) or else the limits will not be accurately specified.
4. Simulation results

All building blocks of the AGC loop have been designed and simulated using Cadence Design Framework II in IBM 90 nm RF CMOS process with 1.2 V nominal supply voltage. The specific circuit technology uses BSIM4 models for passive and active elements for simulation purposes. The nominal threshold voltages are $V_{th}=0.18$ V and $V_{tp}=-0.167$ V. In addition the used channel length $L$ is chosen large enough compared to the minimum length offered by the process, in order to minimize the second order effects, such as channel length modulation, mobility saturation and furthermore to increase the output resistance of the MOS devices. Moreover, the total width for each transistor has been split into multiple gate fingers to reduce parasitic gate resistance and drain-source capacitance.

Fig. 7 illustrates the exponential current versus control voltage $V_{gc}$. The control voltage $V_{ge}$ varies from $-270$ mV to $100$ mV and the exponential current ranges from $10$ μA to $45$ μA. Reference voltage $V_{ref}$ has a mean constant value of $450$ mV, generated by the modified constant-gm circuit and its changes tracking temperature variations. Also the current consumption of the exponential generator is $240$ mV and $380$ mV for minimum and maximum output current, respectively. The gain variation of the VGA against control voltage $V_{ge}$ for three different temperatures ($0$ °C, $27$ °C and $80$ °C) is depicted in Figs. 8 and 9 with and without temperature compensation, respectively. At typical case ($27$ °C) the VGA exhibits a $28$ dB gain range with a linearity error $\pm 1.4$ dB. As it can be observed from Fig. 8, the gain variation is about $\pm 1.54$ dB for maximum gain setting ($V_{ge} = -270$ mV) and $\pm 2.45$ mV for minimum gain setting ($V_{ge} = 50$ mV).

The corresponding gain variations according to Fig. 9 are about $\pm 5.45$ dB and $\pm 3.05$ dB, respectively. So an improvement of 4 dB and 0.6 dB is achieved by the use of the modified constant-gm circuit to suppress temperature variations, on the dynamic gain range of the VGA. Moreover, the linearity errors for $0$ °C and $80$ °C temperatures are $\pm 3$ dB and $\pm 1.1$ dB, respectively. The ac response of the VGA for maximum (circle) and minimum (dot) gain setting is shown in Fig. 10: the $-3$ dB cut-off frequency $160$ MHz and $180$ MHz, respectively.

Figs. 11 and 12 present the AGC loop dynamic response which was tested for two gain cases of the VGA. In the first case, the input amplitude increases to the high level of $79.75$ mV while the gain of the VGA decrease to the low value of $-2.55$ dB. In the second case, the input amplitude decreased to the low level of $3.5$ mV while the gain of the VGA increased roughly to the high value of $25$ dB. The transient responses for the aforementioned cases are shown in Figs. 11 and 12, where the output signal and the gain control voltage are plotted together. The voltage amplitude was defined to be equal $60$ mV, using the squarer of Fig. 4 with $V_{rms}=60$ mV. As it can be observed in Fig. 11, an increase in signal amplitude results to an increase in control voltage $V_{gc}$ which in its turn decreases the VGA gain, according to the dynamics of the loop. The opposite effect is observed in Fig. 12, where a decrease in signal amplitude results in an increase of the VGA gain. According to simulations, the settling time, as it was expected, remains almost constant at $0.65$ μs for the first case and $0.6$ μs for the second case.

In addition to examine the AGC loop behaviour regarding to process variations, a Monte Carlo analysis with $N=100$ has been performed, where $N$ is the number of random samples. The histogram plot shown in Fig. 13 indicates the relative difference in dB of the voltage amplitude before and after the input signal change at the VGA input. Assuming that a relative error in the order of the corresponding VGA linearity error is acceptable, Monte Carlo analysis has shown that almost $85\%$ of the occurrences results in locking the output signal at the appropriate voltage amplitude. The other occurrences result to a non-locking state of the AGC loop, consisting $15\%$ of the total sample numbers, indicating that a future improvement has to been done, in order to compensate this relatively small percentage. Particularly the circuit block of squarer operating as a peak detector needs to be optimized in terms of process variations, since it is responsible for the final amplitude voltage where the loop has to be locked.

Table 1 summarizes a comparison of the performance characteristics from prior works with the proposed one. As it can be observed the proposed AGC loop system exhibits the highest input dynamic range comparing with the other works. It also features a settling time and a power consumption that are lower than all
others except from reference [20], but comparing with the last one, the proposed design outperforms in terms of gain tuning range by 2 dB and data rate. The fastest settling time in [20] is justified by the fact that the loop system architecture is based on a feed-forward AGC loop, which theoretically has an inherent zero settling time [21], depended only by the time response of the peak detector. Moreover the occupied die silicon area is very low, despite the fact that a significant number of passive elements

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(resistors, capacitors) has been used inside at each block of the entire system.

5. Conclusions

A temperature compensated VGA based on an exponential current generator has been presented. The main characteristic of the last one is its simple structure consisting only of two voltage squarers. A 28 dB dynamic range with $\pm 1.4$ dB linearity error is achieved, while a modified constant-$g_{m}$ circuit compensates temperature variations of the VGA gain for a range of 0–80 °C. Finally, an AGC loop has been implemented with favorable characteristics such as tunable gain range, fast settling time, low power consumption and small die area, making it adequate for telecommunication applications.

![Fig. 10. VGA AC response for maximum and minimum gain.](image)

![Fig. 11. Transient response of the AGC loop for signal level increase.](image)
Fig. 12. Transient response of the AGC loop for signal level decrease.

Fig. 13. Monte Carlo histogram plot.

Table 1
Performance summary.

<table>
<thead>
<tr>
<th>Specification parameters</th>
<th>[5]</th>
<th>[6]</th>
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<th>[19]</th>
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* Chip area.

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