A Compact V-Band 3-D MMIC Single-Chip Down-Converter Using Photosensitive BCB Dielectric Film

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***Abstract*— A high-density monolithic-microwave integrated-circuit (MMIC) V-band down-converter, which employs the masterslice three-dimensional (3-D) MMIC technology and photosensitive benzocyclobutene (BCB) dielectric film, is presented in this paper. The 3-D MMIC process, which uses photosensitive BCB dielectric film, reduces the turn-around time by 66% compared to the polyimide-based fabrication process. The BCB-based fabrication process offers flexible metal configurations and high yields. The down-converter is structured on an 8 × 2 master array in a 1.84 mm × 0.87 mm chip. A newly developed down-converter MMIC with a heterostructure MESFET with $f_{\max}$ of 130 GHz consists of a two-stage radio-frequency amplifier and an image rejection mixer with an intermodulation frequency amplifier. This MMIC demonstrates a gain of 19.3 dB and an image rejection ratio of above 18 dB in the frequency range of 56.5–59.5 GHz; its associated gain density is five times higher than that of conventional MMIC's. This paper first clarifies the design criteria for 3-D MMIC packaging using the flip-chip bonding technique. The BCB-based 3-D MMIC technology with the flip-chip bonding will realize much cheaper millimeter-wave wireless equipment.**

***Index Terms*— Amplifier, BCB, down-converter, masterslice, millimeter wave, MMIC, mixer, three dimensional.**

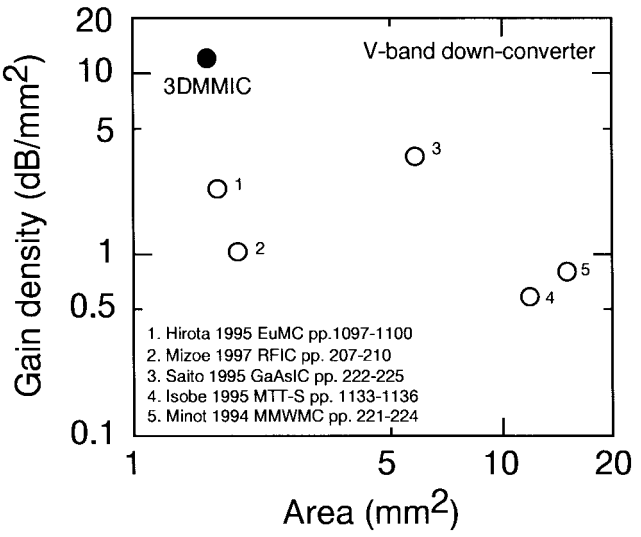

Fig. 1. Comparison of gain density of 3-D MMIC down-converter and planar MMIC down-converters.

I. Introduction

LOW-COST, highly integrated, and high-performance millimeter-wave equipment is strongly required by commercial wireless markets such as automotive radar, high-speed wireless local area networks (LAN's), multichannel video distribution system (MVDS), or local multipoint distribution services (LMDS). To realize such consumer millimeter-wave equipment, great reduction in the cost of both monolithic-microwave integrated-circuit (MMIC) chips and packaging are needed. Reported millimeter-wave MMIC's [1], [2] are large and offer low integration levels even though the wavelength is short, resulting in expensive MMIC's. This is because the coupling between adjacent line segments and the discontinuities in the circuits degrade circuit performance. Furthermore, the use of high-cost InP and InGaAs devices increases millimeter-wave MMIC cost. The authors reported high-density and potentially low-cost millimeter-wave masterslice three-dimensional (3-D) MMIC's that use polyimide dielectric film [3] as a solution to the above problems. The 3-D MMIC technology enables us to eliminate coupling between adjacent line segments and discontinuities such as bends and via holes because of its very fine structure. Accordingly, the 3-D MMIC technology realizes compact and highly integrated millimeter-wave MMIC's. Fig. 1 shows the gain density, defined as conversion gain (decibels) per chip area (mm^2), of V-band single-chip down-converter MMIC's, which consisted of a balanced (or image-rejection) mixer and associated amplifiers such as LO, RF, or IF amplifiers. The 3-D MMIC down-converter achieves the highest gain density of any single-chip down-converter yet reported. Another existing technology is flip-chip bonding, which is very effective in achieving cost reduction and high performance [4], [5].

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TABLE I
COMPARISON BETWEEN PHOTOSENSITIVE BCB AND POLYIMIDE DIELECTRIC FILMS

Dielectric layer	Polyimide	photosensitive BCB
Material constant	ε = 3.3 tanδ = 0.0004*	ε = 2.7 tanδ = 0.0008*
Moisture absorption	1 - 3 %	0 - 0.2 %
Cure temp.	350 °C	250 °C
Breakdown voltage	3×10^6 V/cm	
Patterning controllability	Comparable	
Loss of TFMS line (dB / λg) Z_0 = 50 Ω h = 10 μm f=60GHz	2.0	1.8

* @1MHz

A report on the flip-chip bonding approach for coplanar MMIC's showed that a bump height of over 20 μm is needed to avoid the parasitic effect from the motherboard [4]. However, no design guideline for the flip-chip bonding of 3-D MMIC's has been reported yet. This paper presents a compact V-band single-chip down-converter fabricated by a newly developed masterslice 3-D MMIC technology using photosensitive benzocyclobutene (BCB) dielectric film. First, this paper describes the features of the BCB-based fabrication process. The design and performance of the fabricated compact V-band single-chip down-converter are then shown. Finally, this paper examines the design criteria for the flip-chip bonding of 3-D MMIC's. The synergism realized by the combination of 3-D MMIC's and flip-chip bonding reduce the size and the cost of the millimeter-wave wireless equipment even further.

II. 3-D MMIC TECHNOLOGY USING PHOTOSENSITIVE BCB DIELECTRIC FILM

A. Fabrication Process

The structure and dimensions of the newly developed BCB-based 3-D MMIC fabrication technology [6] are the same as those found in polyimide-based 3-D MMIC fabrication [7] and uses four layers of 2.5-μm thick dielectric film and gold metal. The new process is quite similar to the polyimide-based 3-D MMIC fabrication process. The process steps are as follows.

1) Via holes and trenches are formed in a photosensitive BCB film by using photolithography.
2) A gold metal is formed by electroplating, after depositing adhesion metal and seed metal continuously by sputtering.
3) The gold metal is patterned by ion milling using a photoresist mask.
4) The photoresist mask is removed by O_2 that cannot etch the BCB film.

Table I compares the characteristics of polyimide and photosensitive BCB dielectric films, while Fig. 2 compares the fabrication turn-around time (TAT) of both processes. The lower moisture absorption of the BCB-based process offers short cure time. The negligible etching rate to remove the photoresist mask eliminates a thick stopper metal process normally used to protect the BCB film. Therefore, the BCB-based process provides a TAT that is one third that of the polyimide-based process, as shown in Fig. 2. The extremely low-moisture absorption of BCB also offers flexible metal configuration and enables simple packaging such as nonhermetic packaging. Via holes can be fabricated as stacked forms and spacing between formed metals is narrower than is possible with the polyimide-based process. These features indicate that the new process will yield greatly reduced cost and quick development. This technology can be applied not only to GaAs devices, but also to InP and InGaAs devices due to its low fabrication temperature and short process time.

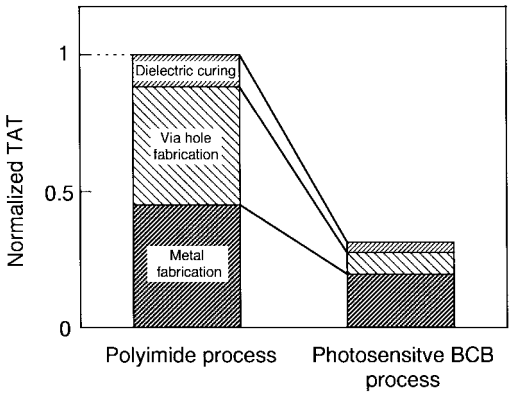


Fig. 2. TAT reduction of 3-D MMIC fabricated process.

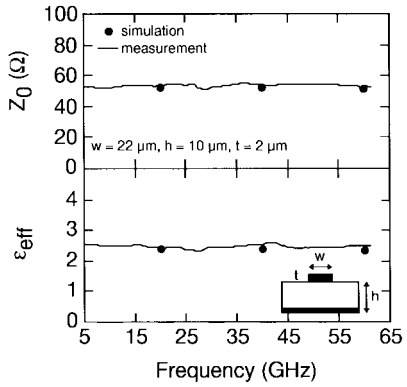


Fig. 3. Measured characteristics of TFMS line.

B. Thin-Film Microstrip Line Characteristics

Fig. 3 shows the measured characteristic impedance and effective dielectric constant of a 22-μm-wide thin-film microstrip (TFMS) line. Black circles plot simulated results, which are in good agreement with the measured results. The simulation was done by using "em" from Sonnet Software Inc., Liverpool, NY. Flat characteristics were obtained over the measured frequency range; the characteristic impedance was 49 Ω and effective dielectric constant was 2.52 at 60 GHz. The transmission loss of a TFMS line on a BCB layer is smaller than that on a polyimide layer because no thick stopper metal is needed for etching, as shown in Table I.

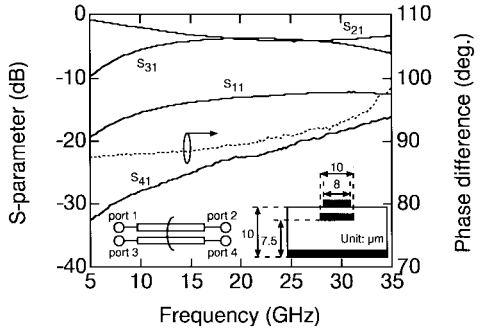


Fig. 4. Measured characteristics of broadside coupler on BCB-based 3-D MMIC.

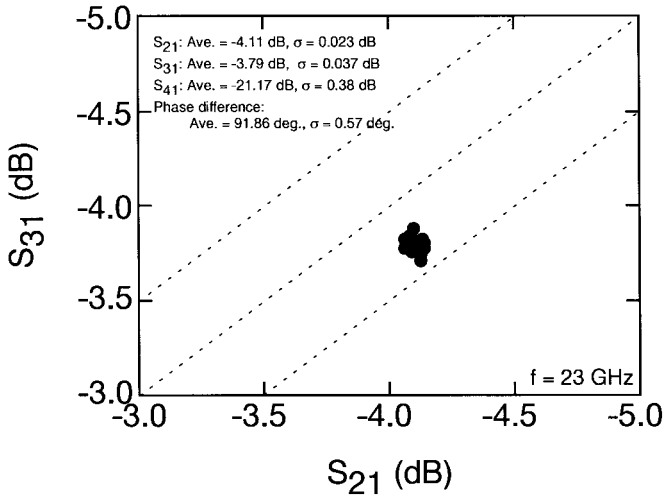


Fig. 5. Distribution of S_31 and S_41 of the fabricated broadside coupler on 3-in wafer.

C. Yield Performance

The performance of a broadside coupler significantly depends on the film thickness of the 3-D MMIC structure. Therefore, deviation in coupler performance is a direct indication of yield performance. Measured performance of a 20-GHz-band broadside coupler fabricated on the BCB-based 3-D MMIC is shown in Fig. 4. The size of the coupler is also shown. The fabricated coupler achieves an insertion loss of -0.9 dB$\pm$0.7 dB and a phase differences of 90°$\pm$2° over the frequency range of 15–31 GHz. S_41 and S_11 are better than -18 and -12 dB, respectively. Fig. 5 shows the deviation of S_21 and S_31 of the fabricated coupler with 100% yield on a 3-in wafer. Averages of S_21, S_31, and the phase difference for 21 fabricated samples on the wafer are -4.11 dB with $\sigma_{S_{21}} = 0.023$ dB, 3.79 dB with $\sigma_{S_{31}} = 0.037$ dB, and 91.9° with $\sigma = 0.57°$, respectively. These results indicate that the BCB-based 3-D MMIC fabrication process offers high yield and uniform performance.

III. Circuits Design and Performance

A. BCB-Based 3-D MMIC Structure with H-MESFET

The BCB-based 3-D MMIC structure combined with InGaP/InGaAs/GaAs heterostructure MESFET (H-MESFET) [8] is shown in Fig. 6. The bottom-level dielectric layer, which supports the T-shaped gate electrode, is 2-μm thick and the other dielectric layers are 2.5-μm thick. Each gold metal layer is 1-μm thick (top gold metal is 2-μm thick). Via holes can be stacked through all dielectric layers due to the low moisture absorption of the BCB; the guaranteed minimum size and spacing of the via holes are 9 and 3 μm, respectively. The H-MESFET has an $f_{\max}$ of 130 GHz and an f_T of 70 GHz. The gate–drain capacitance is about 20% more than the intrinsic capacitance of the FET due to the dielectric film covering the FET. Other FET parameters change slightly after the dielectric film is formed. The result is that the maximum stable gain decreases by a mere 0.6 dB at 60 GHz.

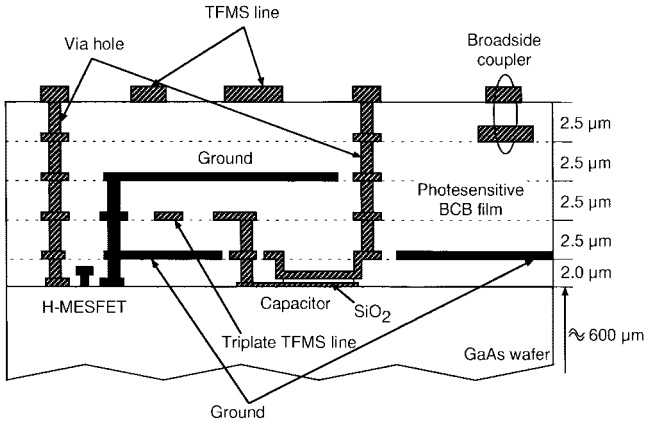


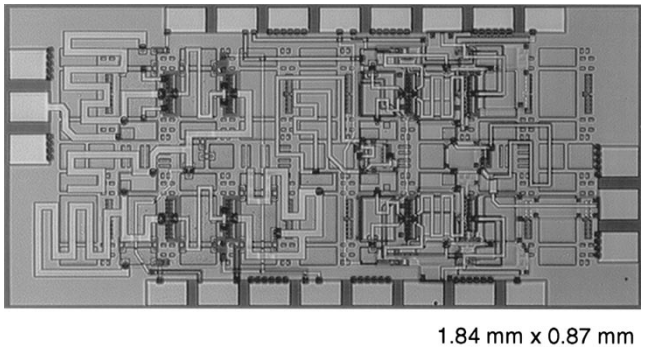
Fig. 6. Basic structure of BCB-based 3-D MMIC with H-MESFET.

B. Single-Chip Down-Converter MMIC

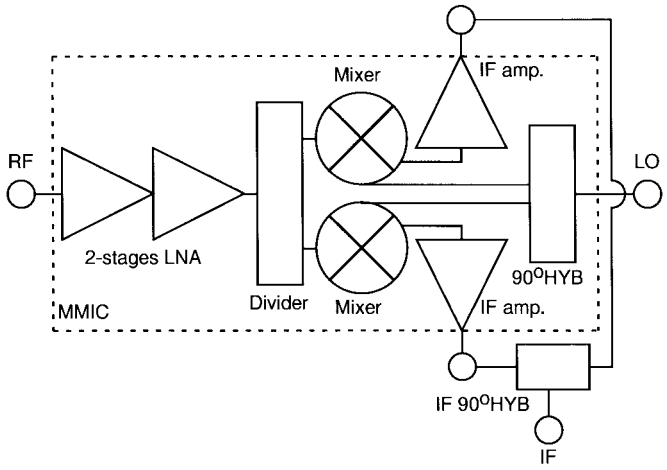
Fig. 7 shows a microphotograph and a block diagram of the fabricated down-converter MMIC. The down-converter consists of a two-stage RF amplifier, an image rejection mixer, and an IF amplifier in a single 1.84 mm $\times$ 0.87 mm chip. These circuits are designed around an 8 $\times$ 2 master array and the gatewidth of each device used is 100 μm.

The RF amplifier shown in Fig. 8 consists of a cascode-connected FET for both high gain and compactness. The connecting line (A in Fig. 8) between the common-source FET and common-gate FET, and the gate line (B in Fig. 8) of the common-gate FET effectively control the input and output impedance and, if properly designed, can realize high gain. The matching circuits of the RF amplifier consist of wide TFMS lines with a 22-μm-wide strip conductor on a 10-μm-thick substrate for lower loss matching. Loss of the input matching circuit is just 0.7 dB. Measured performance of the fabricated amplifier is shown in Fig. 9(a). Solid and dotted lines plot measured results and simulated results, respectively, and both are in good agreement. The gain of the amplifier is more than 17.5 dB and the noise figure is less than 7.5 dB. Fig. 9(b) shows the stability factor K. The K-factor is larger than three over the operating frequency band and its value increases monotonically at lower frequencies.

The image rejection mixer consists of two-drain LO injection mixers, a power divider, and a stacked (broadside) 3-dB coupler. The matching circuits of the mixer and IF amplifier



(a)



(b)

Fig. 7. V-band single-chip down-converter. (a) Microphotograph. (b) Block diagram.

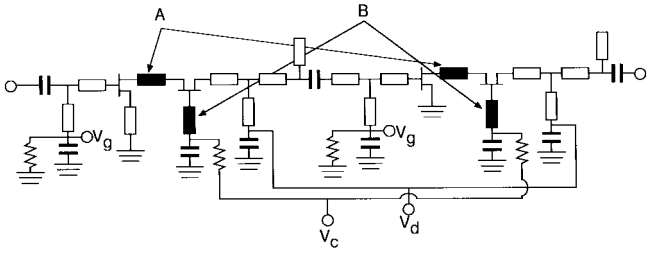
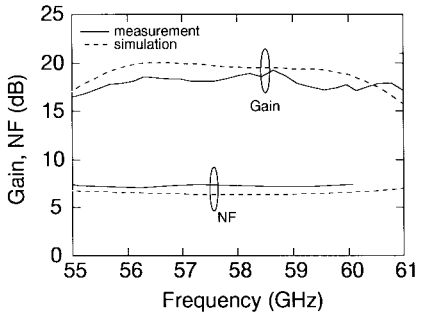
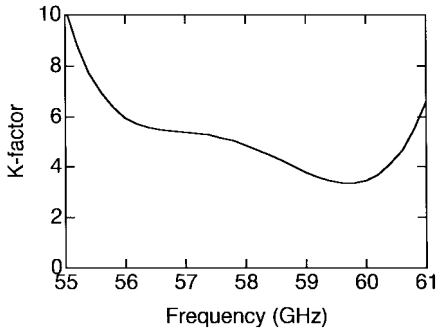


Fig. 8. Equivalent circuit of V-band two-stage amplifier.



(a)



(b)

Fig. 9. Measured performance of V-band two-stage amplifier. (a) Gain and noise figure. (b) Stability factor K.

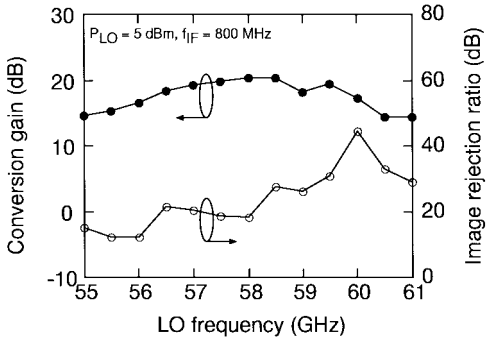


Fig. 10. Measured conversion gain of single-chip down-converter.

are stacked, for compactness, above and below a ground plane placed on the top surface of the middle BCB layer. The IF amplifier consists of a common-source FET and R–C matching circuits. The measured conversion gain of the image rejection mixer is around 1 dB over the measured frequency range when the LO power and IF signal are 5 dBm and 800 MHz, respectively.

The measured gain of the fabricated single-chip down-converter is shown in Fig. 10. The down-converter demonstrated a gain of 19.3 dB$\pm$1 dB and an image rejection ratio of greater than 18 dB over the LO frequency range of 56.5–59.5 GHz. The LO power and IF frequency are 5 dBm and 800 MHz, respectively. Fig. 11 shows the output power versus the input power characteristics at 60 GHz. The fabricated down-converter delivers a saturation power of about 3 dBm. The dissipation power is 220 mW ($V_d = 4$ V, $I_c = 55$ mA). The gain density of this chip is 12.1, which is more than five times that of conventional planar V-band down-converters in the same chip area, as shown in Fig. 1, and more than three times those of larger ones.

IV. Design Criteria for Flip-Chip Bonding

When using flip-chip bonding, it is important to ensure that the MMIC chips do not experience parasitic effect from the motherboard. A simple and effective solution is to keep some distance between the surface of the MMIC chip and motherboard. Fig. 12 shows deviation in TFMS line characteristics for a BCB-based 3-D MMIC on an alumina substrate motherboard. The linewidth and substrate height of the TFMS line

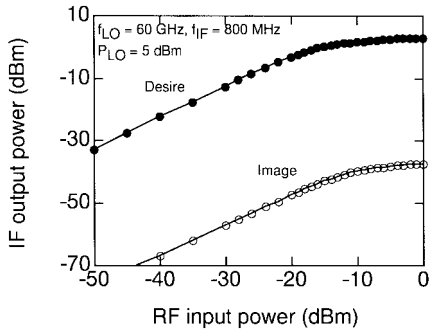


Fig. 11. Output power versus input power of single-chip down-converter.

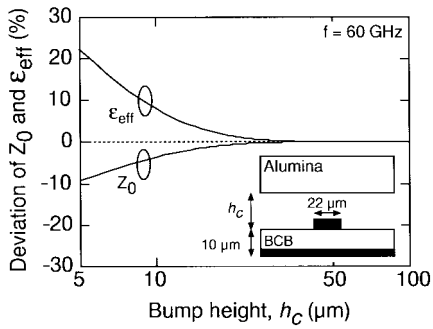


Fig. 12. Deviations of characteristic impedance and effective dielectric constant of TFMS line.

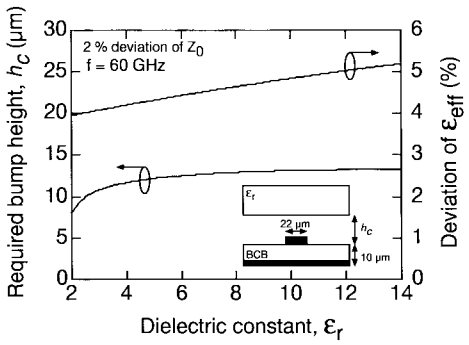


Fig. 13. Required bump height for 2% deviation of characteristic impedance.

are 22 and 10 μm, respectively. The characteristic impedance deviation of 2% can be taken as negligible in terms of MMIC performance [4]. These data indicate that the required bump height for the BCB-based 3-D MMIC's is just 13 μm and the corresponding deviation of the effective dielectric constant is 4.7%. The bump height is much shorter than that for coplanar MMIC's. Fig. 13 plots the required bump height for various dielectric constant of the motherboard and the corresponding deviation of the effective dielectric constant of the TFMS line. The required bump heights are above 14 μm over the calculated dielectric constant, while the corresponding deviation in the effective dielectric constant is less than 5.2%. These results indicate that BCB-based 3-D MMIC's can be employed on various kinds of motherboard by using flip-chip bonding technology with 20-μm bump height without special models or design techniques. Combining the 3-D MMIC technology with the flip-chip bonding promises high-performance millimeter-wave wireless equipment with further cost reductions.

V. Conclusion

This paper introduced a compact V-band single-chip down-converter MMIC as a 1.84 $\times$ 0.87 mm chip using a newly developed BCB-based masterslice 3-D MMIC technology. The fabricated down-converter MMIC achieves a gain density of 12.1, which is more than five times that of conventional planar MMIC's. The developed BCB-based masterslice 3-D MMIC process offers a fabrication TAT that is one-third that of the polyimide-based 3-D MMIC process and can also be applied to InP and InGaP devices due to its low process temperature and short process time. Combining the BCB-based 3-D MMIC process with high-performance devices will greatly improve the noise performance. This paper also clarifies the design criteria for flip-chip bonding 3-D MMIC's. 3-D MMIC's can be mounted on most materials without unusual models or techniques. These results indicate that the 3-D MMIC technology promises to greatly reduce the fabrication cost of millimeter-wave MMIC's and equipment.

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References

[1] K. Ohata, T. Inoue, M. Funabashi, A. Inoue, Y. Takimoto, T. Kuwabara, S. Shinozaki, K. Maruhashi, K. Hosaya, and H. Nagai, "Sixty-GHz-band ultra-miniature monolithic T/R modules for multimedia wireless communication systems," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 2354–2360, Dec. 1996.

[2] U. Güttich, A. Plattner, W. Schwab, I. Telliez, S. Tranchant, P. Savary, P. Bourne-Yaonaba, B. Byzery, E. Delhaye, C. Cordier, and M. Chelouche, "60-GHz GaAs MMIC technology for a high data rate mobile broad-band demonstrator," in *IEEE MTT-S Int. Microwave Symp. Dig.*, San Francisco, CA, June 1996, pp. 495–498.

[3] K. Nishikawa, K. Kamogawa, K. Inoue, K. Onodera, M. Hirano, T. Tokumitsu, and I. Toyoda, "Millimeter-wave three-dimensional masterslice MMIC's," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Baltimore, MD, June 1998, pp. 313–316.

[4] W. Heinrich, A. Jentzsch, and G. Baumann, "Millimeter-wave characteristics of flip-chip interconnects for multichip modules," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 2264–2268, Dec. 1998.

[5] T. Hirose, K. Makiyama, K. Ono, T. Shimura, S. Aoki, Y. Ohashi, S. Yokokawa, and Y. Watanabe, "A flip-chip MMIC design with coplanar waveguide transmission line in the W-band," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 2276–2282, Dec. 1998.

[6] K. Inoue, K. Kamogawa, K. Nishikawa, K. Ikuta, K. Onodera, and M. Hirano, "Three-dimensional MMIC interconnect process using photosensitive BCB and STO capacitors," in *Proc. 28th European Microwave Conf.*, Amsterdam, The Netherlands, Oct. 1998, pp. 642–647.

[7] M. Hirano, K. Nishikawa, I. Toyoda, S. Aoyama, S. Sugitani, and K. Yamasaki, "Three-dimensional passive circuit technology for ultra-compact MMIC's," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 2845–2850, Dec. 1995.

[8] K. Onodera, K. Nishimura, T. Nittono, Y. Yamane, and K. Yamasaki, "Symmetric and asymmetric InGaP/InGaAs/GaAs heterostructure MESFET and their application to V-band amplifiers," *IEICE Trans. Electron.*, vol. E81-C, pp. 868–875, June 1998.

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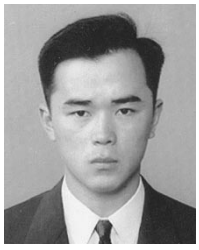

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