Some Work in Progress at IBM’s Austin Research Lab

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I. INTRODUCTION

Power-related research activities at IBM’s Austin Research Lab (ARL) include low power circuitry, power-efficient microprocessor designs, and server systems power measurement and management at many different levels.

Researchers are given the opportunity to see their contributions at all levels of product design, since IBM produces its own microprocessors for its System p, i, and z platforms as well as producing System x platforms with other vendors’ microprocessors, as well as marketing Tivoli systems management middleware.

II. ACTIVITIES

The Austin Research Lab’s Power-Aware Systems Department has partnered with development groups over the last 2 ½ years to produce the PowerExecutive™ systems measurement and management hardware and firmware features now available for most all System x rack-mounted servers (including blades) [1]. Again partnering with a development group, we also contributed many of the EnergyScale™ features in the recently announced POWER6 microprocessor, the first chip in the POWER architecture family that provides advanced power management features [2,3]. These features provide the basic mechanisms that support the dynamic, runtime control and reduction of power consumption as well as measurement sensors to ensure that the processor operates within a safe operating range and at the optimal performance level. In order to provide the best performance for the lowest power, the POWER6 chip has special facilities that an external microcontroller can use to track and intelligently control the behavior of the processor in real-time. Since power management can cause the processor to operate at a speed that is different from its nominal value, the POWER6 chip includes unique features that allow accounting, monitoring, and performance management software to track the changes in the processor’s operation.

Current research is focused around integrating chip-level, system-level and middleware-level features into a coherent whole meeting clients’ needs [4,5]. We are investigating how specific chip-level and higher-level features interact and their tradeoffs.

REFERENCES