A Comprehensive Study on the Soft-Error Rate of Flip-Flops From 90-nm Production Libraries

Tino Heijmen, Philippe Roche, Gilles Gasiot, Keith R. Forbes, and Damien Giot

Abstract—This paper presents a study using alpha- and neutron-accelerated tests to characterize the soft error rate (SER) of flip-flops (FFs) that are used in 90-nm CMOS production designs. The investigated FFs differ in circuit schematic, threshold voltage ($V_T$), drive strength, and cell height. Both the alpha- and the neutron-induced SER of FFs on a dedicated 90-nm test chip showed a strong dependence on clock and data state. Theoretical results demonstrate that the FF SER is modeled best if particle hits at both the NMOS and the PMOS drains are included and if the resulting current pulse is assumed to have a width of approximately 5 ps. Furthermore, the impact of process variations on the FF SER is shown to depend strongly on the data state and on the applied pulsewidth. On average, the SER per bit of the investigated FFs is higher than the typical SER per bit of unprotected static random access memories in 90 nm and has increased with a factor of 3 per technology generation. The reported results illustrate the importance of the characterization of FF SER in order to design reliable integrated circuits.

Index Terms—Accelerated test, alpha-particles, flip-flops (FFs), neutrons, process variations, radiation, sequential, soft error rate (SER), 90-nm process.

I. INTRODUCTION

Radiation-induced soft errors are an increasingly important reliability issue for integrated circuit (IC) design in deep-submicrometer technologies, demanding advanced characterization methodologies [1]. Both high-energy neutrons induced by cosmic radiation and alpha particles emitted by chip and package materials are capable of producing soft errors, also known as single event upsets. In some IC technologies the interaction of low-energy neutrons with boron atoms is a significant source of soft errors [2]. At the chip level, the contribution to the soft error rate (SER) from sequential logic, i.e., latches and flip-flops (FFs), is growing [1]–[3]. The SER per FF has increased due to feature size reduction and supply voltage downscaling. At the same time, it is more and more common to protect (embedded) memories with error-correction-coding circuitry, thus reducing their SER. As a consequence, the relative SER contribution from sequential logic is increasing. Combinatorial logic currently has a minor impact on the chip SER, particularly at moderate operational frequencies, but its contribution to chip SER is also growing with technology scaling [4].

An IC designer using standard-cell libraries generally can choose from a large variety of FFs and latches. The choice depends on the desired functionality (e.g., scannable or non-scannable; plain-, clear-, or preset-FF), timing properties, drive strength, power dissipation, etc. When moving into the technology nodes beyond 0.18 µm the SER of the sequential element is a new design metric that has to be taken into account. Therefore, it is important that accurate data are available about the SER of sequential elements that are used in production designs.

Several studies on the SER of latches and FFs have been reported. SER measurements were published for a 90-nm test chip with dedicated latch structures to investigate the dependence on drain diode type and drain area [5]. Recently, a study was presented on dedicated latch designs processed in a 65-nm technology [6]. Also experimental SER data have been reported for different FFs from a 0.13-µm production library [2], [7]. To our knowledge, the current work is the first detailed characterization study comparing the SER of different FFs from 90-nm standard-cell libraries used in a production design environment.

Part of the work that is presented here was also reported in [8]. Compared with that conference paper, the current work includes an analysis of the experimental results, using a model study. Also, this paper reports new alpha-SER results, because parts of the data of [8] were affected by a problem in the experimental setup. Finally, the theoretical study on the impact of process variations is extended with the effect of the current-pulsewidth.

The current paper is organized as follows. Section II discusses the details of the test chip and the applied test methods. In Section III, the experimental results are presented that were obtained from the alpha- and neutron-accelerated SER tests. Section IV describes a theoretical study that relates the measured SER results to modeled critical charge data. Also, this section discusses in detail the impact of process variability on SER. In Section V, we describe several technology scaling trends.

II. EXPERIMENTAL DETAILS

A. Test Chip

A dedicated test chip was designed to measure the SER of five different FFs. The design was processed in a 90-nm CMOS process optimized for low-power applications and had a nominal supply voltage of $V_{DD} = 1.2$ V. The chip contained...
TABLE I
INVESTIGATED FFs

<table>
<thead>
<tr>
<th>FF</th>
<th>Name</th>
<th>Type</th>
<th>Drive</th>
<th>$V_T$</th>
<th>$h_{cell}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF1</td>
<td>DF1QX05</td>
<td>Plain-FF</td>
<td>0.5×</td>
<td>std</td>
<td>14 pitch</td>
</tr>
<tr>
<td>FF2</td>
<td>DF1QX05V</td>
<td>Plain-FF</td>
<td>0.5×</td>
<td>high</td>
<td>14 pitch</td>
</tr>
<tr>
<td>FF3</td>
<td>DF1SQY1</td>
<td>Plain-FF</td>
<td>0.5×</td>
<td>std</td>
<td>9 pitch</td>
</tr>
<tr>
<td>FF4</td>
<td>DF1QX2</td>
<td>Plain-FF</td>
<td>2×</td>
<td>std</td>
<td>14 pitch</td>
</tr>
<tr>
<td>FF5</td>
<td>DF2SQX05</td>
<td>Clear-FF</td>
<td>0.5×</td>
<td>std</td>
<td>14 pitch</td>
</tr>
</tbody>
</table>

five first-in, first-out (FIFO) shift registers, each containing 100 k (= 102400) cells. A large number of cells are required to obtain accurate neutron-SER data within an acceptable test time. In this paper, the experimental error of the neutron-SER data is 20% or better. The experimental inaccuracy of the alpha-SER data is 5% or better, except for the cases where the observed SER is extremely low (< 10 norm. units). These experimental errors are based on a chi-squared analysis of the 90% confidence limits.

To prevent data corruption due to upsets at clock nodes [9], only large buffer cells were used in the clock-tree. Circuit simulations showed that the critical charge ($Q_{crit}$) for upsets at the clock buffers was larger than 50 fC. This $Q_{crit}$ does not guarantee a neutron-SER immunity of the buffers, but reduces the upset probability to extremely low values. Therefore, the clock-tree of the test chip can be regarded as insensitive to alpha and neutron radiation. The test-input and test-enable signals (in the case of scannable FFs) and the clear-data signal (in the case of clear-FFs) were fixed with the use of tie-off cells, to prevent that internal nodes were floating.

The FFs were selected from standard-cell libraries that are used in the design of production chips. The five FFs, selected from a much larger set, have different properties but are all commonly used in production designs. Therefore, they are well suited for a comparative study of the effect of different design choices on the FF SER in real-life IC designs. The main characteristics of the FFs are summarized in Table I.

FF1 can be regarded as the reference cell: It is a plain-FF with standard-$V_T$ transistors, the lowest available drive strength (0.5×), and has a 14-pitch cell height, which is the default for two of the three companies in the Crolles2 Alliance (STMicroelectronics and NXP Semiconductors). The other four FFs each differ from FF1 in a single respect. FF2 has the same layout but contains transistors with a $V_T$ that is about 100-mV higher than in FF1. FF3, from a Freescale library, has a 9-pitch cell height, which is the default in this company. Furthermore, the cell has a different schematic. One of the differences is that the master and slave latches in FF3 are connected by a transmission gate, whereas in the other FFs the master and slave latches are connected by an inverter plus transmission gate. FF4 is different because it has a 2× driver strength. FF5 is a clear-FF and consequently has a different schematic. This FF was selected because clear-FFs are most widely applied, together with plain-FFs.

FF1, FF2, and FF4 are nonscannable FFs; FF3 and FF5 are scannable. The latter are of the mux-scannable type, which implies that only the input stages are different from their non-scannable analogs. The feedback loops in the master and slave latches are not affected by the scannability. Although the cell area of the scannable version of an FF is typically 20%–30% larger than for the nonscannable variant, it is unlikely that this difference has a significant effect on the SER, because the parts of the cell that contain the feedback loops are identical. Therefore, we assume that scannability does not affect the FF SER.

B. Accelerated SER Testing

Both alpha- and neutron-accelerated SER tests were performed to characterize the SER performance of the FFs. For alpha-accelerated testing, an Am-241 foil was used that was placed over the device under test (DUT) with a measured foil-to-DUT distance of 0.2 mm. The alpha-accelerated tests were performed in air and at room temperature. A monochromatic source (Am-241, emission energy is 5.4 MeV) was used because a broad-spectrum source (for example Th-232) was not available. It is known that the use of a monochromatic source can give different results compared to the use of a broad-spectrum source [10]. The neutron-accelerated measurements were performed at the TRIUMF facility in Vancouver, Canada [11]. Four samples were used in the alpha-accelerated SER tests and two (different) samples in the neutron-accelerated tests. All samples were taken from the same wafer. All tests were compliant with the JEDEC standard JESD89 and its addenda JESD89-2 and -3 [12]–[14]. Static tests were performed by writing either an All1 (Solid1) or an All0 (Solid0) pattern into the shift registers and by setting the clock (CLK) signal either to a constant high or to a constant low value during irradiation. In the CLK = HIGH state, the master latch of the FF is sensitive to upsets; in the CLK = LOW state the slave latch is. Thus, SER is measured at four different states, due to the combination of two data and two clock states. The alpha-SER results presented in this paper have been extrapolated to a nominal flux of 0.001 $\alpha$/h · cm$^2$. The neutron-SER results have been extrapolated to a flux of 14 neutrons/h · cm$^2$, which corresponds to the nominal neutron flux of NYC. In this paper, we focus on the SER of FFs under static conditions. For a discussion on the SER of sequential logic under dynamical conditions the reader is referred to [15].

III. EXPERIMENTAL RESULTS

A. Alpha-SER at Nominal Supply Voltage

Fig. 1 shows the measured alpha-SER values at nominal supply voltage ($V_{DD} = 1.2$ V). All SER data reported in the current paper have been normalized by scaling with a fixed and arbitrary factor. The results reported here differ from the alpha-accelerated SER data of [8], which suffered from a problem in the experimental setup. Because of this, in some cases fewer errors were observed than were actually present in the DUT. The problem in the experimental setup was solved and new alpha-accelerated SER results are presented in the current paper. The issue did not affect the neutron-accelerated SER data.
that were reported in [8] and in Sections III-C and D of the current paper.

Fig. 1 clearly shows that the SER of each of the FFs strongly depends both on the clock state and on the data state. Furthermore, large differences can be observed between the tested FF types. Comparison of FF1 and FF2 shows a small but significant difference, with FF2 having the lower SER for all four states. On average, the SER of FF2 is 15% lower. This result is in agreement with previously reported data showing that the SER of FF2 is 15% lower. This result is in agreement with previously reported data showing that the SER of 0.13-µm static random access memories (SRAMs) processed with the use of the high-\(V_T\) process option is half as large compared to standard-\(V_T\) SRAMs [16]. The difference can be explained by a reduction in the charge collection efficiency when high-\(V_T\) transistors are used.

The dependence of the SER on the data and clock states is very different for FF3 compared with the other FFs. The highest SER was observed for CLK = LOW and Data = 1, whereas the other FFs showed a minimum SER at these conditions. The FF3 cell has a 9-pitch (instead of a 14-pitch) cell height and was designed by a different library group than the other cells. In the design of FF3, different choices were made with respect to circuit topology and transistor sizing. This example demonstrates that cell design has a large impact on the FF SER.

Fig. 1 also demonstrates a strong relation between the driver strength of an FF and the SER of the slave latch. FF1 and FF4 have an identical master latch and consequently show the same SER for CLK = HIGH. However, if CLK = LOW the SER of FF4 is about an order of magnitude lower. This difference is caused by the larger critical charges of the slave latch of FF4. The 2\(\times\) driver strength of FF4 is accomplished by using two inverters in parallel in the output state of the cell, each being two times as large as the single output inverter of FF1. The extra gate capacitance from the larger output stage makes that the amount of collected charge that is needed to flip the state of the slave latch is much larger for FF4.

Finally, FF5 shows a lower SER than FF1 if CLK = HIGH. For the cases where Data = 1 and Data = 0, the SER of the master latch is 20% and 65% lower, respectively. To implement the clear functionality in the FF, two additional transistors have been included in the feedback loop of the master latch and two in the feedback loop of the slave latch. The inclusion of these transistors also affects the sizing of the other transistors in the cell. Consequently, the critical charges of the cell are different from the plain-FFs, which result in lower SER values for the master latch. The fact that the SER of FF5 for CLK = LOW is comparable to FF1, both for Data = 1 and Data = 0, can be regarded as coincidental, because also the slave latch is affected by the extra transistors.

Although the measured SER at a specific operational condition is very different for the five FFs, only a moderate difference was observed for the average values. The lowest average SER, observed for FF5, is only 45% lower than the highest average SER, corresponding to FF1.

B. Voltage Dependency of Alpha-SER

Also the dependence of the SER on the supply voltage was investigated for the four different states. For this purpose, \(V_{DD}\) was varied from 0.4 to 1.5 V. At voltages below 0.8 V, the writing and reading of the shift registers was done at the nominal voltage and \(V_{DD}\) was lowered during irradiation. Because of this and because the tests were performed under static conditions, metastability did not influence the test results. Note that a monochromatic alpha-source (Am-241) was used in this paper. The application of a broad-spectrum source generally results in a different \(V_{DD}\) dependence [10].

The \(V_{DD}\)-dependence of the alpha-SER results is presented in Fig. 2. Again, the data reported here are more accurate than those in [8]. The alpha-SER shows an almost exponential dependence on \(V_{DD}\). Only at very low voltages a weak \(V_{DD}\)-saturation effect can be observed in some cases, e.g., for \(V_{DD}\) = HIGH, Data = 1.

The \(V_{DD}\)-dependence is stronger if Data = 1 then if Data = 0, except for FF3, CLK = LOW. Also, the dependence on \(V_{DD}\) in the states with CLK = LOW is much stronger for FF4 than for the other FFs. The larger \(Q_{crit}\) of FF4 in the CLK = LOW states, because of the large gate capacitance of the output stage of the slave latch, has a more important effect if \(V_{DD}\) is high. Furthermore, if CLK = LOW, Data = 1, the SER of FF3 decreases more slowly with increasing \(V_{DD}\) than the SER of the other FFs. As was discussed in Section II-A, the connection between the master and the slave latch in FF3 is different compared to the other FFs. This is an additional example that the design of the FF has an impact on the SER, not only on the SER value at nominal \(V_{DD}\), but also on the voltage-dependence.

C. Neutron-SER at Nominal Supply Voltage

The results for the neutron-SER at the nominal voltage of \(V_{DD} = 1.2\) V are depicted in Fig. 3. The normalization of the SER data in Fig. 3 is the same as in Fig. 1.

On average, the neutron-SER is lower than the alpha-SER. The ratio between the neutron-SER and alpha-SER, both averaged over all five FFs and all four states, equals 0.31. As discussed in Section II-B, we assume a nominal alpha-particle flux of 0.001 \(\alpha/\text{h} \cdot \text{cm}^2\). This corresponds to a situation where highly purified materials are used in the packaging and in the IC.
processing [17]. In older technologies, neutrons dominate the FF SER, because of the high $Q_{\text{crit}}$. This paper shows that the importance of the alpha-induced SER is increasing, despite the ongoing efforts in the IC industry to reduce the alpha-particle flux in use conditions. The contributions from both neutrons and from alpha particles must be taken into account when characterizing the FF SER in deep-submicrometer processes.

In a number of test runs Cadmium was used to shield the DUT from low-energy neutrons. Runs with and without shielding did not show any significant difference in SER. This result demonstrates that ICs manufactured in the investigated technology are not sensitive to low-energy neutrons. This result was expected, because no BPSG had been used in the processing of the chip [17].

Comparing the neutron-SER results of Fig. 3 with the alpha-SER data of Fig. 1 shows that in general the same trends can be observed, but with some significant differences. First, the variation in neutron-SER for a given operational condition is smaller. As an example, consider the most sensitive cell (FF3) and the least sensitive cell (FF4) for the state $\text{CLK} = \text{HIGH}$, Data = 1. The variation in alpha-SER is more than two orders of magnitude, whereas the difference in neutron-SER equals only a factor of 8. This is because the collected charge resulting from a neutron hit is much larger than in the case of an alpha hit [7].

Although weaker than for the alpha-SER, a significant dependence on the data state is also observed in the neutron environment. For example, FF3 at $\text{CLK} = \text{LOW}$ shows a difference in neutron-SER of a factor of 5 between the Data = 1 and Data = 0 states. Also, a nonnegligible dependence on the CLK state is observed. For FF4 at Data = 1 the CLK = HIGH state has a 5× higher SER than the CLK = LOW state.

The differences in the average value for neutron-SER are even smaller than for alpha-SER. The highest average neutron-SER was observed for FF5, which showed the lowest SER contribution due to alpha particles. The lowest average SER is found for FF4. The averages for FF4 and FF5 are 15% lower and 10% higher than for FF1, respectively. Note that these differences are smaller than the experimental error of 20% for the neutron-SER data.
D. Voltage Dependency of Neutron-SER

The dependence on $V_{DD}$ of the neutron-SER is depicted in Fig. 4 for the different data and clock states. This figure shows a much weaker voltage dependence than is observed for the alpha-SER in Fig. 2. Also at $V_{DD} = 1.5$ V the observed SER value for all five FFs and all four states is relatively high. Increasing $V_{DD}$ from 0.8 to 1.5 V leads to a $6.0 \times$ reduction in the average alpha-SER of the five FFs, whereas the decrease is only $2.6 \times$ for the average neutron-SER. This is due to the larger collected charge in the case of neutron hits, which makes the SER less dependent on $Q_{crit}$, as was discussed above. The variation in SER between the different FFs and the different states is significantly smaller than for the alpha-SER. At all investigated supply voltages, the spread was less than one order of magnitude. If CLK = HIGH and Data = 0, the SER of the five FFs even agrees within a factor of 2.

IV. THEORETICAL RESULTS

A. Modeling of Experimental SER Data

In order to analyze the experimental data in a quantitative manner, the measured SER was modeled as a function of the sensitive diffusion area $A_{diff}$ and the critical charge $Q_{crit}$ [18], [19]. $Q_{crit}$ is defined as the minimum amount of charge that needs to be injected in a circuit node to produce a soft error. The critical charges were calculated with the help of a proprietary SPICE-like circuit simulator, using netlists that include back-end-of-line parasitics. In these simulations, the charge collection process was modeled using a current source that injects into a sensitive circuit node a current pulse of the form [20]

$$I_{pulse}(t) = \frac{2}{\sqrt{\pi}} \frac{Q_{tot}}{\tau} \sqrt{\frac{T}{\tau}} \exp\left(-\frac{t}{\tau}\right)$$

(1)

where $\tau$ is a timing parameter determining the width of the current pulse. The full-width at half-maximum (FWHM) of the pulse equals $1.79 \times \tau$. $Q_{tot}$ denotes the total amount of charge contained by the pulse. With $\tau$ fixed, $Q_{tot}$ is varied in order to find the value for which the current pulse causes an upset. By definition, this value equals $Q_{crit}$. The model for the current pulse is an important factor in the $Q_{crit}$ simulation [21]. The advantage of the model of (1) over, for example, a double-exponential model is that $Q_{crit}$ can be studied as a function of the pulsewidth by varying a single timing parameter.

We first focus on the modeling of the alpha-SER data presented in Section III-B. The most straightforward model assumes that the only cause of soft errors is ionizing particles that intersect the drain diffusion area of NMOS transistors in the OFF-state. In this case, the collection of electrons by an NMOS drain junction results in a current pulse that upsets the cell. The critical charge for an upset is then denoted by $Q_{crit,e}$ and the sensitive drain diffusion area by $A_{diff,N}$. $Q_{crit,e}$ was calculated using a current pulse of the form of (1) with a timing parameter of $\tau = 90$ ps. In this simple model the SER depends

Fig. 4. $V_{DD}$-dependence of neutron-SER.
charge associated with such an upset is denoted $Q$ by the collection of holes instead of electrons. The critical NMOS transistors. In this case, the current pulse is formed particles intersecting the drain junctions of PMOS instead of $-\eta$ only good. The correlation coefficient for these two variables equals $\tau$ shows that the quality of the first-order model of (2) is not very exponentially on $Q_{\text{crit,e}}$ and linearly on $A_{\text{diff,N}}$, which results in the well-known power-law [18], [19]

$$\text{SER} = \kappa A_{\text{diff,N}} \exp(-Q_{\text{crit,e}}/\eta)$$

(2)

where $\kappa$ denotes an overall scaling factor and $\eta$ is a measure for the charge collection efficiency for a given type of radiation and a given IC process technology [18]. The quality of the model can be studied by making a scatter-plot of $\log(\text{SER}/A_{\text{diff,N}})$ versus $Q_{\text{crit,e}}$. Plotting $\log(\text{SER}/A_{\text{diff,N}})$ is preferred over plotting SER, because the former quantity depends linearly on $Q_{\text{crit,e}}$, according to (2). The scatter-plot depicted in Fig. 5 shows that the quality of the first-order model of (2) is not very good. The correlation coefficient for these two variables equals only $-0.58$.

An improved model also includes upsets due to ionizing particles intersecting the drain junctions of PMOS instead of NMOS transistors. In this case, the current pulse is formed by the collection of holes instead of electrons. The critical charge associated with such an upset is denoted $Q_{\text{crit,h}}$. The area of the sensitive drain junction is $A_{\text{diff,P}}$. Here, we assume that if $Q_{\text{crit,h}}$ is smaller than $Q_{\text{crit,e}}$ then the upset is caused by the collection of holes by PMOS drain junctions. Otherwise, the cause of the upset is the collection of electrons by NMOS drains. Fig. 6 shows the corresponding scatter-plot of $\log(\text{SER}/A_{\text{diff}})$ versus $Q_{\text{crit}}$, where $Q_{\text{crit}}$ denotes the minimum of $Q_{\text{crit,e}}$ and $Q_{\text{crit,h}}$. Similarly, $A_{\text{diff}}$ equals $A_{\text{diff,N}}$ if $Q_{\text{crit,e}} \leq Q_{\text{crit,h}}$, and $A_{\text{diff,P}}$ otherwise. The correlation between the two variables in the scatter-plot is much higher than if only NMOS drain hits are assumed. The correlation coefficient equals $-0.85$ in this case.

The width of the current pulse that causes upsets can vary from a few picoseconds to hundreds of picoseconds [22]. A timing parameter $\tau = 90$ ps is representative for a relatively wide pulse. In this case, generally, the current pulse is caused by a track of an ionizing particle that does not intersect a drain junction. Diffusion is then the main charge collection mechanism. Theoretical studies have shown that typically 80%–90% of neutron-induced upsets are caused by nondrain-intersecting events [23]. However, others have reported that the average current pulse due to a neutron hit has a time scale of approximately 10 ps, both for electron and for hole collection [22]. An alpha hit produces a longer pulse, but nearly all the charge is collected within the first 10 ps, as for neutrons. Typically, the FWHM of such pulses is on the order of 5 ps. This corresponds to a value of approximately $\tau = 3$ ps in the current-pulse model of (1). Typically, such a narrow pulse is caused by a particle that intersects the drain junction. In this case, the induced charges are predominantly collected through drift in the high electric fields.

The question is valid if $Q_{\text{crit}}$ data calculated using a pulse with $\tau = 3$ ps show a better correlation with the experimental SER results than when a pulse with $\tau = 90$ ps is used. The results are shown in the scatter-plot of Fig. 7. The correlation
between the experimental data and \( Q_{\text{crit}} \) is significantly better than in the case of \( \tau = 90 \) ps, shown in Fig. 6. The correlation coefficient equals \(-0.97\) in the case of \( \tau = 3 \) ps. Regression analysis showed that 94\% of the variation in \( \log(\text{SER}/A_{\text{diff}}) \) is explained by the change in \( Q_{\text{crit}} \). The remaining 6\% of the variation can be contributed to several effects, including the fact that an average width \( \tau \) is used for the current pulse, the fact that \( A_{\text{diff}} \) is used as a sensitive area in, whereas a 3-D collection surface would be more accurate, and the neglect of upsets due to the simultaneous collection of electrons at an NMOS drain and holes at a PMOS drain.

If hits at both the NMOS and the PMOS drains are taken into account, the following expression can be used to model the SER

\[
\text{SER} = \kappa \left[ A_{\text{diff,N}} \exp\left( -Q_{\text{crit,e}}/\eta_{\text{elec}} \right) + A_{\text{diff,P}} \exp\left( -Q_{\text{crit,h}}/\eta_{\text{hole}} \right) \right]
\]  

(3)

where \( A_{\text{diff,N}} \) and \( A_{\text{diff,P}} \) denote the NMOS and PMOS drain diffusion area, respectively. Both areas are extracted from the cell layout. The parameters \( \eta_{\text{elec}} \) and \( \eta_{\text{hole}} \) denote the charge collection efficiency for electrons and holes, respectively. Both parameters are obtained from least-squares fits.

Equation (3) was fitted to the experimental SER data with 0.9 \( \leq V_{\text{DD}} \leq 1.3 \) V. This voltage range is typical for the operation of 90-nm designs. Therefore, a model that is accurate within this range is required. The optimal parameters for the alpha-SER model were found to be \( \eta_{\text{elec}} = 1.58 \) and \( \eta_{\text{hole}} = 1.39 \) fC. Fig. 8 compares the modeled alpha-SER with the experimental results of Section III-B. The data points that were used in the fit are depicted by closed symbols, whereas the open symbols represent the other data points. The model agrees with the measured alpha-SER data within a factor of 2. For the experimental data obtained at \( V_{\text{DD}} = 1.2 \) V, the agreement is within 30\% or better. The only exception is formed by the SER of FF4 at the conditions where CLK = LOW. In that case, the model of (3) underestimates the SER by a factor of 2 or more. However, as was discussed in Section III-B, the alpha-SER of FF4 is very low if CLK = LOW.

The model of (3) was also fitted to the experimental neutron-SER data discussed in Section III-D. The resulting charge collection parameters are \( \eta_{\text{elec}} = 2.78 \) and \( \eta_{\text{hole}} = 2.45 \) fC. Except for FF4, CLK = LOW, the model agrees with the experimental neutron-SER values within a factor of 2. The agreement at \( V_{\text{DD}} = 1.2 \) V is at worst within 60\%, but generally within 30\%. Recall that the experimental error of the neutron-SER data, based on 90\% confidence limits, is 20\% or better. The larger values for the parameters \( \eta_{\text{elec}} \) and \( \eta_{\text{hole}} \) in the case of neutron-SER can be explained by the fact the neutron hits generally results in larger amounts of collected charge, which implies a weaker dependence on \( Q_{\text{crit}} \). The parameter \( \eta_{\text{elec}} \) is 13\%–14\% higher than \( \eta_{\text{hole}} \), both for alpha- and for neutron-SER. This can be explained by the higher mobility of electrons compared to holes. For FF4, CLK = LOW, the model does not agree too well with the (very) low experimental SER data. Apparently, a further refinement of the model would be needed to accurately predict the SER in this regime also.

It is important to note that if a current pulse with a small pulsewidth is assumed in the model, than both electron pulses, at the drain junctions of NMOS transistors, and hole pulses, at the drains of PMOS transistor, must be taken into account. This is because in some cases one of the two pulses may not result in an upset. For example, for FF1, \( Q_{\text{crit,e}} \), due to electron pulses, is infinitely large for pulses with \( \tau \leq 5 \) ps if Data = 1, both for CLK = HIGH and CLK = LOW, see Fig. 9. This can be explained by the asymmetry in the FF designs. Some of the inverters in the feedback loops are relatively weak and have a large output capacitance. The RC time in the case of a signal transition is then relatively long. If a narrow pulse disturbs the input, due to charge collection, the output is not able to respond quickly enough and the change in the output voltage does not exceed the critical value for an upset. At \( \tau = 3 \) ps in many cases a large difference between \( Q_{\text{crit,e}} \) and \( Q_{\text{crit,h}} \) is observed for the FFs considered in this paper. In some cases one of the two is infinitely large, as is shown in Figs. 9 and 10. Therefore, if we assume a relatively small average pulsewidth, in general, the majority of the FF upsets is either due to electron or to hole collection.
B. Process Variations

Freeman [20] showed in 1996 that process variations can have a significant effect on the $Q_{\text{crit}}$ of bipolar SRAM arrays and, consequently, on their SER. Recently, one of the authors of the current paper reported alpha-SER data that demonstrated the major impact of process variations in contemporary CMOS technologies [16]. Instances from the same SRAM compiler on different chips processed in the same technology showed the average variation of 40% (0.18-$\mu$m SRAM) and 35% (0.13-$\mu$m SRAM). For the 0.18-$\mu$m SRAM, also batch-to-batch variations of 12% on average were observed. The 0.13-$\mu$m SRAM showed average batch-to-batch variations of 16% and additional sample-to-sample variations, typically of 5%. Statistical $Q_{\text{crit}}$ simulations combined with an analytical SER model showed a theoretical 3× spread in the SER of 0.18-$\mu$m SRAMs. This spread corresponds to the difference in SER between the worst case ($-3\sigma$) process variations at the slow process corner and the best case ($+3\sigma$) variations at the fast corner.

In the previous work, the alpha-SER distribution was modeled for FF1 for the states CLK = HIGH, Data = 1 and CLK = HIGH, Data = 0. [8]. Five different process corners were included in the analysis: nominal (NOM), slow-N, slow-P (SNSP), fast-N, fast-P (FNFP), slow-N, fast-P (SNFP), and fast-N, slow-P (FNSP). It was shown that for Data = 1 the SER distributions for the SNFP and FNFP corners are between the NOM distribution, on the one hand, and the FNFP and SNSP distributions, respectively, on the other hand. However, for Data = 0, the SNFP and FNFP distributions almost overlap with the NOM distributions. The difference was explained by the variation in transistor size in the FF. As a result, the stabilization of the node charges by pull-up and pull-down transistors is different for each of the FF states.

In [8], first the statistical spread in $Q_{\text{crit}},e$ was calculated applying a current pulse with a width of $\tau = 90$ ps. Then, the alpha-SER was modeled using the analytical model of [18]. Each of the applied models was calibrated with the experimental data of the FF state under consideration. However, it was demonstrated in Section IV-A that the agreement between this model and the experimental FF SER data is relatively weak. We obtained a better model if hits at both the NMOS and the PMOS drains are included. Also, using a pulselength of $\tau = 3$ ps in the critical charge calculations results in a better correlation between SER and $Q_{\text{crit}}$. In [21], it was shown for SRAMs that the pulselength has a large impact, not only on $Q_{\text{crit}}$ itself, but also on the effect on $Q_{\text{crit}}$ of variations in the transistor model parameters. In this paper, we study in detail the effect of the pulselength on the statistical distribution of the SER of 90-nm FFs.

The computational details for calculating the SER distributions have been discussed in detail elsewhere [16]. The statistical spread in $Q_{\text{crit}},e$ and $Q_{\text{crit}},h$ was computed with a SPICE-like simulator, applying a Monte Carlo algorithm to include variations in the transistor parameters due to process variations. The theoretical results are depicted in Fig. 11. The distributions for pulselengths of $\tau = 3$ and 90 ps are compared for the states CLK = HIGH, Data = 1, and CLK = HIGH, Data = 0 of FF1. Along the $y$-axis is the density of the probability that a sample, processed in the specified corner, has a given alpha-SER.

1) $\tau = 3$ ps: Fig. 11 shows that the SER distributions in the CLK = HIGH, Data = 1 state, for the case that $\tau = 3$ ps, almost overlap for the NOM, FNFP, and SNSP corners, whereas the average SER is slightly lower for FNSP and somewhat higher for SNFP. In this state, $Q_{\text{crit}},e$ is infinitely high if $\tau = 3$ ps, as is shown in Fig. 9. Therefore, all soft errors are caused by the collection of holes by drain junctions of PMOS transistors. This hole collection results in an upward glitch in the voltage level of the storage node connected to the PMOS drain. Because the same model was used to compute the SER, the differences in the five distributions are caused by variations in $Q_{\text{crit}}$. Different contributions to $Q_{\text{crit}}$ are affected differently by the process variations. Fig. 11 shows that the net effect is a lower average SER for FNFP corner and a higher average SER for the SNFP corner, whereas in the SNSP and FNFP corners the variations counterbalance each other, resulting in SER distributions that practically overlap with the NOM distribution.

The situation is different for the CLK = HIGH, Data = 0 state if $\tau = 3$ ps. Fig. 11 shows that in this case the SNSP and FNFP distributions overlap and have an average SER that is approximately 5% lower compared to the NOM corner. Also, the FNFP and SNFP corners show almost overlapping distributions with on average 5% higher SER than the NOM corner. In this situation, practically every soft error is caused by the collection of electrons by an NMOS drain junction, because $Q_{\text{crit}},e$ is much smaller than $Q_{\text{crit}},h$ in this state of FF1 if $\tau = 3$ ps. This electron collection results in a downward glitch in the voltage level of the storage node connected to the NMOS drain. Again, the differences in the SER distributions are caused by variations in $Q_{\text{crit}}$, which result from the combined effect of process variations on the individual contributions to $Q_{\text{crit}}$. Both for Data = 1 and for Data = 0 the spread within the distribution for a given process corner is larger than the differences between the averages for the individual corners. Therefore, sample-to-sample variation is more important here than the impact of the different process corners.
Fig. 11. Statistical variation in alpha-SER for the states CLK = HIGH, Data = 1, and CLK = HIGH, Data = 0 of FF. Analytical SER models of the form of (3) have been used, assuming pulsewidths of τ = 3 and 90 ps.

2) τ = 90 ps: The right-hand side of Fig. 11 shows the results for the case where τ = 90 ps. These data were calculated using a model of the form of (3), with $Q_{\text{crit},e}$ and $Q_{\text{crit},h}$ computed applying a current pulse with a width of τ = 90 ps. The model was fitted to the experimental alpha-SER results as was discussed in Section IV-A for the case of τ = 3 ps. The accuracy of the model for τ = 90 ps is not as good as for τ = 3 ps, as was discussed in Section IV-A. This is reflected by the average SER of the NOM corner, which is systematically too low compared to the results for τ = 3 ps and to Fig. 1. However, the relative differences are more important here than the absolute SER values.

Comparing the resulting SER distributions with the data for τ = 3 ps shows that in the case of τ = 90 ps the overall spread in SER is much larger for the CLK = HIGH, Data = 1 state this overall spread is about one order of magnitude. This implies that experimental SER measurements would show significant sample-to-sample variations. In practice, the typically observed sample-to-sample spread is less than 5%. Note, however, that all measured samples were from the same batch and that therefore effects from different process corners are not included in the experimental results. The fact that large variations are not observed provides an additional argument that it is unlikely that the typical width of the induced current pulse is near τ = 90 ps.

The critical charge, in the case of electron collection, can be approximated by the expression

$$ Q_{\text{crit}} \approx Q_{\text{node}} + I_{\text{P,ON}} w_{\text{pulse}} $$

where $Q_{\text{node}}$ is the nodal charge of the disturbed storage node, $I_{\text{P,ON}}$ denotes the ON-current of the pull-up transistor, and $w_{\text{pulse}}$ is the width of the current pulse. With the help of (4), it is possible to relate $Q_{\text{crit}}$ to the properties of the cell ($Q_{\text{node}}$ and $I_{\text{P,ON}}$) and of the current pulse disturbing the storage node ($w_{\text{pulse}}$). A previous study showed that (4) is a fairly accurate approximation to the $Q_{\text{crit}}$ as obtained from SPICE-like simulations and also that (4) is useful to study the sensitivity of $Q_{\text{crit}}$ to variations in individual transistor parameters [21]. For large pulsewidths, the $I_{\text{P,ON}} w_{\text{pulse}}$ term dominates $Q_{\text{crit}}$. The spread is then primarily due to the effect of process variations on $I_{\text{P,ON}}$, which effect is relatively large. As a result, the variation in $Q_{\text{crit}}$ and, consequently, in SER is larger if a wider pulse is regarded.

Furthermore, the order of the five SER distributions is different than in the case of τ = 3 ps. This is because not only the stabilization of the struck node is important, but also the stabilization of the opposite node in the feedback loop [21]. In the state CLK = HIGH, Data = 1, a “fast” NMOS transistor relatively effectively stabilizes a storage node disturbed by the collection of holes. For such wide current pulses, the impact of process variations is particularly important for the pull-up and pull-down transistors that stabilize the node charges. A “fast” NMOS transistor has a relatively high current drive and, consequently, a relatively large pull-down strength. However, this effect is partially counterbalanced if a relatively “slow” PMOS transistor pulls up the opposite node in the feedback loop. Similarly, in the CLK = HIGH, Data = 0 state the effect
of a “fast” PMOS transistor stabilizing a disturbed node is compensated by a “slow” NMOS transistor pulling down the opposite node in the feedback loop. The argument used in [8] that the disturbed node is driven by a relatively large inverter in the CLK = HIGH, Data = 1 state and by a relatively small inverter in the CLK = HIGH, Data = 0 state is not valid here, because we assume that if CLK = HIGH, Data = 1 the soft error is caused by the collection of holes, which implies that the same storage node is disturbed as in the case of CLK = HIGH, Data = 1, where electrons are collected.

The results presented in this section demonstrate that the width of the applied current pulse has an important effect on the resulting SER distribution. Not only is the overall spread much larger if a wider current pulse is used, also, the ordering of the distributions for the five process corners changes. For example, in the CLK = HIGH, Data = 0 state the FNFP corner has the highest average SER if τ = 3 ps, but the lowest SER if τ = 90 ps. This result shows that information on both the effective current-pulsewidth and on the process corner is important when analyzing soft-error sensitivity.

V. DISCUSSION

A. Technology Scaling

The alpha-induced SER results obtained in this paper have been combined with alpha-SER data from 0.18- and 0.13-µm technologies [18] to derive the scaling trends given in Fig. 12. The SER per bit is shown as a function of technology node both for FFs and for (unprotected) SRAM. For the FF SER, both the average over the four states and all tested FFs is shown and the worst value is shown for to the four states and the five FFs that are considered in this paper.

The SER data in Fig. 12 are expressed per bit. If the SER per square millimeter were considered, the values would be much higher for SRAM than for FFs, because the area of an FF cell is typically an order of magnitude larger than of an SRAM cell. The SER per square millimeter increases with technology scaling, both for FFs and for SRAMs, due to the ongoing reduction in feature size [16], [17].

In this paper, the neutron-induced SER was studied for FFs in a 90-nm process only. However, in [26], the neutron-SER of static latches was predicted to stay approximately constant with technology scaling, provided that VDD scales only moderately. Since the neutron-induced SER of SRAMs is found to decrease, it is very likely that the neutron-SER of FFs will grow more slowly than the alpha-SER, or even stay constant or decrease also.

B. Neutron-SER to Alpha-SER Ratio

Fig. 13 shows the alpha- and neutron-induced components to the SER for FFs and for SRAMs in the investigated 90-nm technology. The neutron-induced SER of SRAMs is the average of several instances on 90-nm test vehicles that were tested at the Weapon Neutron Research facility at Los Alamos. Tests on SRAMs demonstrated that the neutron-SER measured at Los Alamos is typically 25% higher than the SER measured at the TRIUMF facility, which is in agreement with results reported in [10]. Because the Los Alamos facility is regarded as a de facto standard in the industry, the neutron-induced FF SER was multiplied by a factor of 1.25 in Fig. 13. The average neutron-SER for FFs is approximately 4/3 as high as for SRAMs, whereas the average alpha-SER is 2.3× as high. Furthermore, the range in neutron-SER is smaller than in alpha-SER, because of the larger collected charges in the case of neutron hits, as discussed above.

Table II shows the average neutron-SER to alpha-SER ratios for both FFs and SRAMs in 90-nm. The results from this paper are compared with the data from [27] for the same between the worst and average FF alpha-SER is equal to 2.8×, 3.9×, and 3.1× for the 180-, 130-, and 90-nm processes, respectively. For the 0.13-µm node only a single FF design was investigated [24]. The observed alpha-SER showed an extreme data- and clock-state dependence, resulting in the relatively high worst/average ratio for the FF alpha-SER, which is close to the theoretical maximum of a factor of 4.

Our results contradict estimations reported elsewhere [17], [25] that predicted that at the 90-nm node the SER/bit of an FF is still significantly lower than of an SRAM cell. Most likely, the discrepancy is caused by differences in design style. FF functionality can be implemented in many different ways. The circuit topology and transistor sizes are optimized for the typical applications for which the FF designs will be used. Although the FF from a different library (FF3) did show a similar average SER as the other FFs, it is reasonable to assume that design style has a major impact on FF SER. For SRAM cells this is not the case because the design space is much more limited. Therefore, the variation in SER between SRAM cells within a given technology node is much smaller than between FF cells.

The neutron-induced SER of FFs in the 90-nm technology is approximately 25% higher than the SRAM SER, because the area of an FF cell is typically an order of magnitude larger than of an SRAM cell. The SER per square millimeter increases with technology scaling, both for FFs and for SRAMs, due to the ongoing reduction in feature size [16], [17].

In this paper, the neutron-induced SER was studied for FFs in a 90-nm process only. However, in [26], the neutron-SER of static latches was predicted to stay approximately constant with technology scaling, provided that VDD scales only moderately. Since the neutron-induced SER of SRAMs is found to decrease, it is very likely that the neutron-SER of FFs will grow more slowly than the alpha-SER, or even stay constant or decrease also.

Table II shows the average neutron-SER to alpha-SER ratios for both FFs and SRAMs in 90-nm. The results from this paper are compared with the data from [27] for the same...
technology node. It is clear that the ratios that we observe are significantly lower. However, we extrapolate the alpha-SER data to a nominal flux of 0.001 $\alpha$/h $\cdot$ cm$^2$, whereas [27] applied product alpha fluxes, which values were not reported. In addition, there are differences in process technology and in design style. Whereas the process and circuit designs studied in [27] have been optimized for high-performance microprocessors, in the current work we consider a Crolles2 Alliance 90-nm process and corresponding libraries that are dedicated to low-power applications. The difference between the results of this paper and the data from [27] is larger for FFs than for SRAMs. This can be explained by the larger freedom in the design of FF cells, as was discussed above.

The relative importance of the alpha- and neutron-induced SER contributions strongly depends on the use conditions. On the one hand, neutron-SER will generally be dominant at flight altitudes, where the cosmic-neutron flux is roughly two orders of magnitude higher than at terrestrial altitudes. On the other hand, the alpha-SER may be dominant at sea level, particularly if the IC package has been manufactured from less highly purified materials. As an example, consider the component SER (i.e., without inclusion of logical and timing derating factors) of a product IC containing 10 Mb of SRAM and 100k FFs, using the 90-nm SER data presented in this paper. Table III shows the difference in the neutron-SER to alpha-SER ratios for two extreme cases. In the first situation the product is applied at zero altitude and the nominal alpha flux corresponds to the level of a standard package, i.e., with no special measures taken to reduce the alpha flux. In the second situation, the product is applied at a flight altitude and the alpha flux is at approximately the lowest level that can be achieved nowadays at an acceptable cost. The neutron-SER to alpha-SER ratio differs with almost four orders of magnitude for these two situations.

### VI. Conclusion

We have presented experimental alpha- and neutron-induced SER data for 90-nm FFs. We found that the alpha-induced SER contribution is larger than the neutron-SER component when the experimental data are extrapolated to nominal conditions at sea level. This result shows that in sub-100-nm technologies not only cosmic neutrons but also alpha particles, emitted by radioactive impurities, have a significant contribution to the SER, both for SRAMs and for FFs.

Furthermore, we have derived an analytical SER model that is based on simulated critical charges and is calibrated with experimental SER data. The model includes the contributions from two types of upsets: those that are caused by the collection of electrons and those that are caused by the collection of holes. For both types of upsets a critical charge is defined, which is calculated using circuit simulations in which the charge collection is modeled with a current pulse. The width of the pulse is determined by a timing parameter $\tau$. If a relatively narrow pulse is applied ($\tau = 3$ ps) the correlation with the experimental SER data is much better than if a wide pulse ($\tau = 90$ ps) is used. This result implies that drift of the particle-induced charges in the electric fields is the dominant charge collection mechanism and that diffusion is less important. The agreement between the model (for $\tau = 3$ ps) and the measurements is excellent: 94% of the variation in the experimental results is explained by the change in $Q_{\text{crit}}$. The SER model agrees with the measured SER data within a factor of 2 or better.

Our results show a clear correlation between the FF SER, on the one hand, and the cell type, data state, and clock state, on the other hand. In addition, we demonstrated with modeling results that there is a strong correlation between SER spread and process variations. The applied timing parameter $\tau$ of the...
current pulse has a strong impact on the SER distributions that result from the model.

Next to the other design metrics, the SER of the FF cell is one of the points of concern when designing in sub-100-nm CMOS technologies. The clock state dependence is particularly important if the IC is in a state-retention mode in which the clock is frozen. For example, for one of the investigated cells (FF4) the difference in SER for the two clock states is approximately a factor of 20.

Averaged over the data and clock states, the SER varies with only 30% for the investigated FFs. Therefore, in many applications the choice of an FF type from a standard-cell library will not have a major impact on the SER at the chip level. If the contribution from FFs to the chip SER has to be reduced significantly, radiation-hardened cell designs or other mitigation techniques should be applied.

Finally, our experimental results show that in 90-nm, the FF SER per bit exceeds the typical SRAM SER per bit. Combined with the large variations in the FF data, this implies that in general FFs cannot be neglected when the SER of an IC design is estimated and that the characterization of FF SER is necessary at the 90-nm technology node and beyond.

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