Fabrication of large-scale mono-crystalline silicon micro-mirror arrays using adhesive wafer transfer bonding

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ABSTRACT

Today, spatial light modulators (SLMs) based on individually addressable micro-mirrors play an important role for use in DUV lithography and adaptive optics. Especially the mirror planarity and stability are important issues for these applications. Mono-crystalline silicon as mirror material offers a great possibility to combine the perfect surface with the good mechanical properties of the crystalline material. Nevertheless, the challenge is the integration of mono-crystalline silicon in a CMOS process with low temperature budget (below 450°C) and restricted material options. Thus, standard processes like epitaxial growth or re-crystallization of poly-silicon cannot be used. We will present a CMOS-compatible approach, using adhesive wafer transfer bonding with Benzocyclobutene (BCB) of a 300nm thin silicon membrane, located on a SOI-donor wafer. After the bond process, the SOI-donor wafer is grinded and spin etched to remove the handle silicon and the buried oxide layer, which results in a transfer of the mono-crystalline silicon membrane to the CMOS wafer. This technology is fully compatible for integration in a CMOS process, in order to fabricate SLMs, consisting of one million individually addressable mono-crystalline silicon micro-mirrors. The mirrors, presented here, have a size of 16 x 16 µm². Deflection is achieved by applying a voltage between the mirrors and the underlying electrodes of the CMOS electronics. In this paper, we will present the fabrication process as well as first investigations of the mirror properties.

Keywords: Optical MEMS, micro mirrors, spatial light modulator, adhesive bonding

1. INTRODUCTION

Today, spatial light modulators (SLMs) are used in projection display systems [1], adaptive optics and also in advanced lithography. Especially the last item demands for very accurate micro-mirror arrays [2],[3], which have perfect mechanical and optical properties. They are used for instance in DUV lithography systems showed in fig. 1. Therefore an analogue movement of every single micro-mirror is required, realized by an underlying CMOS driving circuit.

As the temperature impact for CMOS-electronics is limited by approximately 450 °C, only low temperature process steps can be used for the mirror fabrication. Thus, the formation of mono-crystalline silicon membranes using high temperature processes, e.g. epitaxy must be excluded. The approach presented here, is based on the transfer of thin mono-crystalline silicon membranes from a donor wafer to the CMOS wafer, using a low temperature adhesive bond process. The micro-mirror array consists of 1 million silicon micro-mirrors with a pitch of 16 x 16 μm^2.

The basic technological concept was already presented by Niklaus et. al. in 2003 [4]. Based on these first results, technology improvements have been attained. This involves the transfer of the basic technology from a 4 x 4 mirror array to a 2048 x 512 mirror array, which can be directly integrated onto a CMOS substrate and the improvement of the bond interface using Benzocyclobutene (BCB). Furthermore, the post formation was changed from gold to aluminium alloys due its better compatibility to the CMOS process.

The use of mono-crystalline silicon as mirror material has several advantages. Especially for lithography applications (e. g. mask writing) in the DUV (deep ultra violet) region, as described here, the accurate and repeatable positioning of each individual mirror must be perfect. Advantageous mirror properties are thus a high elasticity, low internal or compensated stress gradients and no material plasticity. Beyond already used materials like SiGe or aluminium alloys, mono-crystalline silicon fulfils almost all specifications perfectly. Thus, highly planar mirrors without material degradations

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can be expected using mono-crystalline silicon. Due to the good surface quality of the silicon membranes, mirrors with a very small surface roughness can be fabricated.

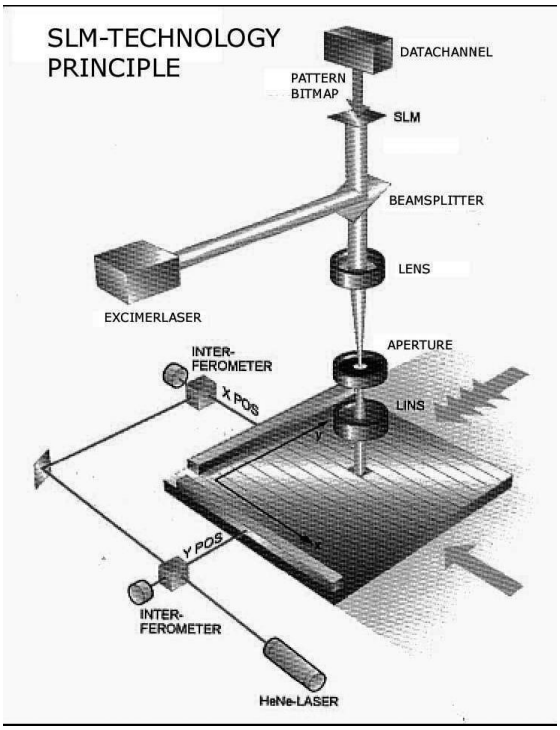

Fig. 1. Principal drawing of a mask writing system using spatial light modulators (picture provided by Micronic Laser Systems)

1.1 Working Principle

The principle drawing of one single micro-mirror is shown in fig. 2. It contains of a counter and an address electrode under each side of the mirror. Applying a voltage between address electrode and mirror results in a deflection of the mirror to the address electrode. Reason for this movement is the electrostatic force [3], which tends to decrease the capacitance (in this case the distance) between mirror and address electrode. The deflection is stopped by the bending moment of the mirror spring, resulting in a comparable but reverse orientated force. For small distances between mirror and electrode, the deflection can be calculated by good approximation with $d \sim U^{2.3}$, considering that the best exponent in this case depends of course also how close the deflection comes to the pull in point.

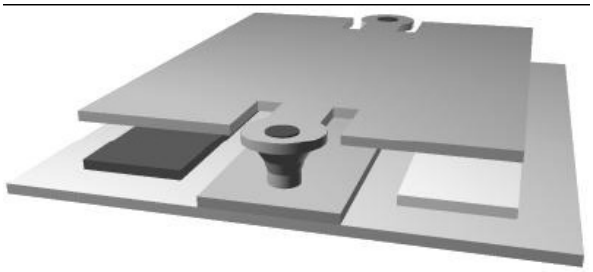

Fig. 2. Principal drawing of a micro-mirror, showing the mirror and the two bottom electrodes

2. FABRICATION

2.1 Process Flow

The fabrication process of mono-crystalline silicon mirrors [fig. 3], using adhesive wafer transfer bonding, started with a CMOS wafer and a SOI wafer as base material. The CMOS wafer contained already all process steps for the complete electrical functionality. On top, the metal layer to build the address and the counter electrode was deposited and structured in a last fabrication step. The SOI wafer on the other hand had a buried oxide thickness of 1000nm and a device silicon membrane of approximately 300nm.

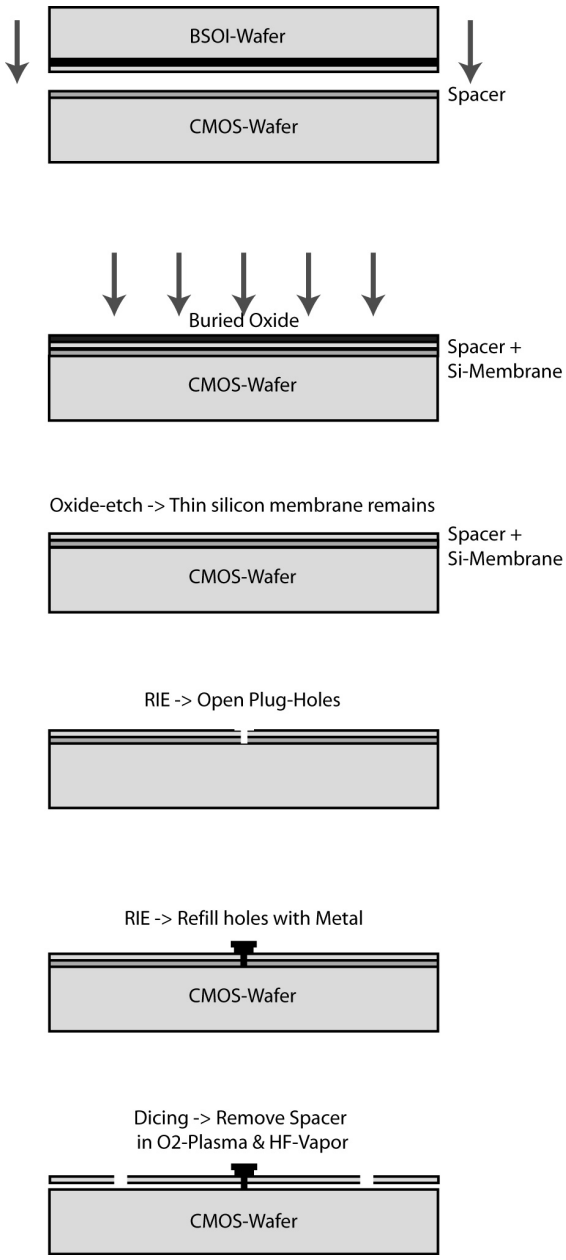

Fig. 3. Process flow for the fabrication of mono-crystalline silicon micro-mirrors using adhesive wafer transfer bonding

In a first step, an oxide was deposited on the top metal layer of the CMOS wafer and polished in a chemical mechanical polishing (CMP) step. Then the 150nm thin Benzocyclobutene (BCB) layer was spin coated. With a temperature step at 160°C, the BCB layer was pre-cured and so ready for bonding. The SOI-wafer was turned over and bonded with the CMOS wafer. Therefore a process temperature of 270°C and a maximum pressure of 20kN were used.

In a further step the handle silicon of the SOI wafer was removed using a grinding and a spin etch step, stopping in the buried oxide layer. This resulting layer was removed using buffered hydrofluoric acid. Thus the transfer of the 300nm thin mono-crystalline silicon membrane to the CMOS wafer was accomplished.

To pin the silicon membrane to the CMOS wafer, small plug holes were etched through the silicon membrane and the BCB combined with the oxide spacer material. The required alignment to the CMOS wafer could be done, because the thin silicon membrane and also the spacer material had enough transparency. The etching stopped on a metal electrode of the CMOS, used for electrical connection of the silicon mirror.

The hole was filled with an aluminium alloy by sputtering. The metal layer was structured using a dry etch step with a chlorine plasma, resulting in metal posts, connecting the silicon membrane with the CMOS wafer.

In a next step, the silicon membrane was structured using a dry fluorine-based etch process, stopping in the underlying BCB bond layer. Thus, the mirror shape and also the mirror springs were defined.

Finally the chips were diced and the spacer material between mirror and CMOS surface was removed using a combination of oxygen plasma and hydrogen fluoride gas.

2.2 Bonding process development

To insure the adhesive bond quality of thin BCB layers, several investigations have been made using two different thicknesses of 150nm and 500nm. Important to reach reliable and reproducible results, parameters like the percentage of crosslinked polymer during the pre-cure, the bond temperature and the bond pressure had to be analyzed. Furthermore the use of a graphite foil to secure a homogenous distribution of the bonding force was tested. The results were evaluated, investigating the bond interface with an infrared (IR) lamp, measuring the bond interface by scanning accustic microscopy (SAM) and measuring the bond strength. The bond strength was calculated using the razor blade method [fig. 4], firstly presented by Maszara et. al [5].

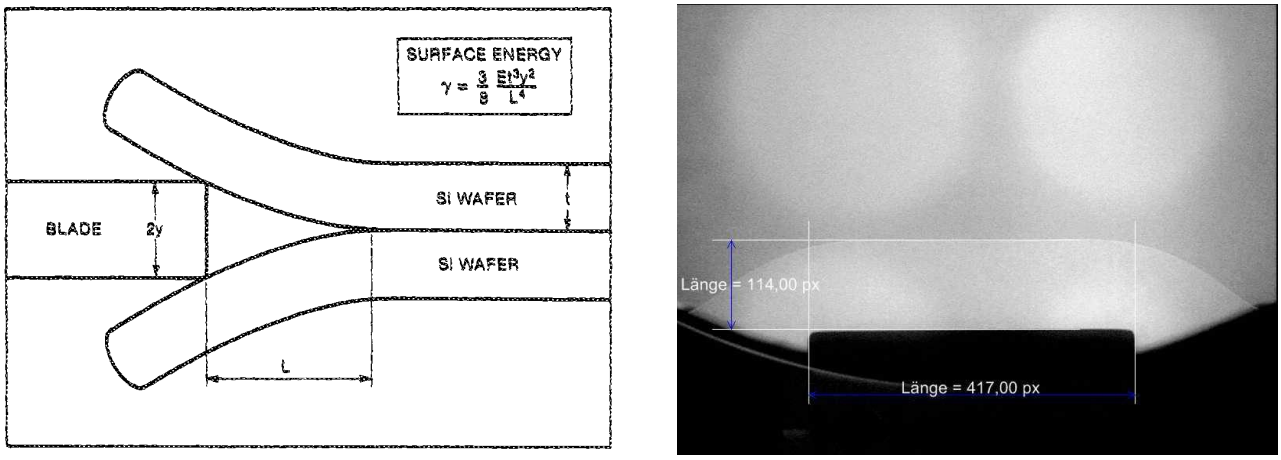

Fig. 4. [left] Principle drawing describing the razor blade method (Maszara et. al. [5])

[right] Picture made with an IR-lamp; on the bottom the inserted razor blade; Measurement of the crack length was accomplished referencing on the length of the razor blade

This method was developed to measure the surface energy of materials without plastic deformation (e.g. silicon-to-oxide bonds). Although the BCB is completely crosslinked during the bonding process, this formula can only be used in rough approximation by

$$\gamma = \frac{3}{8}\frac{Et^3 y^2}{L^4} \tag{1}$$

with γ the surface energy, E the modulus of elasticity, t the wafer thickness, 2y the blade thickness and L the crack length.

All tests concerning the adhesive bond development with BCB were made with silicon wafers. The wafers were bonded in a Süss SB6E bonding tool, applying a maximum temperature of 270°C and a maximum pressure of 20kN. This was done, because bare silicon wafers are less expensive than CMOS wafers and they are transparent for IR illumination, which is not the case for CMOS wafers containing metal layers and highly doped areas. As CMOS wafers are polished several times during the fabrication, the use of bare silicon wafers is comparable to the condition in the real process.

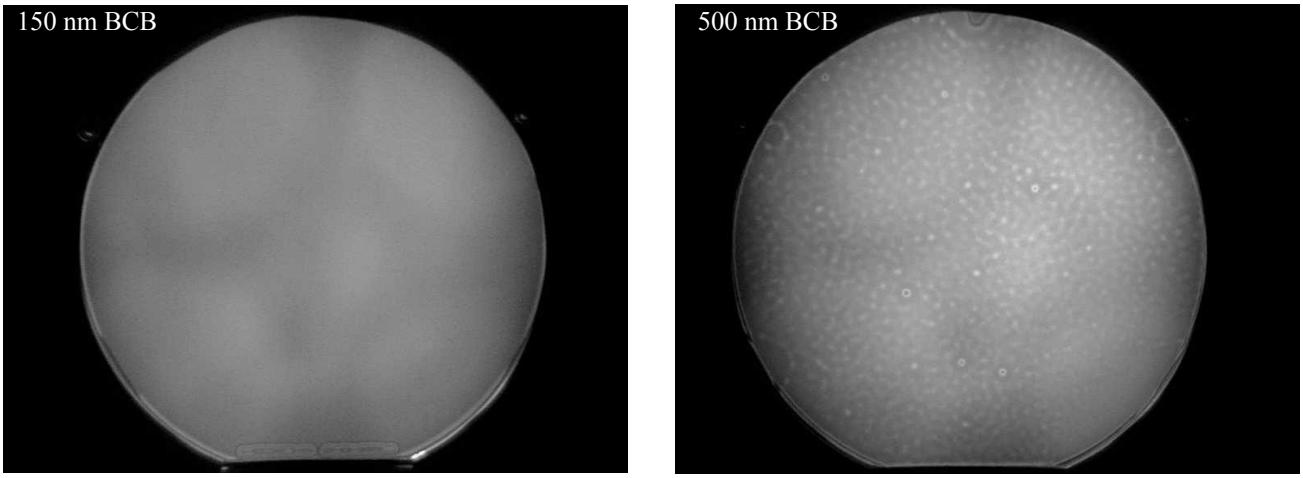

Fig. 5. Pictures of BCB bonded silicon wafers using an IR-lamp. On the left side, wafers bonded with a 133nm BCB layer, on the right side with 470nm. The bond process was adapted for thin BCB layers (homogenous result). The right picture shows gas bubbles in the interface, caused by outgassing during the crosslinking process of BCB.

Results of adhesive bonds with thin BCB, investigated by an IR-lamp are shown in [fig. 5]. The bond program was optimized for 150nm BCB layers [left], as this thickness was also used in the fabrication process. For comparison, BCB layers of 500nm [right] were also analyzed. The deposition was performed by a spinning process, resulting in very homogenous thicknesses across the wafer, although the overall thickness differs by 16nm [fig. 6]. Every value was the average of nine measured positions, which were equally distributed over the wafer surface. As can be seen, the bond process showed very homogenous results for BCB layers of 150nm, whereas bonded wafers with 500nm thick BCB layers showed gas bubbles in the bond interface. This was caused by the outgassing during the crosslinking process of the BCB. As thicker BCB layers contain certainly more gas, it cannot diffuse completely through the BCB layer, before the crosslinking process is accomplished. Thus, for the use of thicker BCB layers, the bond process must be adapted, increasing the time before the wafers are brought into contact.

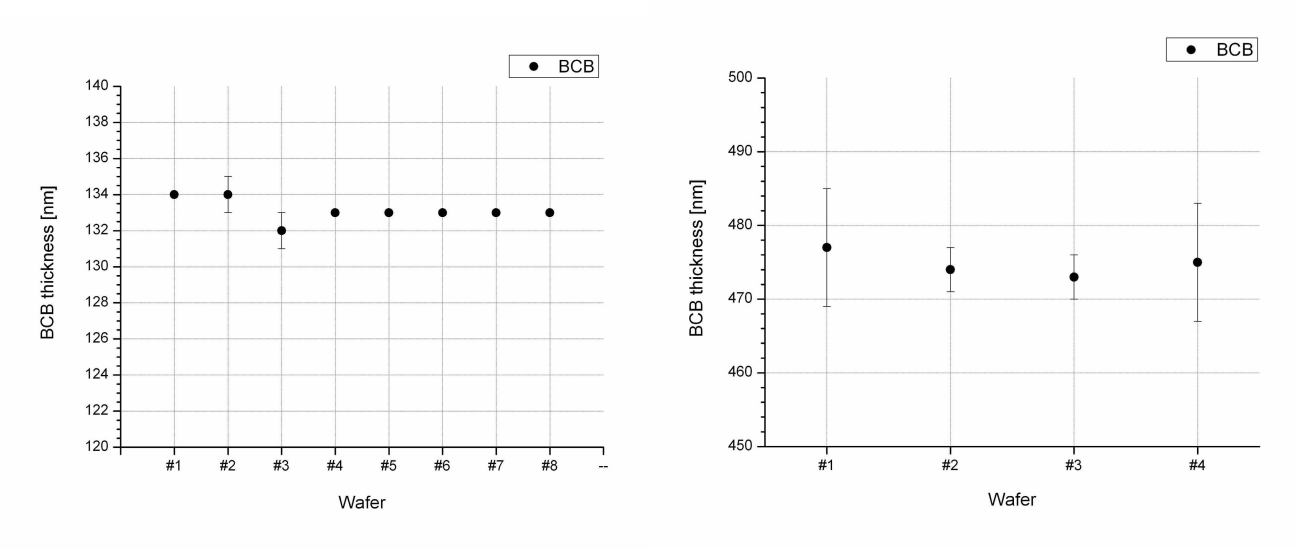

Fig. 6. Measurements of the BCB thickness homogeneity after spin-coating using two difference thicknesses; each point is the average of nine measurements points, distributed over the wafer surface. The deviation is less than 1% for 133nm thick BCB layers, less than 2% for 475nm BCB layers.

The crack length as indicator of the bond strength was measured for each wafer pair (using the razor blade method), which was already investigated with the IR lamp. Results are presented in [table 1]. As mentioned before, the calculation of the surface energy is not exact, as it assumes bonded wafers with no plastic deformation. This is not given for wafers bonded with BCB. Therefore, results for the bond strength can only be seen as qualitative results. Calculations showed, that the surface energy of BCB bonded wafers results in values of ~4.8J/m^2, which would lie by a factor of 2 over the results for high tempered silicon-to-oxide bonds. Nevertheless, this measurement is seen as the best possibility to monitor the bond strength homogeneity in an easy and fast way. For the interpretation of the measured results, only the crack length was regarded as qualifying and comparable parameter. Investigations of the fabrication process showed, that BCB bonded wafers with a crack length of less than 16mm have sufficient bond strength to withstand the mechanical impact during the process. Results presented here show a crack length of only 10mm with a deviation of less than 0.5mm.

Bonded wafer	BCB thickness (avg.) in nm	BCB Thickness (dev. over wafer) in nm	crack length in mm
1	133	1	10,2
2	134	0	10,2
3	133	0	10,2
4	133	1	10,3

Table 1. Crack length measured with the razor blade method of four different wafers. The crack length shows very homogenous results, indicating a stable bond strength and a stable bond process.

Due to these good results, an improvement using a thin graphite foil could not be identified. Former investigations showed however, that using a graphite foil between chuck and wafer can improve the distribution of pressure during the bond process.

To complete the investigation of adhesive bonded wafers using BCB, they were measured with a scanning accustic microscope (SAM). Despite of some single and small defects, the results already got from the infra-red inspection were confirmed [fig. 7].

Fig. 7. SAM-picture of a bonded silicon wafer using a 133nm BCB layer. The picture shows no defects in the bond interface. The black part on the upper side of the wafer results from the delamination by the razor blade test, done before the SAM investigation. Delamination at the bottom is caused by the wafer label.

2.3 BCB release

For the release of the BCB and oxide in the last fabrication step, it must be considered, that BCB contains constituents of silicon. Therefore, a CF_4/O_2 plasma etch was used. Results of released micro-mirrors using this etch process are shown in [fig. 8]. It can be seen, that butterfly-like BCB residues remained under the mirror, which couldn't be removed, even after a three times longer plasma etch step. A further increase of the etch time was not possible, as CF_4 attacks also the silicon micro-mirror and thus will lead to an undesirable damage.

For this reason, the release etch was changed to a pure O_2 plasma etch. In this process all organic BCB constituents were ashed. The remaining silicon constituents were simultaneously oxidized, resulting in silicon-oxide residues after the ashing process step [fig. 8]. The investigation was done using an energy dispersive X-ray spectroscopy (EDX), which couldn't detect any carbon-based residues after the O_2 plasma step, but only silicon oxide. In a second step, all BCB residues and also the remaining oxide spacer could be removed using hydrogen fluoride gas. As hydrogen fluoride gas is highly selective to silicon and metal, the attack on the silicon membranes and the electrodes during the release process was reduced to a minimum.

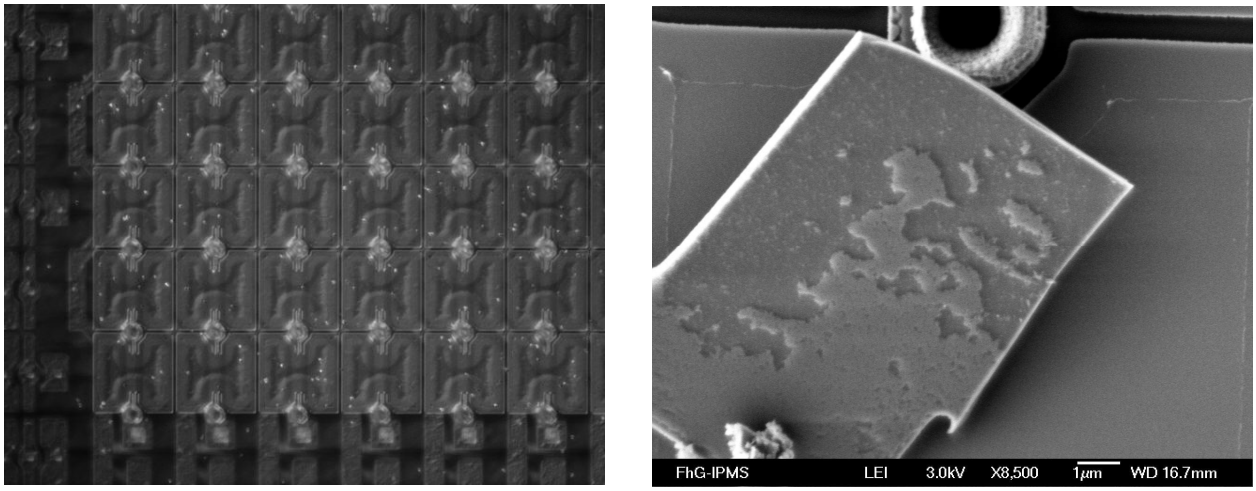

Fig. 8. [left] Micro-mirror array after using a CF_4 plasma to etch the underlying BCB layer with butterfly-like residues.

[right] Silicon oxide residues on the micro-mirror backside after treatment of the BCB layer with an O_2 plasma

3. RESULTS AND MEASUREMENTS

Investigations of fabricated micro-mirrors have been made on passive structures. These passive micro-mirror arrays contained only the top CMOS-metal layer, not the complete CMOS wafer. The process is still comparable to the micro-mirror fabrication on CMOS, but it's less expensive and time-consuming.

Fig. 9 shows a post hole, etched through the silicon membrane and the BCB / silicon oxide spacer material. The walls of the hole form a slight slope, which support the metal filling of the post. The etch process provides furthermore continuous walls, which show no under-etch in the lateral dimension. On the right side of fig. 9, a microscope picture of the micro-mirror array before dicing and release etch is presented.

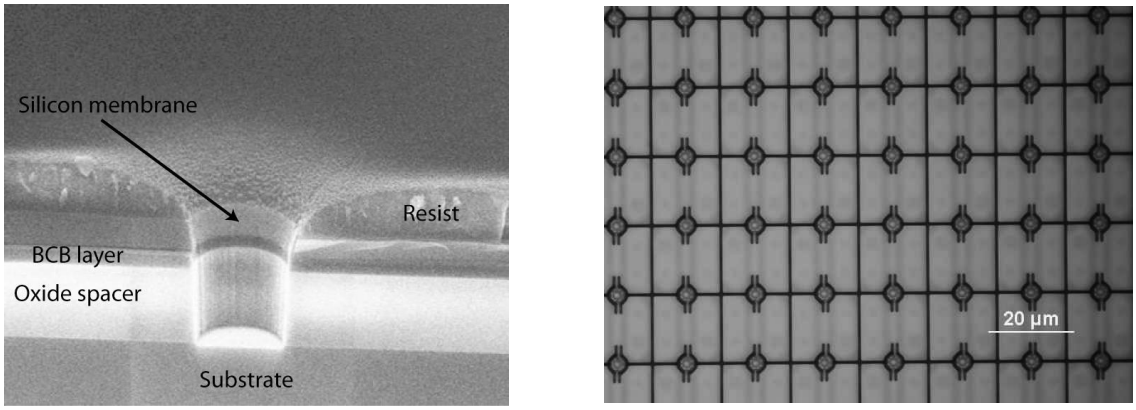

Fig. 9. [left] Picture of a post hole etched in silicon, BCB and oxide spacer. [right] Picture of the silicon mirror array before dicing and the release step

In fig. 10 the deflection versus the applied voltage of a micro-mirror is shown. The deflection shows an exponential dependence to the voltage. In these measurements, the applied voltage was limited to 16V with a maximum deflection of 55nm. Furthermore, the long-term stability as indicator for the level of drift was also analyzed [fig. 10]. Therefore, the mirrors were actuated with 15V over 60 minutes and measured with white light interferometry. Over this time, the mirrors showed almost no changes, the difference of the deflection was approximately 1nm.

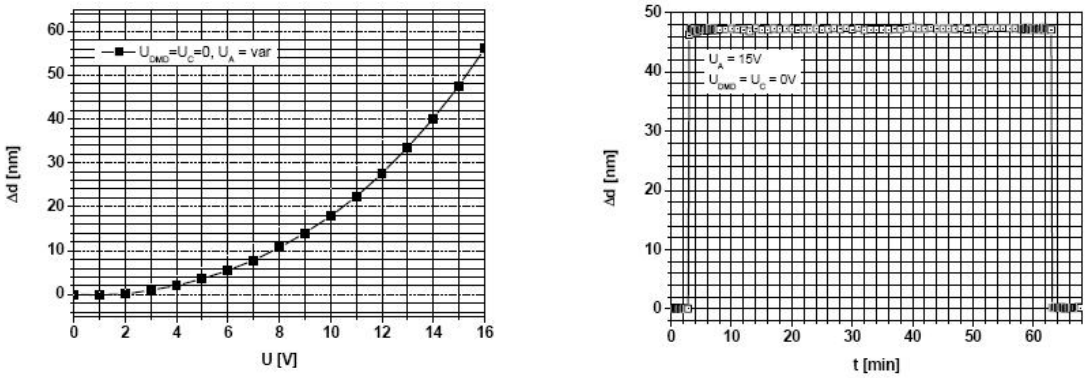

Fig. 10. [left] Measured deflection of silicon micro-mirrors with increased voltage

[right] Micro-mirror long-term stability as indicator of a level of drift

4. CONCLUSION

In this paper, the fabrication of mono-crystalline silicon micro-mirror arrays using low temperature and CMOS-compatible adhesive wafer bonding with BCB was presented. This process can be easily adapted for fabrication of micro-mirror arrays on a CMOS substrate, providing the actuation of each mirror separately. The fabrication process was discussed in detail with a special focus on the development of thin film BCB to silicon bonding. First investigation show, that the mirrors reach deflection of 55nm by applying a voltage of only 16V. A stable deflection could be achieved for more than 60minutes, a drift level of deflected mirrors could not be detected.

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REFERENCES

[1] Texas Instruments Technical Journal, vol. 15, 1998, no. 3.
[2] Ljungblad, U. B., Askebjer, P., Karlin, T., Sandstrom, T., and Sjoeberg, H., "A high-end mask writer using a spatial light modulator," Proc. SPIE 5721, 43 – 53 (2005).
[3] Dauderstädt, U., Dürr, P., Ljungblad, U., Karlin, T., Schenk, H., and Lakner, H., "Mechanical stability of spatial light modulators in microlithography," Proc. SPIE 5721, 64-71 (2005).
[4] Niklaus, F., Haasl, S. and Stemme, G., "Arrays of monocrystalline silicon micromirrors fabricated using CMOS compatible transfer bonding," IEEE/ASME J. of Microelectromechnical Systems, 12(4), 465-469 (2003).
[5] Maszara, W. P., Goetz, G., Caviglia, A., and Mckitterick, J. B.," Bonding of silicon wafers for silicon-on-insulator," J. Appl. Phys. 64 (10), 4943-4950 (1988).