Stable complementary inverters with organic field-effect transistors on Cytop fluoropolymer gate dielectric

M. P. Walser, W. L. Kalb, T. Mathis, T. J. Brenner, and B. Batlogg
Laboratory for Solid State Physics, ETH Zurich, 8093 Zurich, Switzerland

(Received 29 December 2008; accepted 12 January 2009; published online 5 February 2009)

We present results on small-molecule $p$- and $n$-type organic semiconductors in combination with the highly water repellent fluoropolymer Cytop as the gate dielectric. Using pentacene and $N,N'$-ditridecyldiphenylene-3,4,9,10-tetracarboxylicdiamide (PTCDI-C$_{13}$), we fabricated complementary inverters of high electrical quality and stability that are almost unaffected by repeated gate bias stress. The combined $p$- and $n$-type field-effect transistors show nearly ideal characteristics, very small hysteresis, and similar saturation mobilities ($\sim 0.2\ cm^2/V\ s$). Particularly PTCDI-C$_{13}$ thin-film transistors exhibit a remarkable performance in the subthreshold regime if chromium is used as contact material for electron injection: a near zero onset and a subthreshold swing as low as 0.6 V/decade. © 2009 American Institute of Physics. [DOI: 10.1063/1.3077192]

Intense efforts in research on organic semiconductors have lead to new organic materials with $p$- or $n$-type conduction, being ready for the integration in low-cost large area electronics and electronics on flexible foils and transparent substrates. A major challenge to the application of organic electronics is to realize complementary circuits. Charge transport in organic thin-film transistors (OTFTs) is mainly confined to the interface between the organic semiconductor and the dielectric. The tendency for organic semiconductors to show $p$-type conduction, but rarely $n$-type conduction, was attributed to the semiconductor-dielectric interface: electrons are trapped at the interface by hydroxyl groups present in the form of silanols in the case of the commonly used SiO$_2$ dielectric. Thus the key in promising material combinations for complementary organic circuits is a gate dielectric that allows for both $p$- and $n$-type conduction with the adjacent semiconductors, provides for chemical and electrical stability, can be easily processed, and leads to highly reliable devices. $N$-type transport has been studied on various double-layer gate dielectrics, particularly on SiO$_2$ with a thin polymeric layer on top. It was found that hydroxyl-free polymers passivate the siloxyl groups on the SiO$_2$ surface and thus improve the air stability of $n$-type OTFTs.

Previously, we reported on $p$-type small-molecule organic semiconductors in combination with an organic spin-on dielectric called Cytop, which yield field-effect transistors (FETs) with unprecedented electrical stability. Cytop has initially been used as gate dielectric in organic field-effect transistors by Veres et al. This amorphous fluorocarbon polymer is highly water repellent, has a low permittivity (2.1), is highly transparent, and also is an excellent electrical insulator. Water is known to cause gate bias stress effects, which can be reduced by employing a highly hydrophobic gate insulator. Cytop has a water contact angle of 112$^\circ$ on average, which is better than for many other polymers, and comparable to high-quality self-assembled monolayers. We found that the high contact angle of spin-coated Cytop does not decrease if the thickness of the Cytop film is reduced (down to $\sim 6$ nm).

In this study, we spun ultrathin Cytop layers on $n^+$-Si/SiO$_2$ ($\sim 260$ nm) substrates used as convenient bottom gate. Cytop CTL-809M from Asahi Glass Japan was dissolved in CT-Solv.180 in the ratio $\sim 1:30$ and spun at 1000 rpm for 40 s. The thickness of the layer (7–9 nm) was measured with a step profiler and verified with atomic force microscopy. Typical areal capacitance ($C_{\text{A}}$) of untreated Si/SiO$_2$ substrates was 12.0 nF/cm$^2$ and decreased to 11.2 nF/cm$^2$ when a spin-coated Cytop layer (7–9 nm) was added. As $p$-type semiconductor we used pentacene and as $n$-type semiconductor $N,N'$-ditridecyldiphenylene-3,4,9,10-tetracarboxylicdiamide (PTCDI-C$_{13}$) from Sigma Aldrich. High mobility (0.6–2.1 cm$^2$/V s) is reported for this and other PTCDI derivatives, such as PTCDI-C$_{12}$. For the present study, organic semiconductors and contact metals were thermally evaporated through a shadow mask at a base pressure near $3 \times 10^{-6}$ mbar. Approximately 40 nm of PTCDI-C$_{13}$ and pentacene were deposited at a rate of 0.05–0.3 Å/s, and approximately 40 nm of contact metals at 0.3–1 Å/s. The organic films were exposed to air for several minutes between the fabrication steps. Electrical measurements were performed with a HP 4155A semiconductor parameter analyzer in a He atmosphere in the dark (O$_2$, H$_2$O $<$ 0.3 ppm).

The proper choice of the electrode material is important for optimal charge carrier injection. Thus, various metals including Au, Cr, Al, and LiF have been tested with PTCDI-C$_{13}$. Using Cytop as gate dielectric, we find that chromium provides very good electron injection into PTCDI-C$_{13}$. Compared to gold contacts, the nonlinearity in the output characteristic is strongly reduced and the subthreshold regime is improved substantially. Typical transfer characteristics for PTCDI-C$_{13}$ with Cr electrodes and pentacene with Au electrodes are shown in Fig. 1. Due to the very low density of “slow” traps, hysteresis in transfer characteristics is very small and output characteristics exhibit no hysteresis at all.

In our previous studies on Cytop, we observed pentacene TFTs to be less stable against gate bias stress than pentacene single-crystals FETs. TFTs also showed much higher (more negative) onset and threshold voltages, which was attributed to growth related structural defects within the pentacene thin
Pentacene TFTs in the present study (SiO₂/Cytop) show approximately an onset voltage \( V_{on} \approx -7.7 \text{ V} \) and a threshold voltage \( V_T \approx -20 \text{ V} \). For PTCDI-C₁₃ TFTs we find \( V_{on} \approx 2.4 \text{ V} \) and \( V_T \approx 7 \text{ V} \), which is much lower than for octadecyltrichlorosilane (OTS) treated SiO₂ (~300 nm) with a similar gate capacitance (16 V/44 V).\(^{17}\) Importantly, onset and threshold voltages for PTCDI-C₁₃ are only one-third of that for pentacene on the same substrate. These results agree with studies on thicker Cypot dielectrics (~375 nm) that show similar gate capacitance normalized values. Particularly remarkable for PTCDI-C₁₃ on Cytop is the very steep onset. In the present study, the subthreshold swing \( S \) is as low as 0.6 V/decade, which is only one-fourth of that for pentacene thin films (~2.6 V/decade). Gate capacitance normalized values for PTCDI-C₁₃ are \( C_{ox}S \approx 6.7 \text{ nC/}(\text{decade} \text{ cm}²) \), which is in the order of pentacene single-crystals devices [1.3 nC/ (decade cm²)].\(^7\) However, single-crystals devices are essentially unaffected by growth related defects. Importantly, the remarkable performance in the subthreshold regime was only observed for chromium and not for gold electrodes. Following the analysis in Ref. \(^{18}\) we estimate the deep trap density of PTCDI-C₁₃ to be about a quarter of that for pentacene in the thin film. Due to the steep onset and low off current (~10⁻¹⁰ A), on/off ratios in the order of 10⁶ are possible for \( V_{GS} \) nearly above \( V_T \). Low subthreshold parameters such as onset voltage, threshold voltage, off current and subthreshold swing are particularly important for low-power complementary logics.

To fabricate complementary inverters, the basic elements of complementary logics, we combined pentacene and PTCDI-C₁₃ TFTs (photograph in Fig. 2). Inverters are commonly characterized by their static response, i.e., the voltage at the output node \( (V_{out}) \) during a voltage sweep at the common input gate \( (V_{in}) \).

Electrical stability was quantified for inverters from another fabrication batch. Figure 3 shows the shift in the switching points between logic high and low (defined from maxima in \( I_{DD} \)) due to gate bias stress. For periods of 2 h (gray shaded regions), logic low/high (0 V/40 V) is applied during a voltage sweep at the common input gate \( (V_{in}) \). Figure 2 shows static transfer characteristics of the completed inverter for supply voltages \( V_{DD} \) between 20 and 40 V. Also shown is the current \( I_{DD} \) that flows from \( V_{DD} \) to ground \( (V_{SS}) \). The hysteresis is as low as 0.2 V (inset in Fig. 2) and reflects the very small hysteresis of the combined transistors. The symmetry in the static response indicates that neither \( p- \) nor \( n- \) type conduction is dominant. Due to similar saturation mobility of \( p- \) and \( n- \) type conducting TFT, the same channel length and width can be chosen for both. The maximal gain \( g = -dV_{out}/dV_{in} \) is very high, with a maximum around 250 (inset in Fig. 2). Inverters still worked after 6 months in He atmosphere despite several days of contact to air. Importantly for applications, a reduction in \( V_{DD} \) can be expected for patterned gate electrodes.\(^{19}\)

![FIG. 1.](Image) (Color online) Transfer and output characteristics of the combined \( p- \) and \( n- \) type TFTs. Forward and reverse sweeps are shown in all panels. Hysteresis is only visible in the subthreshold regime (1 V for pentacene, 0.8 V for PTCDI-C₁₃). Note the very low onset voltage (2.4 V), threshold voltage (7 V), and subthreshold swing (0.6 V/decade) for PTCDI-C₁₃. \( C_{ox} = 11.2 \text{ nF/cm}² \), \( \mu_{sat} = 0.28/0.18 \text{ cm}²/V\text{s} \) for pentacene/PTCDI-C₁₃.

![FIG. 2.](Image) (Color online) Static inverter characteristics for a complementary pentacene/PTCDI-C₁₃ inverter with a 8 nm thick Cypot dielectric and a common \( n”- \) Si/SiO₂ bottom gate \( (V_{SS}) \). Neither \( p- \) nor \( n- \) type conduction is dominant, although both TFTs have the same channel length and width. Right: Photograph with dimensions. Inset: Gain and hysteresis for \( V_{DD} = 30 \text{ V} \). The hysteresis is as small as 0.2 V and the gain as high as 250.

![FIG. 3.](Image) Shift in the switching points due to gate bias stress. For periods of 2 h (gray shaded regions), logic low/high (0 V/40 V) is applied during a voltage sweep at the common input gate \( (V_{in}) \).
at the common input gate ($V_{\text{in}}$) while $V_{\text{DD}}=40$ V. No voltage is applied in the rest of time. The sequence was interrupted every 30 min to measure the static transfer characteristics consecutively four times (measurement period $\sim 1.5$ min per sweep). The maximal shift is less than $\pm 1$ V and the hysteresis was typically 0.4 V in the first and 0.2 V in all subsequent sweeps (the fourth sweep is used for Fig. 3). The stress experiment was repeated four times with the same device, twice as described above, and twice applying logic high first and logic low next. The shape of the curve shown in Fig. 3 was very similar for all sequences, apart from a vertical shift by approximately 0.2 V. Similar results were found for another device (16 nm Cytop) that was stressed and measured at 60 V instead of 40 V (shift $<\pm 1.5$ V, hysteresis 0.3 V). Transfer characteristics at $t=0$, 5.6, 16.8 h are shown in Fig. 4. Off currents are $<10^{-11}$ A for both input states. This results in low static power consumption, the main reason for doing complementary logics in the first place.

In summary, we propose a material combination for high quality and stress resistant organic complementary electronics. Including the very special fluoropolymer Cytop as the gate dielectric allows not only for both p- and n-type conduction, but rather leads to a very low interface trap density if combined with n-type semiconductors such as PTCDI-C_{13}. Therefore, TFTs exhibit nearly ideal characteristics, very small hysteresis, and very steep onset if an appropriate electrode material is used.

We would like to thank K. Pernstich for valuable discussions and M.P.W. gratefully acknowledges financial support by ETH Zurich in the form of an “Excellence Scholarship and Opportunity Award.”