ESTIMATING COMPLEXITY IN MULTI RATE SYSTEMS

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ABSTRACT

Estimating a system's complexity is essential before making a decision about the architecture to be built or not. Especially for mobile User Equipments (UE) complexity is a big issue. Reduced complexity, mainly meaning reduced number of additions and multiplications in a system, is highly desired also to minimize power consumption. In order to be able to compare different systems and architectures, a figure of merit for the complexity of each specific system has to be introduced. For single rate systems usually the number of operations needed for one output sample can easily be calculated. For multirate systems this task is not that trivial, as operations have to be done on different sampling rates. This paper introduces methods for gaining figures of merit of complexity for multirate systems and proposes a novel method which is believed to be best suited.

Index Terms— multirate, complexity, estimation, comparability

1. INTRODUCTION

Estimation of complexity for simulated architectures in digital signal processing is an important task and has been covered various fields among information processing. Gaining information about the complexity of programming algorithms has been a big issue already in the early 1970s [1], but also today getting insight into complexity of algorithms is seen as a very important task. It is both important in pure software related topics of information processing [2] but also on pure hardware related tasks [3]. In this paper a method for estimating the complexity of hardware related, but potentially reconfigurable algorithms by software is introduced. The goal is, to make different architectures on multiple rates and multiple outputs comparable concerning their complexity and therefore power consumption. With appropriate estimates and adequate figures of merit for complexity, different implementation approaches can be compared before being mapped on a hardware platform. However, finding good figures of merit for complexity estimates often is not that trivial. In single rate systems, where all systems like filters, regulators, etc., are running on the same sampling rate, estimates for complexity to compare different systems can be gained by counting the physically present operating units like adders and multipliers. If multirate systems are to be investigated this is no longer possible. Although great investigation in multirate systems has already been done in the past, e.g. in [4, 5], in the author's opinion no sufficient figure of merit for classifying the complexity of multirate systems has been defined. Therefore, more advanced approaches have to be found. In this paper two possible approaches for treating multirate systems are given with one of those being considered as optimal. The paper is structured as follows. Section 2 explains the main problem and introduces methods for gaining complexity estimates for single and multirate systems with single and multiple output. Section 3 treats a real world example and provides an alternative description for the gained complexity estimation figure of merit.

2. COMPLEXITY ESTIMATION

This section describes methods for evaluating the overall complexity for different system types. For all systems a common input sampling rate is assumed. Starting with a single rate system with one output in the following a multirate sys-

tem with one output will be investigated. Finally multiple output multirate systems are discussed.

2.1. Single Rate System

In a single rate system all components are running on one single sampling frequency. Therefore, estimating the complexity is straight forward. Assuming the system according to figure 1, the overall complexity can be estimated by adding up all physically present adders and multipliers. A complexity estimate for this system would be

$$\begin{aligned} \mathbf{C}_1 &= (2+4+6+32)\text{adds} + (4+16)\text{mults} \\ &= 44\text{adds} + 20\text{mults}. \end{aligned} \tag{1}$$

Fig. 1: Example of a single rate system.

This estimation is straight forward, but also builds the basis for further investinvestigations in multirate systems.

2.2. Multirate System with Single Output

Given a multirate system according to figure 2, estimating the overall complexity is slightly more complicated. The different sampling rates have to be considered.

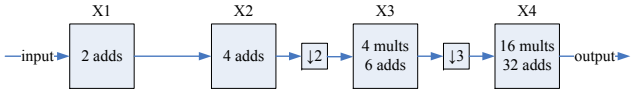

Fig. 2: Example of a multirate system with single output.

As it can be seen, the single blocks in the system are the same like in the single rate example, whereas some downsampling blocks are added. Compared to the previous example, it is no longer valid, to just add up all physically present operation blocks, i.e. adders and multipliers. In fact, the single operation blocks have to be weighted by the downsampling factor in front of the blocks. This can be explained by the following: assuming an overall downsampling factor of six, like given in figure 2, for one output sample six input samples had to be present before. If one adder is physically present before the downsampling stage, for one output sample after the downsampling stage no longer one but six additions have to be considered, as all six input samples resulting in one output sample have to pass the only adder. In the given example it would be as follows: for each output sample at block X4 one input sample at block X4 is needed. Due to the downsampling by a factor of three, for one output sample at block X4 now three input samples at block X3 are needed. The overall complexity can be calculated according to

$$\begin{aligned} \mathbf{C}_2 = \; & 1 \cdot (32\text{adds} + 16\text{mults}) + 3 \cdot (6\text{adds} + 4\text{mults}) + \\ & 3 \cdot 2 \cdot 4\text{adds} + 3 \cdot 2 \cdot 2\text{adds} \\ = \; & 68\text{adds} + 28\text{mults}. \end{aligned} \tag{2}$$

The result seems surprising on first sight as $\mathbf{C}_2 > \mathbf{C}_1$, although downsampling has been performed and the complexity should decrease. What is not considered in this representation is, that the output sampling rate in this multirate example is lower and therefore the number of operations has to be performed less often in a given time window than in the previous example. The input sampling rate is still assumed to be the same for both examples. This is an important point to consider. The given problem can be solved by adjusting the number of operations to a common sampling rate, e.g. the output sampling rate. In both cases given so far, the number of operations refer to one output sample gained. For the first example, the output sampling rate is six times the one from example two. Assuming a fixed time window of observation, the chain from the first example had to be processed six times, while the second example's chain was only used one time. Considering this result leads to a complexity for the single rate example of

$$\mathbf{C}_{1,norm} = 6 \cdot \mathbf{C}_1 = 264\text{adds} + 120\text{mults} > \mathbf{C}_2. \tag{3}$$

This gives a fair comparison, as in 3 the precondition constant input sampling rate is also considered. However, normalizing the number of operations in this way leads to some problems in the case of multirate systems with more than one output.

2.3. Multirate System with Multiple Outputs

In typical applications for multirate systems, e.g wavelet filter banks or blocker detection units described in [6–9], there is more than one output present in the system. Also the different outputs are considered to be at different sampling frequencies. Figure 3 gives an illustration of this scenario.

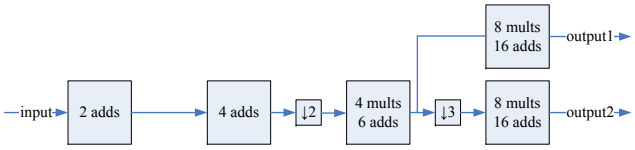

Fig. 3: Example of a multirate system with multiple outputs.

As it can be seen, the system consists of the same amount of physically present operating blocks like the others before. Only the last block (block X4 according to figure 2) has been split into two identical blocks with half of the operating units each. Now the question is how to weight these blocks and again achieve a fair comparison of complexity. In the example described in section 2.2, the reference and starting point for the complexity estimate has been the effort for one output

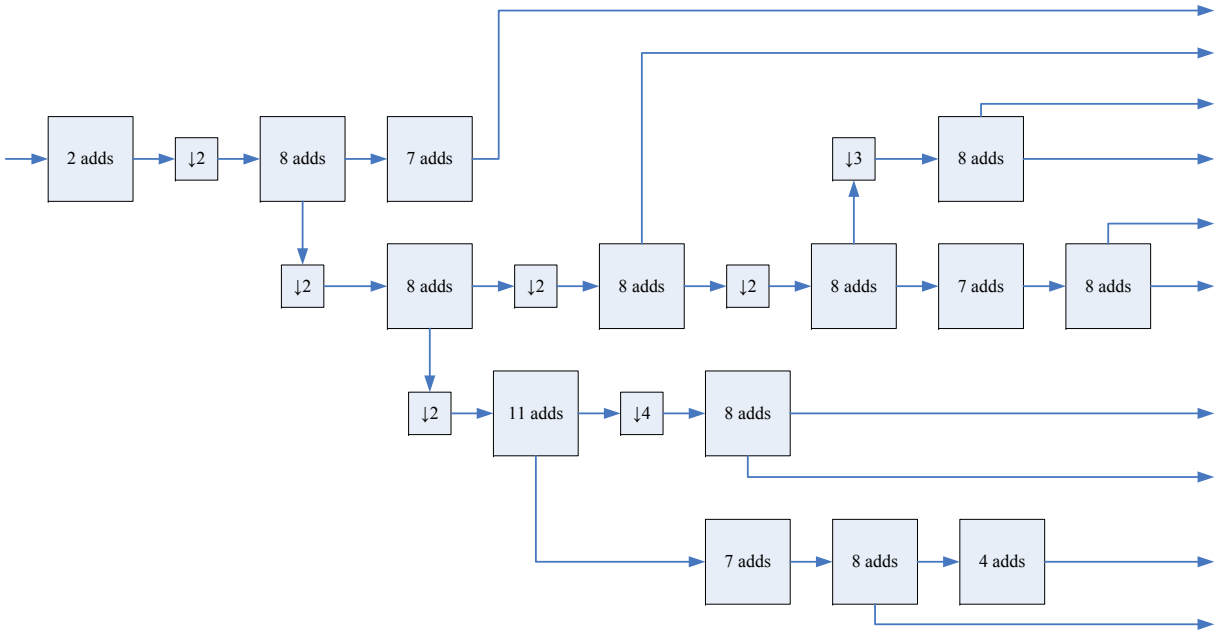

Fig. 4: Example chain of a blocker detection unit for LTE systems.

sample to be calculated. In this example more outputs at different sampling rates are present. It would be possible to take one output sample from output1 as a new reference (coinciding with $\frac{1}{3}$ of an output sample at output2, which is not treatable) or one output sample at output2 (coinciding with three output samples at output1). For complex systems this decision will not be unique and a fair comparison would be very difficult. A better approach would be to take one input sample as a reference. In this case the computational effort needed to process one input sample can be easily estimated. The advantage of this is, that the approach is directly comparable with the single rate example as the input frame is considered to be from the same source and same sampling frequency. Also a comparison with the multirate single output example would be possible. For this example the complexity given by $\mathbf{C}_2$ refers to one output sample. Due to the downsampling factor of six this also refers to six input samples. Normalizing $\mathbf{C}_2$ to one input sample again would provide a fair comparison of complexity.

$$\mathbf{C}_{2,norm} = \frac{\mathrm{C}_2}{6} = \frac{34}{3}\text{adds} + \frac{14}{3}\text{mults}. \tag{4}$$

For the third example this estimation of complexity can be done by starting at the input with weight '1' and following each path to the output by weighting each stage with the downsampling factor D^{-1}. We end up with

$$\begin{aligned}\mathbf{C}_3 \quad &= 2\text{adds} + 4\text{adds} + \tfrac{1}{2}(6\text{adds} + 4\text{mults}) + \\ &\tfrac{1}{2}(16\text{adds} + 8\text{mults}) + \tfrac{1}{2\cdot 3}(16\text{adds} + 8\text{mults}) \\ &= \tfrac{59}{3}\text{adds} + \tfrac{22}{3}\text{mults}\end{aligned} \tag{5}$$

Now all three systems can be compared as

$$\mathbf{C}_{2,norm} < \mathbf{C}_3 < \mathbf{C}_1 \tag{6}$$

for both additions and multiplications. All three systems now can be compared w.r.t. their complexity. For these examples, the single rate model is the most complex while the multirate example with one output is the least complex.

The approach discussed in this section is considered to be optimal for most cases, if communication systems are the systems under test. Those systems typically consist of one input and multiple outputs. In the next section a realistic example is discussed and an alternative description is introduced.

3. REALISTIC EXAMPLE AND ALTERNATIVE DESCRIPTION

Figure 4 shows a realistic example for an architecture taken from a Long Term Evolution (LTE) blocker detection chain. This chain is a representative architecture for a blocker detection unit described in [8]. No further details about this specific application should be given here, the important thing is the estimation of the overall complexity of the system to make it comparable to other approaches.

A typical input sampling frequency of this kind of architecture and class of communication systems is 104MHz. As it can be seen, multiple stages at different sampling rates are present. Each stage consists of adders only. Multiple outputs at different sampling rates have to be considered. This real world example is of the type described in section 2.3. According to the methods defined there, a complexity estimate

Table 1: Number of real additions for the investigated filter chain approach per input sample

sampling frequency	number additions
104MHz	2
52MHz	15
26MHz	8
13MHz	38
6.5MHz	23
3.25MHz	8
2.2MHz	8

of this architecture can be given by

$$\begin{aligned}\mathbf{C}_{real} = & \quad 2+\tfrac{1}{2}(8+7)+\tfrac{1}{2\cdot 2}\cdot 8+ \\ & \tfrac{1}{2\cdot 2\cdot 2}(8+11+7+8+4)+\tfrac{1}{2\cdot 2\cdot 2\cdot 4}\cdot 8+ \\ & \tfrac{1}{2\cdot 2\cdot 2\cdot 2}(8+7+8)+\tfrac{1}{2\cdot 2\cdot 2\cdot 2\cdot 3}\cdot 8 \\ = & \quad 2+\tfrac{15}{2}+2+\tfrac{19}{4}+\tfrac{1}{4}+\tfrac{23}{16}+\tfrac{1}{6} \\ = & \quad 18.1\,[adds] \end{aligned} \tag{7}$$

This means, for one input sample mathematically 18.1 additions have to be performed while this sample propagates through the system. Of course, after downsampling by a factor of two, 1/2 of a sample would be remaining at the downsampler's output, which is not feasible for real systems. This shows, that the made assumption is only of mathematical nature and only can be used to estimate and compare complexity of different systems with different structures.

The gained result could also be interpreted differently. At different stages different sampling frequencies are provided for the adders. It is possible to write down the actual additions at those different sampling frequencies, like shown in table 1. Again by weighting the number of additions at each stage by $\frac{f_{s,stage}}{f_{s,input}}$ with $f_{s,stage}$ defined as the sampling frequency at the specific stage and $f_{s,input}$ being the sampling frequency at the input of the system, we end up with 18.1 additions per input symbol like described above. Both representations are equivalent.

4. CONCLUSIONS

Estimation of a system's complexity is an important task in digital signal processing. Even more important is to find a common figure of merit of complexity in different systems to be able to compare more of them w.r.t. complexity and therefore power consumption. It has been shown, that this task is easy to be solved for single rate systems with one input, while it is more sophisticated for multirate multiple output systems, which are commonly used in many applications. A method to be able to compare complexity for these systems was introduced. A novel figure of merit for estimating complexity, average operations per input sample, has been defined and an alternative description introduced.

Acknowledgment

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5. REFERENCES

[1] A. Kalnin'sh, "Complexity Estimation for the Coloring of Graphs on a Turing Machine," in *Probl. Peredachi Inf.*, vol. 7, no. 4, 1971, pp. 59–72.

[2] F. B. Kalva, Hari, "Complexity Estimation of the H.264 Coded Video Bitstreams," in *The Computer Journal*, vol. 48, no. 5, 2005, pp. 504–513.

[3] M. Bhat and H. Jamadagni, "Complexity Estimation and Network Synthesis based on Functional Smoothness and Entropy Measures," in *IEEE INDICON 2004 First India Annual Conference*. Karagpur: IEEE, Dec. 2004, pp. 368–372.

[4] J Harris, Fredric, *Multirate Signal Processing for Communication Systems*, 5th ed. Upper Saddle River, New Jersey 07458: Pearson Education, Inc. - Publishing as Prentice Hall Professional Technical Reference, 2008.

[5] H. G. Goeckler and A. Groth, *Multiratensysteme*. Wilburgstetten: J. Schlembach Fachverlag, 2004.

[6] A. Mayer, L. Maurer, G. Hueber, T. Dellsperger, T. Christen, T. Burger, and Z. Chen, "RF Front-End Architecture for Cognitive Radios," in *Proceedings of the 18th Annual IEEE International Symposium on Personal, Indoor and Mobile Radio Communications, PIMRC*, Athens, Greece, Sep. 2007, pp. 1–5.

[7] A. Mayer, L. Maurer, G. Hueber, B. Lindner, C. Wicpalek, and R. Hagelauer, "Novel Digital Front End Based Interference Detection Methods," in *Proceedings of the 10th European Conference on Wireless Technology*, Munich, Germany, Oct. 2007, pp. 70–74.

[8] T. Schlechter and M. Huemer, "Overview on Blockerdetection in LTE Systems," to be published in *Proceedings of Austrochip 2010*, Villach, Austria, Oct. 2010.

[9] G. Hueber, R. Stuhlberger, and A. Springer, "Concept for an adaptive digital front-end for multi-mode wireless receivers," in *Proceedings of the IEEE International Symposium on Circuits and Systems, ISCAS*, Seattle, WA, May 2008, pp. 89–92.