Influences on the nonlinearity of HfO_2 based ferroelectric synapses (FeFETs) for neuromorphic computing

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Hafnium oxide based ferroelectric FETs (FeFETs) have been demonstrated as a viable memory implementation of synapses for neuromorphic computing and deep learning [1]. For a neuromorphic implementation the synaptic memory is mandatory to retain a multitude of addressable conductance states in order to resemble the weight function. In FeFETs this is realized by remnant polarization state levels resulting in modulated drain current. To address the different states (weight increase/decrease), three different types of signal sequences have been utilized. Firstly, varying the number of pulses, secondly, varying the pulse width, and thirdly, varying the pulse height [2]. One important figure of merit is the nonlinearity of the weight increase/decrease.

Here, we present the modulation capability of the nonlinearity for Si- and Zr-doped HfO_2 FeFETs. We demonstrate that the nonlinearity decreases with increasing read gate voltage in depression, whereas it increases in potentiation. Furthermore, for the studied pulse sequences, the influence of pulse width and amplitude is discussed. Additionally, influences from the device integration, such as interface layer material and spacer oxide, as well as the ferroelectric layer dopant, were investigated. Finally, the trends of different device parameters are depicted in terms of future scalability.

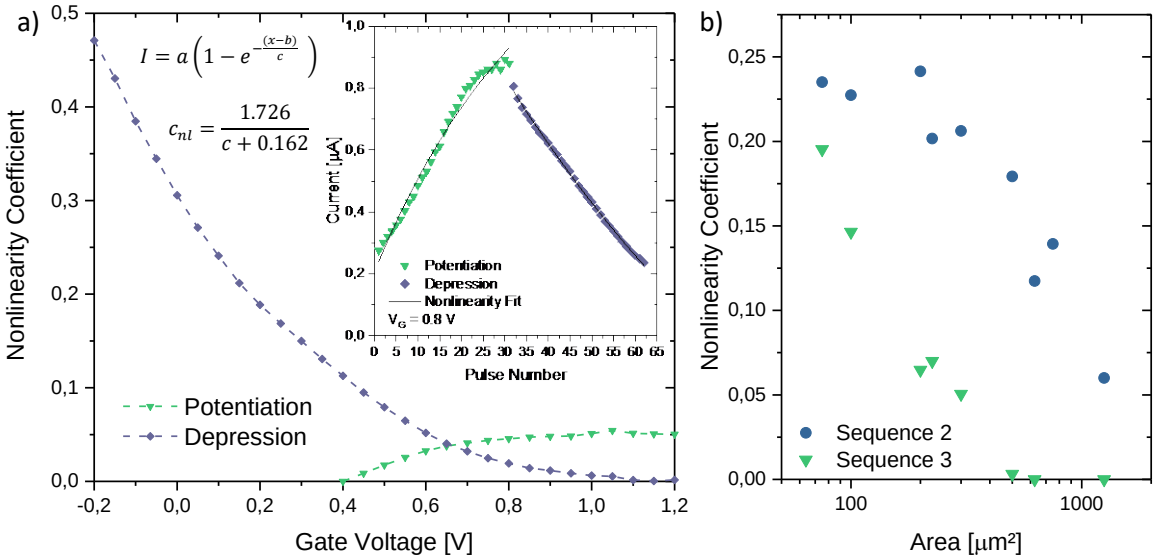

Figure 1: a) Gate voltage dependence of the nonlinearity coefficient for a pulse sequence with varying amplitude. Depression shows a reduction of nonlinearity with increasing gate voltage. On the contrary, the nonlinearity coefficient of potentiation increases. Furthermore, the current at a gate voltage of 0.8 V vs. the pulse number is given in the inset figure. b) The increase of the nonlinearity coefficient with a decreasing area. The nonlinearity Coefficient (here shown for depression) for sequence 2 increases less drastically with area than sequence 3.

[1] Jerry, M. et al.; IEDM, 6.2.1-6.2.4, 2017

[2] Oh, S. et al.; IEEE Electron Device Lett. 38 (6), p. 732-735, 2017