A Low-Noise, High-Gain Quasi-Millimeter-Wave Receiver MMIC with a Very High Degree of Integration Using 3D-MMIC Technology

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SUMMARY We present a highly integrated quasi-millimeter-wave receiver MMIC that integrates 22 circuits in a $3 \times 2.3$ mm area using three-dimensional MMIC (3D-MMIC) technology. The MMIC achieves low noise (3 dB) and high gain (41 dB) at 26 GHz by using an on-chip image reject filter. It integrates a multiply-by-eight (X8) local oscillator (LO) chain with the IF frequency of the 2.4 GHz band and can use low-cost voltage-controlled oscillators (VCOs) and demodulators in a 2–3 GHz frequency band. Multilayer inductors contribute to the miniaturization especially in a 2–12 GHz frequency band. Furthermore, it achieves a high dynamic range by using two step attenuators with a new built-in inverter using an N-channel depression field-effect transistor (FET). The power consumption of the MMIC is only 450 mW.

key words: receiver, low noise, 3D-MMIC, fixed wireless access (FWA) system

1. Introduction

The broadband communication environment has been developing very rapidly in recent years. Fixed wireless access (FWA) systems have the advantage of providing fast Internet services to areas and user homes where it is difficult to provide broadband optical access. However, FWA equipment is still very expensive because the main market for these systems is business users, and thus these systems must provide high link quality over long distances. To provide low cost FWA systems for home users, we developed the Wireless IP Access System (WIPAS), which is a point-to-multipoint (P-MP) FWA system using 64-QAM and 16-QAM and QPSK signals in the 26 GHz frequency band [1]. A summary of its specifications is shown in Table 1.

Table 1 Summary of WIPAS specifications.

<table>
<thead>
<tr>
<th>Frequency Band</th>
<th>26GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Access</td>
<td>P-MP</td>
</tr>
<tr>
<td>Transmission</td>
<td>TDMA/TDD</td>
</tr>
<tr>
<td>Transmission Capacity</td>
<td>240 Mbit/s</td>
</tr>
<tr>
<td>RX power range</td>
<td>-80 to -30 dBm</td>
</tr>
<tr>
<td>Modulation</td>
<td>64-QAM, 16-QAM, QPSK</td>
</tr>
<tr>
<td>Transmission power</td>
<td>10.3 dBm @ 64-QAM, 11.5 dBm @ 16-QAM, 14 dBm @ QPSK</td>
</tr>
</tbody>
</table>

Avoiding quasi-millimeter-wave interconnects between chips or components is an excellent way to improve wireless equipment. Since it is very important to integrate RF functions on a single chip, our approach was to integrate receiver circuits and multiply-by-eight (X8) circuits for local oscillator (LO) signals. Even with this approach, however, the chip must remain small because large chips bring about lower yield rates and higher prices.

The use of CMOS technology is suitable for achieving a high degree of integration. However, the new-generation CMOS devices that have been developed for millimeter-wave and quasi-millimeter-wave MMICs have low breakdown voltage and greatly increase photomask costs. In contrast, GaAs devices for such MMICs have higher breakdown voltages. They are suitable for multilevel modulation such as 64-QAM, because their signals require the operating points of devices to be significantly backed-off from their saturation points. These features make them suitable for middle-size markets such as those for FWA systems. However, it is difficult for conventional GaAs-MMICs to achieve high gain and low noise by integrating receiver circuits and LO circuits in a small chip [2], [3]. A higher degree of integration is needed for GaAs-MMICs.

We also developed three-dimensional MMIC (3D-MMIC) technology [4], [5], which makes highly integrated MMICs possible. Figure 1 shows the basic structure of a 3D-MMIC device. Such devices are formed on a substrate using a standard fabrication process and the upper polyimide layers are used for passive circuitry. This offers three significant benefits. First, thin film microstrip (TFMS) lines, which make narrow line width and tight line spacing possible, are formed on this structure [6]. Second, the stacked

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Fig. 1 Basic 3D-MMIC structure.
structure makes small and broadside coupling possible, resulting in 3-dB couplers and multilayer inductors. Third, ground planes can be formed on any dielectric layer and can isolate the components, which are formed above and below the ground plane.

The authors have proposed a highly integrated receiver MMIC that uses 3D-MMIC technology [7]. It has a low noise, high gain, high dynamic range, and high degree of integration. In this paper, we discuss the key technologies of the high performance receiver MMIC in detail. To achieve a low noise, an on-chip image reject filter is proposed and used in the receiver chip. The block diagram is examined in detail, and the low noise and high gain low noise amplifier is designed. To realize high gain and the high dynamic range, RF and IF bands step attenuators with a built-in inverter are used. Moreover, a resistive mixer is examined for high linearity. We use multilayer inductors for high degree of integration and small size.

The rest of this paper is organized as follows: In Sect. 2, we describe the target values of the MMIC. In Sect. 3, the key technologies of the receiver MMIC are explained in detail. In Sect. 4, we conclude the paper with a summary of key points.

2. Circuit Design

The 3D-MMIC process incorporates five polyimide layers and four wiring metals (Au) on the GaAs wafer surface. The thicknesses of the top polyimide layer and the other polyimide layers are 3.5 and 2.5 μm, respectively. Those of the top wiring metal and the others are 2 and 1 μm, respectively. The active process uses GaAs 0.15 μm-gate (pseudomorphic high mobility transistors (pHEMTs), metal-insulator-metal (MIM) capacitors, and epitaxial resistors.

The target values of the receiver MMIC were set as follows:
- Conversion gain is greater than 35 dB.
- Noise figure is smaller than 4 dB.
- Dynamic range is greater than 50 dB (−80~ −30 dBm).
- Chip size is smaller than 9 mm\(^2\).
- IF and voltage-controlled oscillator (VCO) frequency bands are 2–3 GHz.

To reduce the number of chips, we attempted to integrate receiver circuits and a multiply-by-eight (X8) LO chain. Figure 2 shows the block diagram designed to achieve the above-mentioned targets. The developed receiver MMIC integrates low-noise amplifiers (LNAs), an image reject filter, step attenuators with a built-in inverter, a down-converter, and intermediate frequency amplifiers. It also integrates three frequency doublers, driver amplifiers, and a 2-band elimination filter for LO signals.

To achieve high gain and low noise, a 4-stage LNA is used. The step attenuators are inserted into the LNA and a 3-stage IF amplifier is used to prevent the circuits from being saturated. These attenuators can achieve a large dynamic range.

The IF and LO circuit frequencies are 2.4–12 GHz. Such circuits need large-size inductors for matching. To reduce the chip size, we used multilayer inductors as shown in Fig. 1. The stack inductors can have inductances 2–8 times greater than those of single-layer inductors.

3. MMIC Performance

3.1 Low-Noise Amplifier (LNA)

As shown in Fig. 3, a 3D-MMIC transistor has additional parasitic capacitances because it has a polyimide layer. This affects HEMT behavior at high frequencies such as that observed in the quasi-millimeter-wave band. Therefore, we optimized it with parasitic capacitances.

Figure 4 shows simulated and measured performance, with and without the capacitances, of a 1-stage LNA for the 26 GHz band. The simulated results with the proposed model are in good agreement with the measured results.

Figure 5(a) shows the 3-stage LNA configuration. It has a self-bias configuration using resistors connected between transistor and ground sources, and the gate biases are set to 0 volts. This configuration decreases the circuit performance variation produced by factors such as temperature fluctuation and production tolerance. For example, GaAs amplifier’s gain and drain current \(I_{ds}\) decrease as the temperature rises. In the self-bias configuration, gate-to-source voltage is shown as \(V_{gs} = -I_{ds} \times R_s\), where \(R_s\) is the resistance of the resistor between source and ground, as shown in Fig. 5(b). Therefore, the gate-to-source voltage at low temperature is lower than that at high temperature (\(V_{gs,low\_temp} < V_{gs,high\_temp}\)). This decreases the gain variation. The 0-volt gate bias eliminates its gate bias line.

The impedance-matching circuits are composed of....
TFMS lines made of top wiring metal. The ground plane is formed on the top surface of the bottom polyimide layer and covers almost the entire die surface. The spacing between line and ground plane of TFMS lines is under 10 μm. In general, lines are sufficiently isolated when line spacing is three times wider than the spacing between line and ground plane, as shown in Fig. 6. This means lines can be spaced only 30 μm apart. The TFMS lines make significant miniaturization possible. The 3-stage LNA is arranged on an area of only 1.0 × 0.6 mm.

Figure 7 shows the measured S-parameters and noise figure (NF) of the 3-stage LNA. The gain is above 21 dB and the NF is less than 2.2 dB from 24.5–26.5 GHz. It is small and has high gain, low noise, and a drain current of 45 mA.

3.2 Image Reject Filter

The band rejection filter at the image frequency band is located after the 3-stage LNA. It uses two open stubs, one 20 μm wide and 530 μm long and the other 14 μm wide and 2360 μm long. The stubs use TFMS lines made of top wiring metal, which can integrate a long stub into a small area. The estimated area using an image reject mixer is 4 times larger than that of the image reject filter.

Figure 8 shows the implemented image reject filter and
its measured insertion loss (S21). The insertion loss is \(-18\) and \(-1.5\) dB at 19 and 26 GHz, respectively.

### 3.3 Step Attenuators with Built-in Inverter

To achieve a high dynamic range, two step attenuators are also integrated. To improve low-noise performance, the attenuators should be located at an early stage. On the other hand, to improve dynamic range, they should be located at a later stage. To achieve both low-noise performance and high dynamic range, one attenuator is located between the 3-stage and 1-stage LNAs and the other is located between the 1-stage and 2-stage IF amplifiers (see Fig. 2). Both attenuators require control bias and inverted bias. To reduce the number of MMIC pads, a new built-in inverter that can generate these biases is also integrated. This inverter controls the two attenuators through the use of identical timing.

Figure 9 shows the configuration of the step attenuators with the built-in inverter. Both the attenuators and the inverter consist of resistors, capacitors, and transistors to decrease size and widen frequency range. Table 2 shows the simulation results for the output biases of the inverter. The inverter outputs \(V_{out1}\) of \(-1.48\) volts and \(V_{out2}\) of 0 volts when it receives \(V_{in}\) of \(-1.5\) volts. It also outputs \(V_{out1}\) of \(-0.01\) volts and \(V_{out2}\) of \(-1.33\) volts when it receives \(V_{in}\) of \(-3.5\) volts. The \(V_{out1}\) is almost the same as the reversing voltage of \(V_{out2}\). The \(V_{out1}\) and \(V_{out2}\) are changed between 0 volts and the pinch-off bias. The \(V_{out1}\) and \(V_{out2}\) can be used for the control biases of the step attenuators. Therefore, no additional MMIC pad or external inverter is required.

Figure 10 shows the measured insertion loss and return loss of the step attenuator with the built-in inverter, which can be used in a very wide frequency band. Figure 10(a) shows the RF band attenuator. At 26 GHz, the insertion loss is \(1.8\) dB in the attenuator’s OFF state and \(8.7\) dB in its ON state, the ON/OFF ratio is about \(7\) dB. The return loss is less than \(-26\) dB from DC to 3 GHz. Figure 10(b) shows the IF band attenuator. At 2.4 GHz, the insertion loss is \(1\) dB in the attenuator’s OFF state and \(18.4\) dB in its ON state, the ON/OFF ratio is about \(17\) dB. The return loss is less than \(-26\) dB from DC to 3 GHz.

### 3.4 Down-Converter

This receiver treats multilevel modulation signals such as 64 QAM. Unfortunately, these signals have large peak-to-average power ratio (PAPR). The large PAPR requires the operating points of devices to be significantly backed-off from their saturation points, and the down-converter used for this purpose must have a large dynamic range. Therefore, a resistive mixer is used as a down-converter [8]. In a resistive mixer, we define the LO input signal as

\[
V_{LO} = a_{LO} \cdot \left( \frac{1}{2} + \frac{2}{\pi} \sin \omega_{LO} t + \frac{2}{3\pi} \sin 3\omega_{LO} t + \cdots \right),
\]

and the RF input signal is defined as \(V_{RF} = a_{RF} \sin \omega_{RF} t\)

The IF output signal can be described as

\[
V_{IF} = a_{RF} \cdot \left( \frac{1}{2} \sin \omega_{RF} t - \frac{1}{\pi} \{ \cos(\omega_{LO} + \omega_{RF}) t - \cos(\omega_{LO} - \omega_{RF}) t \} + \frac{1}{3\pi} \{ \cos(3\omega_{LO} - \omega_{RF}) t + \cdots \} + \cdots \right)
\]

Since the desired IF output \(\omega_{LO} - \omega_{RF}\), is \(1/\pi\) times that of the RF input signal, the conversion gain should be about \(-10\) dB. Regardless of how low the conversion gain is, however, it has higher linearity than other types of field-effect transistor (FET) mixers and needs no drain bias. Eliminating the drain bias line helps to reduce MMIC size.

Figure 11 shows the down-converter circuit. The gate bias is set around the pinch-off voltage. RF signals are input to and IF signals are output from the drain port.
3.5 LO Circuits

In quasi-millimeter-wave bands, VCOs are usually more expensive than those in microwave bands. Low-cost VCOs and demodulators in the 2–3 GHz frequency band can be obtained from a variety of makers. To reduce the cost of wireless equipment, the receiver MMIC operates with a VCO in the 3 GHz band and with an intermediate frequency (IF) at 2.4 GHz. The MMIC integrates multipliers and driver amplifiers for LO signals. Signals from the VCO are multiplied in an integrated multiply-by-eight (X8) LO chain up to the 24 GHz band, resulting in an IF center frequency of 2.4 GHz, as shown in Fig. 13.

Figure 12 shows the down-converter’s measured output components. Its conversion loss is 11 dB and its input $P_{1dB}$ is 3 dBm at input frequency of 26 GHz and input LO power of 0 dBm.

3.6 IF amplifiers and Multilayer Inductor

IF amplifiers located at the output stage employ inductive loads to gain large output signals. In such amplifiers, spiral inductors are used as an output-matching network to achieve
high output power. However, amplifiers at microwave frequency need large inductors for matching [11]. These inductors occupy a large area on MMICs. 3D-MMIC technology features the kind of multilayer inductors shown in Fig. 1, which have inductances two to eight times higher than those of single-layer inductors and contribute greatly to reducing MMIC size [12]. We used three types of inductors to reduce the inductor size, i.e., single-, double-, and triple-layer ones. The spiral pattern of the single-layer inductor consists of a 2-μm-thick top wiring line which is a low-loss Au line of the 3-D process. Those of the double- and triple-layer inductors consist of a 2-μm-thick top wiring line and 1-μm-thick second and third Au lines.

Figure 17 shows measured inductance versus area for the single-, double-, and triple-layer inductors. When the area increases, the effect of increasing inductance by adding layers also increases.

Figure 18 shows the measured self resonant frequency versus inductance of the single-, double-, and triple-layer inductors. Almost no difference was observed in the measurement results for any of the inductors, even though it has been reported that the self resonant frequency decreases when using multilayer inductors on silicon. We consider that this is because the 3D MMIC process we employed makes use of polyimide layers that are 2.5 μm thick. Consequently, the parasitic capacitance is small and the self resonant frequencies of the multi-layer inductor do not decrease.

Figure 19 shows the measured peak Q-factor versus inductance. Though the results obtained are somewhat uneven, the Q-factor decreases when the inductance values rise. No tendency for the Q-factor to decrease due to an increase in the number of layers was observed.

Our IF and LO driver amplifiers use double and triple-layer inductors. There are fifteen stack inductors on the receiver MMIC, which saves about 6% of the MMIC area.

Figure 20 shows measured performance of the 2-stage IF amplifier. Its gain is 15 dB and its saturation power is
3.7 Capacitors Located under Ground Plane

Decoupling capacitors on DC bias lines and bypass capacitors for self-bias configurations require large capacitance values and occupy a large portion of the chip area. Their total capacitance is about 200 pF and their size is about 0.64 mm², which is 9% of the MMIC area. To reduce the chip size, these large capacitors were fabricated under the ground plane and isolated to TFMS lines, as shown in Fig. 6. This enables the large areas above the capacitors to be used for signal lines, which also helps reduce MMIC size.

3.8 Receiver MMIC

Figure 21 shows a photograph of the fabricated receiver 3D-MMIC. It integrates the above-mentioned RF and IF circuits and LO chain. It has a total of 22 circuits, which are integrated on a chip only $3 \times 2.3 \text{ mm}$. The MMIC power consumption is 450 mW.

We tested two types of receiver MMICs, with and without an image reject filter, as shown in Fig. 8. The measured conversion gains are shown in Fig. 22. With an image reject filter, the gain is 41 dB at 26 GHz and above 37 dB between 24.5–28 GHz. Without the image reject filter, the gain is 40 dB at 26 GHz and above 38 dB between 24.5–28 GHz.

The gain with the image reject filter is higher than that of without image reject filter at 26–28 GHz. The enhancement is caused by only the parameter tuning of the impedance matching and gain of the LNA. The step attenuator can control the conversion gains by about 22 dB, with little change in the frequency characteristics.

The measured SSB NF are shown in Fig. 23. With an image reject filter it achieves a low SSB NF, i.e., 2–3.5 dB between 24.5–26.5 GHz. This SSB NF is lower than that obtained without an image reject filter, e.g., it is 1.5 dB lower at 26.5 GHz. The experimental results show that the image reject filter is beneficial for increasing the gain and lowering the noise. The conversion gain of the receiver chip with an image reject filter is lower than that of one without an image reject filter at the 19–23 GHz image band. Therefore, the lower noise level at the image band is converted to the IF band, which results in a lower SSB NF. With an FWA system functioning as receiver equipment, the NF requirement is less than 8 dB. The NF target for our newly developed receiver MMIC is less than 4 dB. With an image reject filter, our receiver MMIC achieves this target.

With step attenuators, the receiver MMIC can receive higher RF input power than it can with no attenuators. The usage of attenuators in our receiver MMIC extends its input $P_{1db}$ from −41 to −26 dBm, as shown in Fig. 24.
Table 3 shows a comparison of the proposed MMIC receiver with other receiver MMICs [2], [3]. Our receiver has the advantages of high gain and low noise. In addition, though it includes IF amplifiers and an X8 LO chain, the chip size is only 6.9 mm². It is thus small in size and furthermore has high gain, low noise, and a high dynamic range.

4. Conclusions

We have presented a highly integrated quasi-millimeter-wave receiver MMIC that uses 3D-MMIC technology. The receiver MMIC integrates low noise amplifiers, an on-chip image reject filter, step attenuators with built-in inverter, a resistive mixer, IF amplifiers, and an X8 LO chain. These circuits were integrated on a chip of only 3 x 2.3 mm by using the miniaturization techniques such as TFMS lines, and multilayer inductors. The MMIC performed excellently, achieving a SSB noise figure of 3 dB and a high gain of 41 dB at 26 GHz using the on-chip image reject filter. High dynamic range was achieved using two step attenuators with a new built-in inverter. The power consumption of the MMIC was only 450 mW. This MMIC will help reduce the cost of equipment for quasi-millimeter-wave FWA systems.

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References


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