Low-noise charge sensitive readout for pyroelectric sensor arrays using PVDF thin film

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Abstract

The paper presents a fully integrated low-noise readout circuit for the purpose of front-end amplification in pyroelectric infrared focal plane arrays (IRFPA). A low-noise and low-power charge sensitive amplifier (CSA) has been fabricated and characterised in a standard CMOS process. A value of 11.4 nV/√Hz at 100 Hz input referred noise voltage has been measured for a maximum power dissipation of 210 μW. Pyroelectric polyvinylidene fluoride (PVDF) thin films have been coated on 256-element focal plane arrays including the low-noise CSA as readout device. Experimental values of voltage responsivities of 3510 V/W on average at 10 Hz modulation frequency have been achieved for a sensing area of 105×105 μm. © 2000 Elsevier Science S.A. All rights reserved.

Keywords: CMOS; Low noise; Focal plane array; PVDF

1. Introduction

The prospect of developing low-cost uncooled infrared imaging devices based on pyroelectric materials within silicon circuits is highly motivating. New technologies now allow the development of low-cost infrared arrays that present similar performance to that of photon-type infrared imager. The applications include night vision, surveillance, public safety, medical imaging, process control, etc. Sensors based on the polyvinylidene fluoride (PVDF) thin film are still under investigation [1], and imaging devices detecting low-temperature targets are yet to appear. Despite the proven need of an insulating layer or suspended micro-machined structure to enhance the PVDF responsivity [1–5], this work aims at a simpler, thus low-cost, means of connecting the sensing material onto the readout silicon chip. The choice of readout circuit and technology is crucial to ensure good performance of the overall sensor.

Various configurations of amplifiers have been employed in the past, and the choice of readout often depends on a compromise between chip area and circuit complexity. Single MOSFET or JFET devices as source follower, common drain and common source amplifiers have been reported to achieve successful sensors [6]. These configurations provide the detector with a charge to voltage converter with excellent yield while utilising minimum area. However, a source follower has a unity gain and thus fails to amplify the detector noise beyond the input noise level of subsequent stages. The common-source or common-drain configuration is usually employed to overcome this problem. Unfortunately, this type of amplifier is not easily implemented in conventional integrated circuit technology, as a gate bias resistor is required. This is a consequence of the extremely high resistance presented by the PVDF polymer layer, thus not providing a sufficient gate leakage current to hold a DC voltage. The biasing of a simple common-source MOSFET readout is shown in Fig. 1.

Moreover, the value of gate biasing resistor has to be kept high in order not to degrade the detector responsivity, clearly in contradiction with the noise requirements since the gate bias resistor generates a thermal noise source increasing with increasing resistor value. Furthermore, although on-chip resistors can be achieved, their accuracy and linearity in conventional CMOS technologies remain poor, and resistors of large values cannot be realistically
implemented. The implementation in CMOS technology of the common-source MOSFET amplifier has thus emerged to be an impractical approach [7]. Others have proposed a number of alternative approaches, including diodes, DC feedback loops [8] and radiation-damaged diodes [9] to obtain the necessary high resistances. These either required an additional process or extra on-chip area, therefore increasing difficulty and/or fabrication cost.

A low-noise charge sensitive amplifier (CSA) presenting high input impedance and low power has been developed as front-end amplifier. The topology of capacitive feedback amplifier is possible since the sensing element presents a sufficiently large equivalent capacitance. The amplifier has been implemented in a standard 0.7 µm CMOS process. A fully integrated readout structure combining sensing area and preamplifier allowing for large array implementation has been designed.

In this paper, the design of an integrated low-noise CSA for pyroelectric detectors is presented. The basic theory behind signal and noise generation in pyroelectric detectors with front-end amplifiers based on CSA circuits is given in Section 2. The constraints of low-noise design in CMOS technology are exposed in Section 3 alongside the detailed analysis of the CSA design. Experimental results of the 256-pixel (16 × 16) infrared focal plane array (IRFPA) based on CSA readout are reported in Section 4.

2. Signal and noise from pyroelectric detectors with CSA readout

Signal voltage created by a change of temperature in the PVDF material can be estimated from the charge generated on the detector electrodes. A simplified representation of the analogue and thermal model of a pyroelectric sensor is shown in Fig. 2. For the purpose of signal analysis, the irradiance incident on the detector is considered as a sinusoidal modulation of angular frequency ω, and is given by:

$$P(jω) = P_0 e^{jωt}$$  \hspace{1cm} (1)

where $P_0$ is the maximum irradiance in W/m². The heat capacity $H$ and thermal conductance $G_T$ of the pyroelectric layer can be used to define the partial irradiance reaching the pyroelectric layer as a function of spatial average temperature $\bar{T}_{pvdf}$:

$$\eta P(jω) = H \frac{d\bar{T}_{pvdf}}{dt} + G_T \bar{T}_{pvdf}$$  \hspace{1cm} (2)

where $\eta$ is the emissivity of the absorbing layer. A solution to this equation is found to be:

$$\bar{T}_{pvdf}(jω) = \frac{\eta P_0}{G_T + jωH} e^{jωt}$$  \hspace{1cm} (3)

The spatial average temperature in the PVDF layer $\bar{T}_{pvdf}$ may be estimated numerically from a multi-layer thermal analysis [10]. From the spatial average temperature in the PVDF layer, the charge $Q$ developed across the detecting layer is obtained from:

$$Q(jω) = \rho A \bar{T}_{pvdf}(jω)$$  \hspace{1cm} (4)

where $\rho$ is the PVDF pyroelectric coefficient and $A$ the pixel area. The current signal representing the transfer of infrared input power $P(jω)$ into an electrical form is obtained from combining Eqs. (3) and (4) and taking the derivative with respect to time:

$$I_d(jω) = \frac{\eta P_0 jω AP}{G_T + jωH} e^{jωt}$$  \hspace{1cm} (5)

The voltage responsivity [11] is defined as the ratio of output voltage to incident irradiance as described in:

$$|\Re(jω)| = \frac{\eta P_0 \omega}{G_T(1 + \omega^2 \tau_T^2)^{1/2} G_E(1 + \omega^2 \tau_E^2)^{1/2}}$$  \hspace{1cm} (6)

where $\tau_T = (H/G_T)$ and $\tau_E = (C_E/G_E)$ represent the thermal and electrical time constant, respectively. In the electrical part of the sensor model (see Fig. 2), $G_E$ and $C_E$ represent the equivalent conductance and capacitance, respectively, of the PVDF and readout circuit. For a 9-µm
thick PVDF film, the thermal parameters of the pyroelectric layer as a function of detector area are given below:

\[ G_T = \frac{A_d}{6.4 \times 10^{-3}} \text{K/W} \text{ and } H = 20.7 A_d J/K. \]

The input impedance of the preamplifier plays a crucial role in Eq. (6) since it modifies the electrical conductance \( G_e \) and respective time constant. The need for a high input impedance circuit can be deduced from Eq. (6) where large responsivities are obtained for small values of electrical conductance. This defines an important requirement on the readout circuit for pyroelectric detectors.

The basic circuit diagram of the sensor with CSA readout is given in Fig. 3. The resistive feedback \( R_F \) has been implemented with a P-channel MOS transistor. \( R_d \) and \( C_d \) represent the detector resistance and capacitance, respectively. Due to the extremely high resistivity of PVDF (10^15), the equivalent electrical conductance \( G_e \) is mainly dependent on the readout circuit input impedance while \( C_e \) is the equivalent capacitance of the PVDF layer, the input gate of the readout circuit, and the feedback capacitor:

\[ G_e \approx \frac{1}{R_F} \text{ and } C_e = C_d || C_F || C_{\text{gate}} \]

The simplified small signal equivalent circuit used for noise analysis of the sensor with CSA readout is shown in Fig. 4, where \( i_n^2 \) represents the thermal noise generated from mean fluctuation in the detector thermal conductance. The pyroelectric layer capacitance has a dielectric loss associated with it that creates a noise current \( i_d^2 \). On the amplifier side, input referred noise voltage and current are the noise sources contributing to the detector noise, labelled \( i_n^2 \) and \( E_{n1}^2 \), respectively.

As the readout circuit presents a MOSFET input device, the parallel noise source \( i_n^2 \) can be identified as the shot noise generated by the gate leakage current, while the series noise source \( E_{n1}^2 \) at the gate is derived from input referred drain noise current. The drain noise current in MOSFET devices is arising from the sum of thermal noise from the channel resistance and Flicker noise generated from imperfections in the silicon surface. A first simplification can be made considering that practical values of gate leakage current in MOSFET devices render the shot noise contribution negligible [12]. The noise contribution from the feedback transistor is also negligible since for extremely large values of channel resistance, the corresponding noise current contribution is inversely proportional to channel resistance \( (4kT/R_F) \). The total noise contribution of the various noise sources at the input of the readout, after simplification, is given as:

\[
\frac{V^2}{\Delta f} = \frac{N^2}{\eta^2} \left( 4kT^2G_T \right) + \left( G_E + j\omega(C_d + C_F) \right)^{-2} \times \left[ \left( C_d + C_F + C_{GS} \right)^2 \right] (7)
\]

where \( k \) represents Boltzmann’s constant, \( T \) absolute temperature, and \( \tan \delta \) the dielectric loss in the sensing material. The first term describes the contribution from the thermal fluctuation noise, expressed as a noise voltage
through the sensor voltage responsivity. The second term describes the noise contribution from the dielectric noise of the PVDF and the input referred noise of the CSA readout. However, the dominant source of noise remains that of the readout circuit. Figures of merit such as the Noise Equivalent Power (NEP) are used to evaluate IR sensor performances. The NEP is defined as the ratio of noise voltage to responsivity. Therefore, the NEP is varying with respect to the input referred noise presented by the CSA. To improve the sensor performance, the NEP should be minimised, and hence amplifier input noise should be minimised.

3. Charge sensitive amplifier

The design of the CSA has been refined for noise, power and area optimisation. Unfortunately, these constraints are interdependent. In MOSFET devices, flicker noise dominates at low frequencies, and gate noise voltage has been shown to be inversely proportional to gate area [13]. Consequently, it is difficult to achieve low-noise amplifiers in CMOS technology while keeping the design area as small as possible. The structure presented here is a development of the common-source amplifier. Effectively, the use of a single input device as the primary gain stage simplifies the circuit noise analysis. A single-ended folded cascode topology has been adopted. This structure has been extensively employed for the purpose of charge amplification [14,15]. It presents the advantage of having a high DC gain and a wide band width. The DC gate bias voltage of the input device is set by means of a resistive feedback using a MOS transistor. To achieve high voltage gain, the load seen by the input cascode transistor has been implemented as a cascode active load [12].

The input device size and aspect ratio can be chosen to meet noise, gain and power requirements. A high aspect ratio increases the device transconductance, hence, increasing the gain. At the same time, increasing the channel area reduces the device flicker noise. For a given silicon area budget, values of gate width (W) and length (L) can be determined to achieve minimum noise. In this particular example, the channel width has been chosen as 1000 μm and length as 1.4 μm. This channel area yields a calculated value of input referred noise voltage of 10.4 nV/√Hz.

<table>
<thead>
<tr>
<th>Table 1</th>
<th>CSA electrical properties</th>
</tr>
</thead>
<tbody>
<tr>
<td>Property</td>
<td>Value</td>
</tr>
<tr>
<td>Open-loop gain</td>
<td>82</td>
</tr>
<tr>
<td>Input referred noise at 100 Hz</td>
<td>$1.4 \times 10^{-9}$</td>
</tr>
<tr>
<td>Band width (closed-loop)</td>
<td>5</td>
</tr>
<tr>
<td>Current consumption</td>
<td>52</td>
</tr>
<tr>
<td>Feedback capacitance</td>
<td>1</td>
</tr>
<tr>
<td>Area</td>
<td>$100 \times 125$</td>
</tr>
<tr>
<td>Power supply</td>
<td>±2</td>
</tr>
</tbody>
</table>

![Fig. 6. Noise equivalent circuits for the purpose of CSA noise analysis.](image)

![Fig. 7. CSA measured and estimated input referred noise spectrum.](image)
at 100 Hz in the process considered. Next, the device drain current may be set to meet power and speed requirements. Also, the drain current should be chosen high enough such that flicker noise contribution remains the dominant source of noise within the frequency band of interest. The amplifier current consumption is 50 μA in a 4-V voltage supply. Therefore, each readout element does not have power dissipation in excess of 200 μW.

A transistor level diagram of the CSA is given in Fig. 5. Devices M1 to M5 constitute the core of the amplifier, while \( M_F \) and \( C_F \) constitute the feedback impedance. Biasing is provided via devices \( M_{\text{bias}1} \) to \( M_{\text{bias}5} \). A voltage buffer is implemented as the output stage. The bias current reference \( I_{\text{bias}} \), idealised on the diagram, has also been implemented on chip. For the purpose of noise analysis, the circuit considered is shown in Fig. 6a. The noise analysis shows that the equivalent input referred noise voltage, with reference to Fig. 6b, is found to be:

\[
E_{\text{eq}}^2 = E_{n1}^2 + \left( \frac{g_{m3}}{g_{m1}} \right)^2 E_{n3}^2 + \left( \frac{g_{m4}}{g_{m1}} \right)^2 E_{n4}^2 + \left( \frac{g_{m5}}{g_{m1}} \right)^2 E_{n5}^2
\]

where input noise voltage and transconductance subscripts are related to transistor denomination as shown in Fig. 6. By careful design the input device noise contribution \( E_{n1}^2 \) represent 95% of the overall input referred noise voltage. The remaining 5% are contributions from devices M3, M4, and M5, and are therefore negligible. The CSA output noise under closed-loop conditions and with the detector connected to its input has been measured using the HP35660A Dynamic Signal Analyzer (DSA). A low-noise operational Amplifier from Linear Technologies (LT1028) has been used to amplify the CSA output noise to a suitable level prior to be fed into the DSA. The measured output noise is then input referred and the corresponding noise spectrum is shown in Fig. 7. Experimental results are shown to be in good agreement with the estimated values. From this data, a value of 11.4 nV/√Hz at 100 Hz has been obtained.

The core amplifier gain is equal to the product of the input device M1 transconductance and output resistance at node \( a \) (see Fig. 5). Because of the implementation of the load as a cascode active load, higher values of output resistance can be achieved than conventional active loads would allow to. An open-loop gain of the order of 80 dB has been obtained. The feedback capacitance \( C_F \) realises the closed-loop configuration in conjunction with the equivalent capacitance present at the input of the CSA, yielding a DC gain equivalent to \( C_d/C_F \). \( C_F \) has been implemented as a polysilicon implanted capacitor, with a value of 1 pF in the CMOS process employed. The input

![Common top electrode (GND) Conductive polymer](image)

9 μm pre-polled PVDF

![UV curing bonding layer](image)

Epoxy

Bottom electrodes patterned in the CMOS process

Si substrate

![Exploded view of various layers involved in pyroelectric thin film on silicon sensor fabrication.](image)
device, due to its large gate area, has been patterned in an inter-digitated structure in order to fit within the allocated sensing area. The voltage transfer characteristic \( \left( \frac{V_{\text{out}}}{V_{\text{in}}} \right) \) of the amplifier has been measured in the 0.1–10 Hz frequency band. A high-pass characteristic due to the feedback impedance has been observed. Thus, a value of about 80 GΩ has been deduced for \( R_F \). The electrical properties of the CSA implemented in the 0.7 μm CMOS process are given in Table 1. The frequency dependence of the equivalent input capacitance of the CSA and associated pixel has been measured using a HP4284A Precision LCR meter. Results of this measurement are given in Fig. 8.

4. Infrared sensor results

Pyroelectric sensors are built by bonding a pre-poled 9-μm thick PVDF film on a silicon substrate by means of UV curing epoxy. The epoxy layer is deposited by spin coating prior to the application of the pyroelectric film. A common front electrode consisting of a conductive polymer PEDT/PSS is also preliminary deposited on the PVDF thin film, and doubles as an absorbing layer. An exploded view of the sensor layers is given in Fig. 9. The pyroelectric detector material is sandwiched between two conductive layers. Individual bottom electrodes are patterned as an array in the top metal layer (aluminium alloy) in the CMOS process. A common front electrode consisting of a conductive polymer PEDT/PSS is also preliminary deposited on the PVDF thin film, and doubles as an absorbing layer. For more information on the process of applying the conductive polymer layer employed, the reader is referred to a more detailed publication on the subject [16]. The silicon substrate thickness is about 365 μm and is inclusive of a nitride-based passivation layer. The straight-forward bonding technique used allows standard CMOS technology to be employed when developing the readout circuits.

A 256-element (16 × 16) array based on the CSA read-out previously described has been implemented in the Mietec 0.7 μm CMOS process. In view of reducing the overall sensing area (pixel), CMOS readout area and sensor area have been merged in the practical implementation. This is physically achieved by reserving one of the metal layers in the process to layout the circuit, and the upper metal layer for the sensing area. A photograph of the sensor array before PVDF coating is shown in Fig. 10. The array addressing is made on-chip by a matrix of N-channel MOS single-pole double-throw switches.

The CMOS chip containing the readout circuitry is then coated with a 9-μm PVDF film. The sensor responsivity
Table 2
Pyroelectric sensor with CSA readout main figures of merit

<table>
<thead>
<tr>
<th>Parameter (at 100 Hz)</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Responsivity</td>
<td>2200</td>
<td>V/W</td>
</tr>
<tr>
<td>Output noise voltage</td>
<td>60×10^{-9}</td>
<td>V/√Hz</td>
</tr>
<tr>
<td>NEP</td>
<td>2.4×10^{-11}</td>
<td>W/√Hz</td>
</tr>
<tr>
<td>D&lt;sup&gt;&lt;small&gt;+&lt;/small&gt;&lt;/sup&gt;</td>
<td>4.4×10&lt;sup&gt;&lt;small&gt;4&lt;/small&gt;&lt;/sup&gt;</td>
<td>cm&lt;sup&gt;&lt;small&gt;3&lt;/small&gt;&lt;/sup&gt;/Hz/W</td>
</tr>
</tbody>
</table>

has been experimentally tested using a mechanically modulated and calibrated IR source (Globar element). The frequency dependence of the responsivity is shown in Fig. 11. It has been previously demonstrated elsewhere that the frequency dependence of the responsivity is comparable to that of a common-source MOSFET with a 1-GΩ bias resistor [7]. High input impedance has therefore been achieved with the CSA readout. An average responsivity of 3510 V/W at 10 Hz modulation frequency has been measured. Table 2 gives the various figures of merit obtained for the realised pyroelectric sensor. As a consequence of the input DC voltage of the CSA, output voltage drift and offset are inevitable. Similarly, offset voltages from one amplifier to another will vary in time with temperature. However, these problems can be corrected by various signal processing techniques, for instance, they can be compensated by differentiation of two consecutive readings.

5. Conclusions

A low-noise and low-power charge sensitive amplifier having a measured input noise of 11.4 nV/√Hz at 100 Hz has been reported. The CSA has been implemented in the standard Mietec 0.7-μm CMOS process through the Europractice facility. A compact and new method of layout of the readout circuit has allowed for sensing area and readout area to be merged. A 256-element (16×16) fully working array that employ the CSA has readout device has been fabricated and assessed. A voltage responsivity of 2200 V/W, a specific detectivity of 4.4×10<sup><small>8</small></sup> cm<sup><small>3</small></sup>/Hz/W and NEP of 2.4×10<sup><small>−11</small></sup> at 100 Hz modulation frequency have been attained for a sensing area of 105×105 μm. The results obtained are encouraging for the development of low-definition pyroelectric-based image sensor. The responsivity may be improved considering that the current work does not involve any insulating layer between sensing material and readout substrate. This would allow responsivities of around 10 kV/W to be obtained and beyond, and detection of objects with temperatures close to the ambient is foreseen.

Acknowledgements

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References


Biographies

Harald J. Weller was born in France in 1973. He received the MSc degree in Electrical Engineering in 1997 from Napier University. In the summer of 1996, he worked at Racal-MESL, Edinburgh, as a student engineer. He is currently a PhD candidate in Electrical Engineering at the University of Cambridge, as a research associate.

Dadi Setiadi was born in Palembang, Indonesia in 1965. He received his MSc degree in Electrical Engineering in 1991 from the Delft University of Technology. In 1995, he received his PhD degree in Electrical Engineering at the University of Twente, his thesis dealing with integrated VDF/TrFE copolymers-on-silicon pyroelectric sensors. In 1996, he became a post-doctoral fellow in the Sensor and Instrumentation Group, Napier University, UK. In 1999, he joined the Department of Engineering, University of Cambridge, as a research associate.
T.D. Binnie obtained a PhD in Solid State Physics from Heriot Watt University before employment as a Development Engineer for Hughes Microelectronics Europe. Since joining Napier University as a lecturer in Electronic Engineering in 1986, he has worked on many research and development projects. In 1991, Dr. Binnie set up the Sensor Systems Group at Napier University to work on a variety of academic and commercial contracts. The group consists of four academic staff and three full-time research staff. Dr. Binnie is a co-holder of SERC Grant Award (GR/H81016) “Traffic Representation by Artificial Neural Systems”, and program leader of EPSRC grant award (GR/K17224) “Infra red Sensor Arrays”. He has also held commercial research contracts with Shell Exploration and Production (UK), Shell Research and Hewlett Packard Research Laboratories and is a consultant to Vision Group. Dr. Binnie was appointed Reader in Sensor Systems in 1996 and is a member of the EPSRC College of Peers for Control and Instrumentation. He was joint winner of the Enterprise Oil — Heriot Watt University Environmental Award, in 1995.