Modelling and Analysis of Power-Ground Plane for High Speed VLSI System

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Abstract—This paper presents RLC equivalent model of power plane for power distribution network (PDN) in high speed VLSI system consisting of package, board, and voltage regulator module. The frequency independent RLC equivalent model can be easily integrated in any SPICE compatible circuit simulator. SPICE simulation results of the proposed RLC models for regular and irregular power-ground plane pair have been extensively verified with full wave EM simulation results. The model shows good matching when compared with EM simulation results. The proposed SPICE model substantially reduces the CPU run time that requires only few seconds for which the EM solver would have taken several hours. Effects of different geometry and material of power plane on self-impedance profile have been analyzed.

Keywords- power-ground plane model, RLC model, EM simulation

I. INTRODUCTION

This In high speed VLSI system devices operate in GHz frequency range. Due to high switching speed of these devices, power distribution network (PDN) impedance causes ripples in power supply. If PDN is not designed properly it can cause false switching or even it can damage the device permanently. Typically, a complete PDN consists of voltage regulator module, bulk capacitor, characterization board power planes, via-hole pairs, decoupling network on board, package balls, package substrate power plane, decoupling network on package substrate, die-bumps and chip power module as shown in Fig. 1. Each element of power distribution network can be represented by an equivalent RLC which affects system frequency and transient response. Quality parameters of PDN are mainly acceptable power supply drop, maximum ripples, minimum voltage level and complete network frequency response. Power integrity concept has become more important in recent times in semiconductor industry due to shrinking transistor geometry with lower voltage thresholds, increasing leakage currents, increasing transistor packaging density, increasing transistor count in a device, increasing transistor switching rate, higher device current consumption. All these demanding constraint necessitate a robust and careful design of power distribution network [1-6]. A non-optimized power plane results in degradation of device performance in terms of fan-out ability, jitter performance and eye-diagram opening issues.

Ripples in the power supply can not be avoided fully. It can only be controlled within certain limit by proper designing of PDN. One of the best ways to control ripples on power supply is to keep impedance value of PDN low enough for the entire range of frequency from DC to maximum operating frequency in the order of GHz [1-2]. At low frequency, power planes behave as capacitor and make resonance according to their cavity dimension. Without accurate modeling and simulation, it is difficult to know the resonance and antiresonance in the PDN impedance profile [7-8].

The 3-D general purpose electromagnetic (EM) simulators employ the most accurate approach for simulating PDN geometry. These simulators are accurate but slow and require large memory for simulation. They require several hours to simulate the whole PDN geometry. From the verification point of view these tools are accurate but not feasible from design point of view where for each modification simulation take longer time.

Several topologies have been reported in literature for modeling of PDN components [1], [3-4]. At the early stage of design phase, equivalent SPICE model is very useful for circuit designer as well as for PCB designer point of view as SPICE simulation gives quick simulation results. In this paper, we propose an efficient RLC equivalent model of power plane that shows good matching when compared with EM simulation results.

The rest of the paper is organized as follows: Section II presents the modeling of power-ground plane. In section III,
SPICE simulation of the power plane model is given and the model accuracy is verified EM simulated results. Finally, the conclusions are drawn in section IV.

II. POWER-GROUND PLANE MODELLING

For accurate simulation of irregular shaped power and ground plane EM simulators are used. To develop an equivalent RLC model, the irregular shaped power and ground plane is divided into the grid like structure as shown in Fig.2. Lumped equivalent model for each section of the grid known as unit-cell are represented with RLC elements. Any arbitrary shaped power-ground plane can be represented by an array of unit cells. More dense is the grid structure more accurate will be the simulation results but after a certain limit of number of grids it only consumes more CPU run time without any improvement on response.

Several topologies have been reported in the literature to model unit cell of power-ground plane. In this paper, three SPICE models of irregular shaped power-ground plane pairs T, Π and C have been analyzed and compared for better performance, as shown in Fig. 3 [1-2].

The values of the equivalent RLC elements are derived based on the transmission line properties of the unit cell. For square shaped unit cell where W is the width of unit cell, d is the dielectric separation between power and ground plane, t is thickness of plane metal layer, μ is the conductivity of material, ε_0 is the permittivity of vacuum, ε_r is the relative permittivity of dielectric layer, γ_con is the permeability of power plane conductor and tan θ is loss tangent of the dielectric.

For π-model and T-model of unit cell, equivalent capacitance and inductance between plane of unit cell is computed by (1).

\[ C = \varepsilon_r \varepsilon_0 W^2 d \]
\[ L = \mu d \]

Both DC and frequency dependent resistance accounted for loss due to skin depth is considered for power and ground plane pair by multiplying resistance with a factor of 2.

\[ R_{dc} = \frac{2}{\sigma \cdot t} \]
\[ R_{ac} = 2 \times \sqrt{\frac{\pi \cdot \text{frequency} \cdot \mu_{con}}{\varepsilon_r}} \]
\[ R = R_{dc} + R_{ac} \]

The conductance (G) that models the dielectric loss is also a frequency dependent quantity and given by (3).

\[ G = \frac{d}{2 \cdot \pi \cdot \varepsilon_r \varepsilon_0 \cdot W^2 \cdot \tan \theta} \]

For C-model square unit cell capacitance C is calculated same as for T and π-model. Velocity of a plane wave traveling between the parallel plates of the power planes is calculated as,

\[ \text{Velocity} = \frac{C_{\text{light}}}{\sqrt{\varepsilon_r}} = \frac{1}{\sqrt{LC}} \]

\[ L' \text{ and capacitance } C \text{ for power planes. The spreading inductance } L' \text{ is derived as } L' = \frac{1}{C' \cdot \text{Velocity}^2}. \]

The resistance of C-model is given by \( R' = R/2 \).

It is important while representing power and ground plane by lumped element that length of the square unit cell is properly chosen otherwise reflection error can occur due to miss-termination at boundary. To avoid reflection due to miss-termination, delay through unit-cell should be less than 1/5 of a rise time for a transient signal. For a rise time \( t_{\text{rise}} \) most of the frequency content lies within \( f_{\text{max}} \),

\[ f_{\text{max}} = \frac{0.35}{t_{\text{rise}}} = \frac{0.35}{5 \times \tau} = \frac{1}{14.3 \tau} \]

where \( \tau \) is the transmission delay. Length of the unit-cell \( L_{\text{unit cell}} \) is given by \( L_{\text{unit cell}} \leq \frac{\lambda_{\text{min}}}{14.3} \) where, \( \lambda_{\text{min}} \) is the wavelength corresponding to the \( f_{\text{max}} \). Unit cell length should be chosen according to the maximum frequency used in the
SPICE simulation and should be kept about 1/15 of the maximum frequency of interest to avoid reflection error.

III. SPICE SIMULATION ACCURACY AND ANALYSIS

To verify the SPICE model accuracy, a square power plane of 10 mm length has been taken. Material properties of the power plane are fixed as $\varepsilon_r = 3$, $d = 2$ mil, $t = 1$ mil, $\sigma = 5.87 \times 10^7$ Siemens/meter and $\tan \theta = 0.035$. RLC netlist is generated using Cadence Virtuoso schematic editor for 20x20 grid structure. RLC components are modeled according to the derived equations. The three models have been implemented and simulated using SPICE based simulator. Performances of all three models are computed and compared for accuracy and CPU run time. To measure self-impedance, 1 amp AC current source is applied at desired port keeping all other ports open, now the measured voltage on the same port will give its self-impedance. Their simulation run time for transient and AC simulation are compared in Table I. The same power plane is simulated using EM Simulator. Simulation results are shown in Fig. 4. Fig. 4 shows that accuracy of equivalent RLC models degrade from full wave EM simulation results. In C-model, equivalent RLC elements are used for both power and ground plane separately but this model cannot be applied for the geometry in which both power and ground plane are of different structure. Other than performance, T-model needs extra termination to model power-ground plane at the open boundaries which can cause unnecessary reflection at the edge. So, for better performance in term of both accuracy and CPU run time $\pi$-model provides better results than others. In this paper, $\pi$-model has been considered for power-ground pair modeling for package as well as for board.

For regular geometry model SPICE simulated results are very close to EM simulation results. Now to validate the model for irregular shaped power plane as shown in Fig. 5, full wave EM and SPICE simulation is done. Fig. 6 shows the

<table>
<thead>
<tr>
<th>TABLE I CPU RUN TIMES FOR THREE BASIC UNIT-CELL MODELS</th>
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<tr>
<td>Transient simulation time</td>
</tr>
<tr>
<td>(second)</td>
</tr>
<tr>
<td>T-model</td>
</tr>
<tr>
<td>$\pi$-model</td>
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<tr>
<td>C-model</td>
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Figure 4. Self-impedance profile comparison unit cell models

Figure 5. Layout of irregular power plane

Figure 6. Grid structure of unit cell for the irregular power plane

Figure 7. Self-impedance obtained from SPICE and EM simulation at port 1
RLC equivalent circuit for 4×4 square inch power-ground plane pair is generated considering square unit cell of width 6.35 mil. SPICE simulations are carried out for varying separation keeping relative dielectric permittivity of 4 for FR4 dielectric material, thickness of plane metal layer as 1 mil, conductivity of $5.87 \times 10^7$ Siemens/meter and dielectric loss tangent of 0.035. Fig. 8 shows self-impedance profile for different power-ground plane separation. With decrease in separation, plane capacitance and loop inductance increases and decreases with same factor as of separation, respectively. So, the resonant and anti-resonant frequencies do not change. Impedance profile is only getting wider with decreasing separation because Q-factor is decreasing in magnitude.

**IV. CONCLUSIONS**

In this paper, three different topologies for SPICE level modeling of power plane are presented. SPICE simulation results of these models are compared with EM simulation results. It is seen that π-model gives better results when we consider both simulation runtime and accuracy. The SPICE model of power plane produces same level of accuracy compared to EM simulation within few seconds. This will save large simulation time compared to EM simulation when the designer has to vary different design parameter of power plane in the early stage of design phase. The proposed modeling technique is validated for both regular and irregular shaped power plane. The characteristics of power plane in term of self-impedance profile using π-model are analyzed for varying separation, dielectric constant and dielectric loss tangent.

**REFERENCES**


