Implementation of Optimized High Performance 4x4 Multiplier using Ancient Vedic Sutra in 45 nm Technology

Diptendu Kumar Kundu[1], Supriyo Srimani[2], Saradindu Panda[3], Prof. Bansibadan Maji[4]
[1,3]Electronics and Telecommunication Department, Narula Institute of Technology, India
[2]Department of Radio Physics and Electronics, Rajabazar Science College, Calcutta University, India
[4]Professor and Head, Department of Electronics and Communication Engineering, NIT, Durgapur, India
diptendukumarkundu@gmail.com[1],srimani.supriyo@gmail.com[2], saradindupanda@gmail.com,[3]bmajiecenit@yahoo.com[4]

***Abstract*— With the enrichment of new technology in the fields of VLSI design and communication there is also a demand of high speed and low area. The aim of this paper is to design a multiplier circuit based on Vedic sutras. The algorithms based on conventional mathematics can be optimized and simplified by using Vedic sutras. In this paper we have given the design up to Multipliers based on Vedic multiplication sutra "Urdhva-Tiryakbhyam" the design of 2x2, 4x4 has been designed in DSCH2 and all the outputs have been given. The layout of those circuits has been also generated by Microwind. The internal circuit diagram of all the blocks has been explained. The noise, power have been calculated by T-Spice-13 in 45nm Technology. The hardware has also been implemented in XILINX and tested in Basys™2 Spartan-3E FPGA Board.**

***Index Terms*— Urdhva Tiryakbhyam, T-Spice, XILINX, DSCH2, MICROWIND.**

I. INTRODUCTION

A multiplier is one of the key hardware blocks in most of the digital signal processor systems. Multiplication is an operation of scaling one number by another multiplication operation such as convolution, Discreet Fourier Transform, Fast Fourier transform etc. With ever increasing higher block frequency it become necessary to have a faster arithmetical circuit with advancement in technology many researchers had tried to design multiplier which have the feature of low power consumption high speed or even combination of them. Multiplication can be implemented using several algorithms such as array, Booth, Carry save, Modified Booth and Wallace multiplier. In case of array multiplier multiplication of two binary numbers can be obtained by using a combinational logic, it performs the products of all bits at once. So it is a fast algorithm. But array multiplier requires large number of gate. So, it is not an economically designed. In CSA method bits are processed one by one to supply a carry signal to an adder. So it depends on previous carry as the number of bits increases the execution time also increases. In case of Wallace tree method three bit signals are passed to a one bit full adder which is called three inputs Wallace tree circuit. Out of this sum is supplied to the next state FULL ADDER located at the higher position. In Wallace tree method, the circuit layout is not easy although speed operation is high. The booth multiplier works at partial product, it scans three bit at a time. The two bit from the present pair, and the third bit from the higher order bit of an adjacent lower order pair. This method of Booth recording reduces. The number of adders hence the power is reduced. But as the third bit come from the other part of the partial product so present state bits have to wait for the processing so delay is increased [4]. The Sanskrit word 'Veda' means 'knowledge'. The Vedas consist of a huge number of documents called 'Ganita sutras' (the name 'Ganita' means mathematics), were devoted to mathematical knowledge. Sri Bharati Krishna Tirtha Maharaja introduce Vedic Mathematics is based on 16 sutras dealing with mathematics related to arithmetic, algebra and geometry [6].

In this paper we have designed a multiplier based on Vedic Sutra. The First section describes the basic circuits of designing a Multiplier in minimal transistor i.e. AND gate, Half Adder, Full Adder. In the next section we have discussed about the Vedic Sutra both in decimal and binary. On the basis of that we have implemented the circuit of 2x2 Vedic Multiplier. Then using that 2x2 Vedic Multiplier as a basic block we have implemented 4x4 Vedic Multiplier. Then again applying the Vedic Sutra we have implemented the 4x4 multiplier separately. All the waveforms corresponding each circuit are given separately. Noise, Power, Delay, and Area has also been calculated and given in the result analysis section.

II. CIRCUIT TECHNIQUES

Urdhva-Tiryakbhyam sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "vertically and crosswise". The main advantage of utilizing this algorithm in comparison with the existing multiplication techniques is the fact that it utilized only logical AND operation, Half address, Full address to complete the operation. Also the partial products required for multiplication are generated in parallel and a priori to the actual addition thus saving as lot of processing time. All the basic blocks are described below. The Increasing shades of Black in the blocks denote AND gate, Half Adder and Full Adder respectively in the following designed circuits.

A. AND GATE:

The AND gate is designed by 3 transistors (3T) where both

the NMOS are connected in cross-coupled manner i.e. the gate of the first NMOS (A) is connected with the source of second NMOS and vice versa. The inputs are given to the gate of each NMOS. Both the drain of NMOS are sorted and connected with the drain of PMOS. The gate and source of the PMOS are connected to ground. When the input is 00 i.e. A=0 and B=0 the PMOS is ON but both the NMOS are off so the output becomes zero. When the input is 01 i.e. A=0 and B=1 the PMOS is ON so the output becomes zero and similarly for input10 the output becomes zero. In the case of input 11 i.e. A=1 and B=1 the PMOS is off but both the NMOS are ON and the output becomes high. Figure.1 shows the circuit arrangement and the output waveform of the 3T AND Gate.

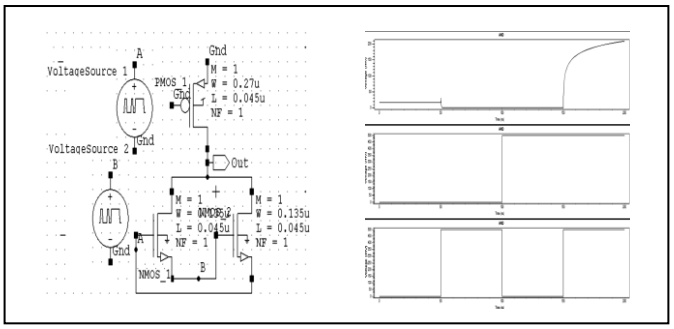

Fig. 1. Circuit Diagram and Output waveform of 3T -AND gate

B.HALF ADDER

The Half Adder is implemented by 5 transistors where Sum is generated by 3T XOR gate and the carry is generated by a mux controlled by the XOR output. The circuit diagram is shown in Fig.3. The 3T XOR operation is as follows: When the input B is at logic high, the circuit functions like a normal inverter. When the input B is at logic low, the CMOS inverter output is at high impedance. However, the pass transistor M_3 is enabled and the output Y gets the same logic value as input A. However, when A=1 and B=0, voltage degradation due to threshold drop occurs across pass transistor and consequently the output Y is degraded with respect to the input. Figure.2 shows the circuit arrangement and the output waveform of the 5T Half Adder.

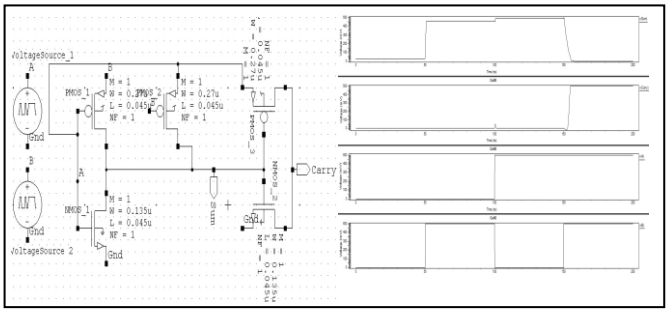

Fig. 2. Circuit Diagram and Output waveform of 5T Half Adder

C. FULL ADDER

The design of an eight transistor (8T) full adder using XOR (3T) function and the waveform of Full Adder (8T) is shown in Figure.3. 8T full adder using centralizer output condition contains three modules—Two XOR (3T) gates and one multiplexer (2T). The MUX is controlled by the output of XOR of the first two inputs.

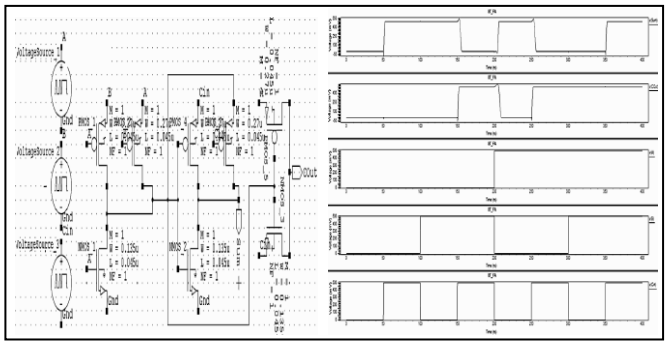

Fig. 3. Circuit Diagram and Output waveform of 8T Full Adder

Now the Multiplication Algorithm is discussed. The Urdhva Tiryakbhyam sutra is applicable for decimal system as well as for binary system. For implementing this algorithm we expressed the numbers in a different way. Such as $4\times2=8=0^8$ and $9\times3=27=2^7$. Let us consider two examples to describe the algorithm.

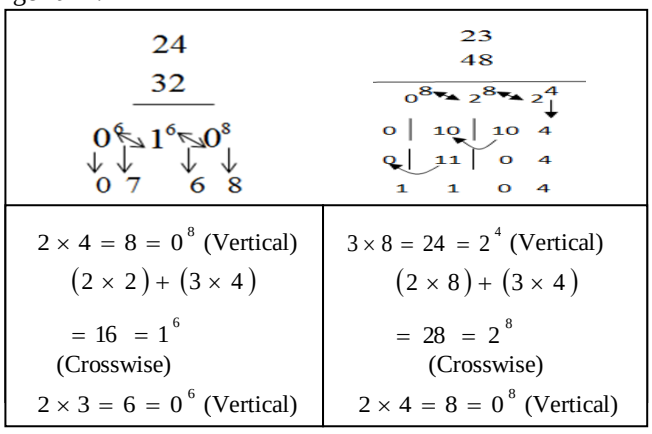

Fig. 4. Urdhva Tiryakbhyam sutra for Decimal Numbers

In the first example, No carry are generated from the previous stage i.e. 0 carry has been generated from the previous stage. But for the second example each step there is a previous carry and the carry is added to the next stage and so on. Finally we get the result.

In case of Binary the representation is slightly deferent such as $1x1=1=0^1$ and $(1x1)+(1x1)+(1x1)+(1x1)=1+1+1+1=100=10^0$ let us take as example to describe the binary multiplication.

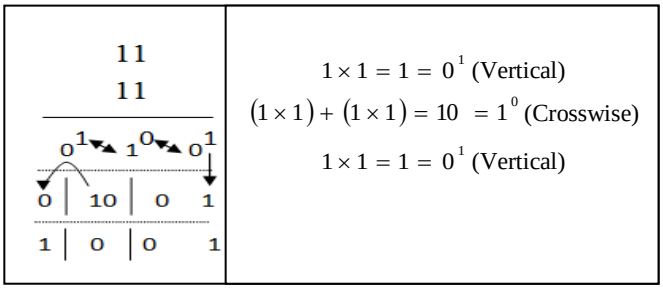

Fig. 5. Urdhva Tiryakbhyam sutra for Binary Numbers

Here the binary addition is done by half address and full address and we know any adding operator results a sum and a carry. From the representation of the number we can easily found the relation that the representation in nothing but Sum Carry .

Now from the mathematics we will deduce the circuit of 2×2 Vedic multiplier. To draw the circuit we have take two 2 bit numbers A (A_1A_0) and B (B_1B_0). In case of A_0 B_0 multiplication cases are 0x0, 0x1, 1x0, 1x1 resulting 00, 00, 00, 01, i.e., 0 0 0 1 , 0 , 0 , 0 we can see that all the MSB bits are 0 i.e. No carry is forwarded to the next stage. For the crosswise stage the product of A_1 B_0 and A_0 B_0, is passed to the half address and the carry is forwarded to the next stage where it is added with the product of A_1 B_1. From the explanation we draw the circuit given in Fig.6 and the output has been shown by glowing of LED. The VHDL output is shown in Fig.7.The layout has also given in Fig.8 also and the output of the layout is also given in Fig.9.

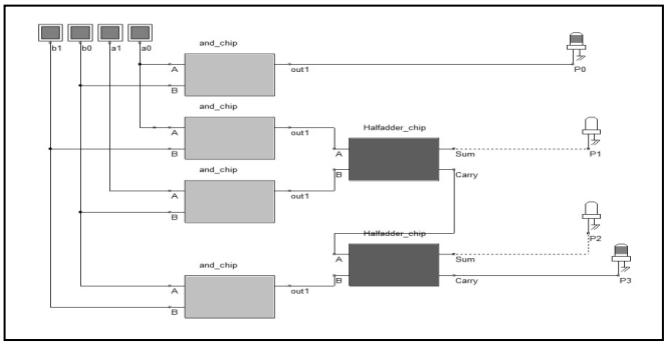

Fig. 6. Circuit implementation of 2x2 Vedic Multiplier.

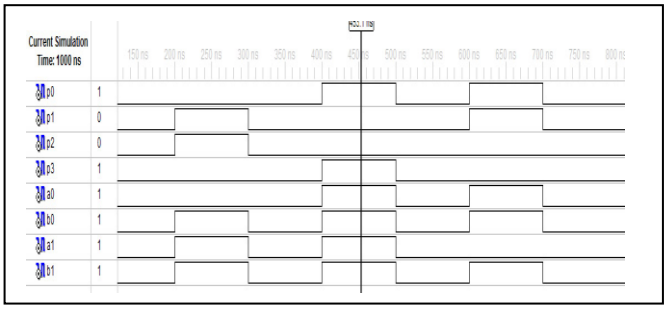

Fig. 7. VHDL Output of 2x2 Vedic Multiplier.

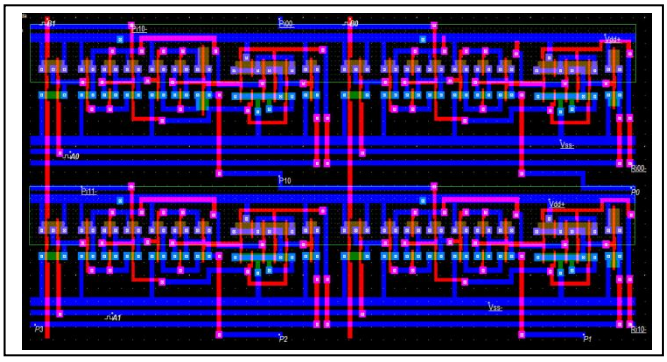

Fig. 8. Layout of 2x2 Vedic Multiplier

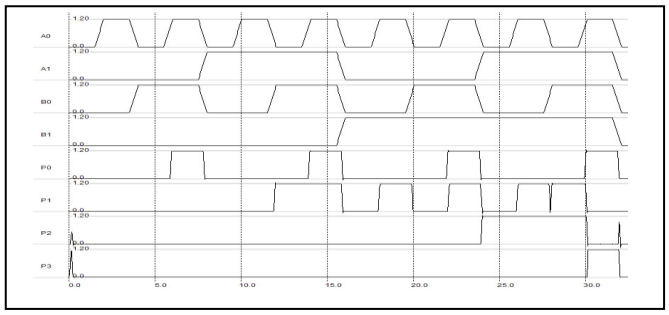

Fig. 9. Output of the Layout of 2x2 Vedic Multiplier

The total no of gates used in this 2x2 Vedic multiplier in 4 AND gates and 2XOR gates, 2 MUX. So total no of MOS used is (4x3) + (2x3) + (2x2) =22MOS.

Now we have created 4x4 multiplier using 2x2 Vedic multiplier as a basic block. Let us consider two 4bit numbers A ($A_3A_2A_1A_0$) and B ($B_3B_2B_1B_0$) to describe the algorithm.

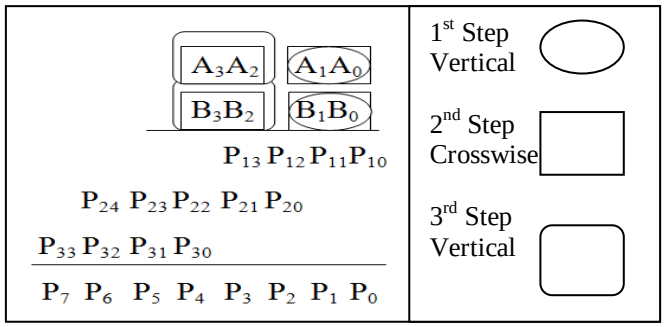

Fig. 10. Block Diagram of 4x4 Vedic Multiplier using 2x2 Vedic Multiplier

Let us take an example A (1111) and B (1111) which will verify the previous block diagram.

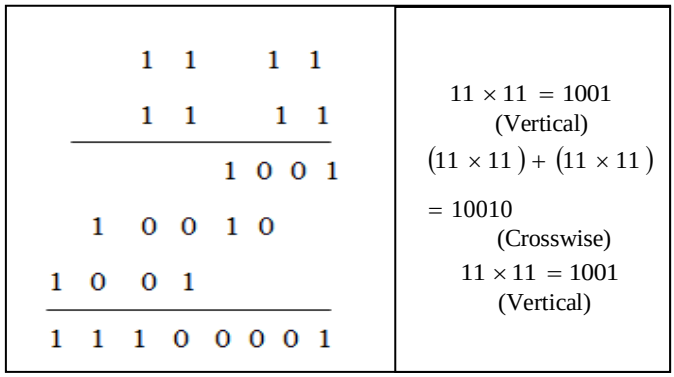

Fig. 11. Example of 4x4 Vedic Multiplier using 2x2 Vedic Multiplier

Now we can draw the circuit diagram from the above process and the circuit is shown in Fig.12. The VHDL output has been shown in Fig.13.

The total no of MOS required is 4 number of 2x2 Vedic Multiplier i.e. 4X22= 88, 4 Bit parallel added (3x2)=32, 5bit parallel adder (8X5) = 40 So in total (88+32+40) =160 no of MOS is required.

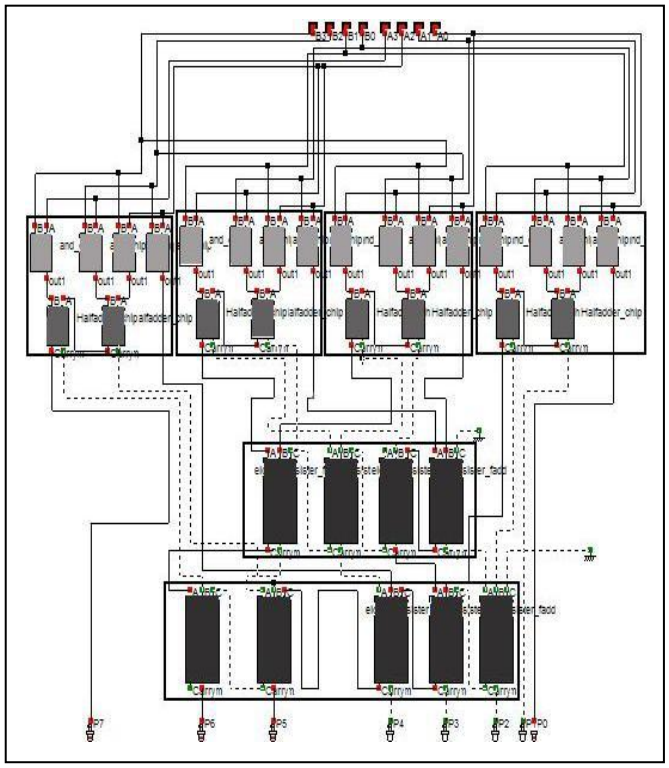

Fig. 12. Circuit diagram of 4x4 Vedic Multiplier using 2x2 Vedic Multiplier.

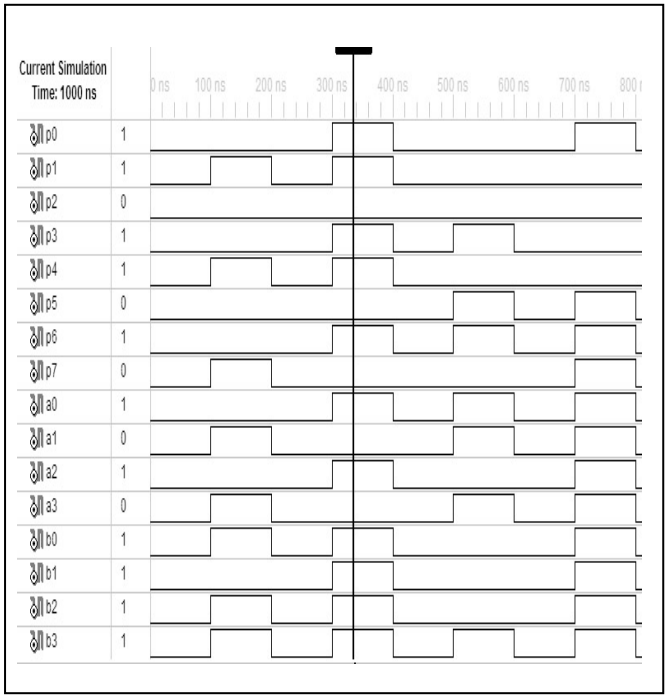

Fig. 13. VHDL Output of 4x4 Vedic Multiplier using 2x2 Vedic Multiplier

Now we have designed 4x4 Vedic multiplier using the Vedic Sutra. Let us see the algorithm first for that we have considered two no's as usual A (1111) and B (1111).

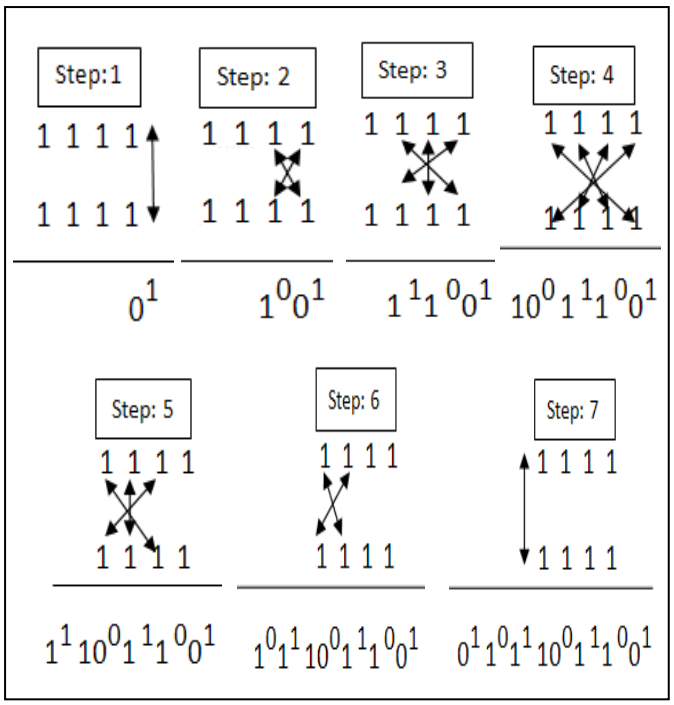

Fig. 14. Steps regarding 4x4 Multiplication using Urdhva Tiryakbhyam sutra

Now the result comes like $0^1 1^0 1^1 10^0 1^1 1^0 0^1$.For getting the final result we here used two arrows one sided arrow shows the final result and both sided arrow shows the intermediate stage and we have numbered each step using Alphabets. And for marking addition we have used the + sign Fig.15 shows the complete steps for addition and result.

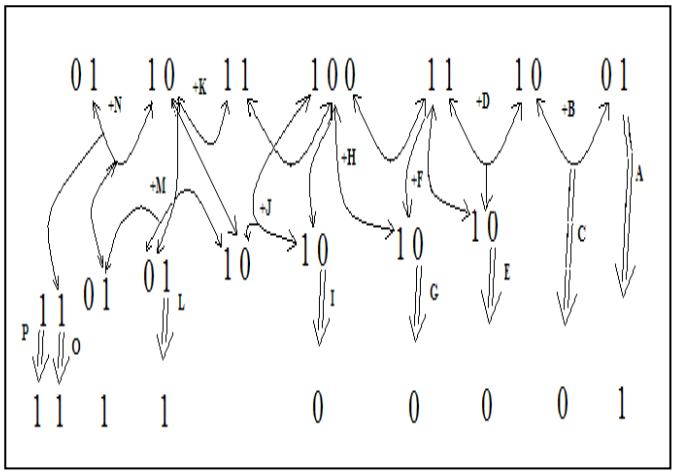

Fig. 15. Final Steps regarding 4x4 Vedic Multiplication

In the process a block is required which will add 4 bits and give us the result. The circuit that does the following function is given in Fig.16.The process has been implemented in circuit and the output has been soon via glowing of LED in Fig 17 also the layout has been drawn and the output of layout is also given in Fig.18. The VHDL output for different inputs shown in Fig.19.

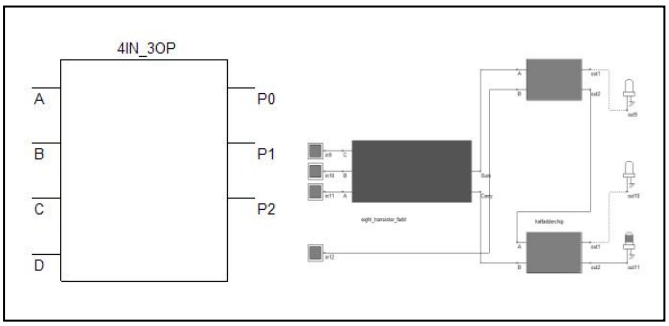

Fig. 16. Circuit that performs 4 bit addition

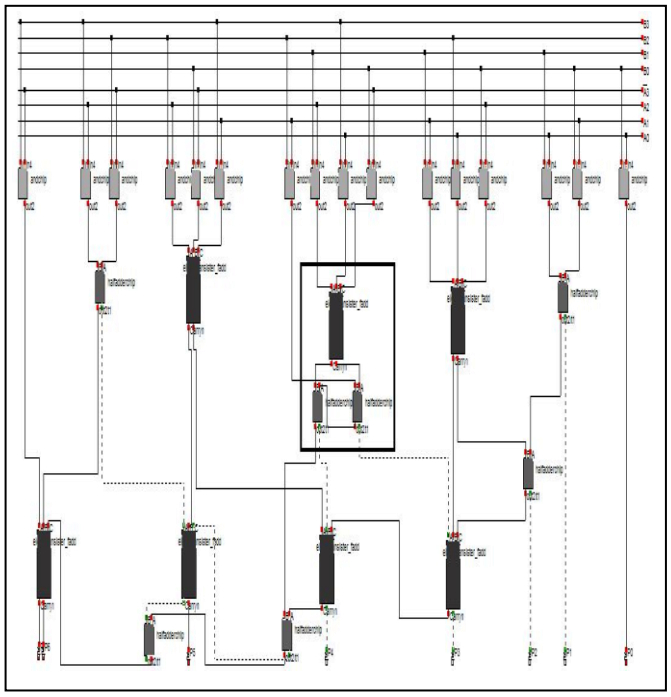

Fig. 17. Circuit implementation of 4x4 Vedic Multiplier.

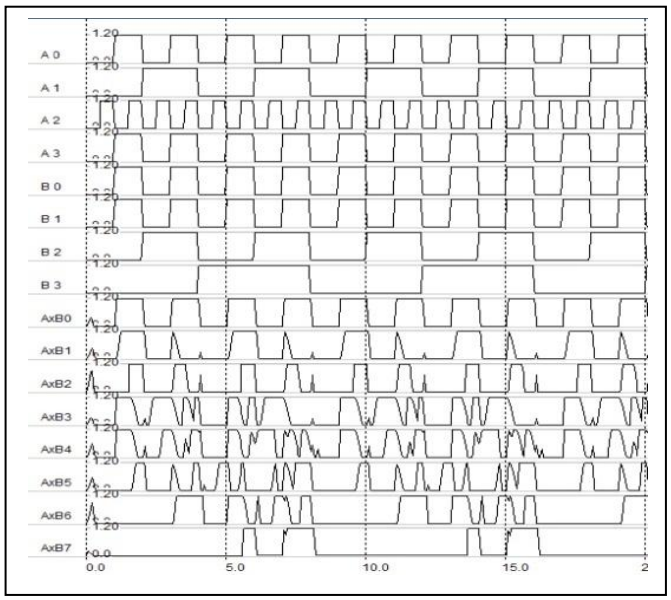

Fig. 18. Output of the Layout of 4x4 Vedic Multiplier

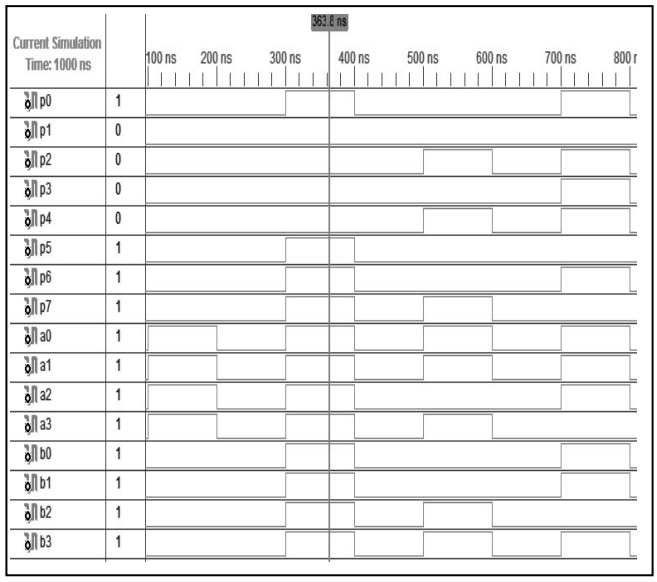

Fig. 19. VHDL Output of 4x4 Vedic Multiplier.

III. Result Analysis

The circuit of 2x2, 4x4 using 2x2 as a basic block, 4x4 Vedic Multiplier has been tested in DSCH2. The Noise, Power has been simulated in Tanner Spice-13 in 45nm Technology. The Layout has been generated in Microwind2. The input voltage is taken as 0.5V. The frequency of operation is taken as 1000MHz. The Hardware has also been tested in XILINX 10.1 and tested in Basys™2 Spartan-3E FPGA Board kit. The Area, Noise, Power and Delay of 2x2 Vedic Multiplier has been given in Table 1. The Comparison of Noise, Power, Delay, Area and Transistor count of 4x4 Vedic Multiplier with other multipliers [7] is given in Table 2.

TABLE I. RESULTS OF 2X2 VEDIC MULTIPLIER

2x2 Vedic Multiplier	OUTPUT NOISE	OUTPUT POWER	DELAY	AREA
	15µV	4.62nW	0.025nS	32*15 μm^2

TABLE II. COMPARISION OF DIFFERENT 4X4 MULTIPLIERS

MULTIPLIER NAME	CMOS BASED	GDI XOR BASED ARRAY	VEDIC MULTIPL - IER
TRANSISTOR COUNT	320	136	139
NOISE	33µV	35µV	30µV
POWER	2.12×10^{-4} W	5.52×10^{-4}W	$9.2x10^{-5}$ W
DELAY	1.08nS	2.19nS	0.060nS
AREA	6.46mm^2	6.19mm^2	5.01mm^2

IV. CONCLUTION

In the era of low power and fast electronics devices speed and power consumption is the major factor of modern industry. So, here we design a high speed multiplier following the algorithm of Urdhva Tiryakbhyam sutra of Vedic mathematics and using less number of transistors of the basic block of the multiplier we designed the circuits, for reducing the power and increase the speed. From the Result analysis we conclude that the proposed multiplier is 18 times faster, 181 less Transistor required, 2 time power efficient and 1.2 times area effective from the Conventional Multiplier. So, we state that the proposed multiplier has high speed, low power, and area efficient. As this multiplier algorithm is such that it never create any practical product and the multiplication operation is done in parallel so the delay is minimum, as the speed improve, so this multiplier can be used in any digital logical unit replacing the existing multipliers. This multiplier can easily used in digital signal processing module and also used for convolution and digital signal processing module. Used this in an FPGA kit it can be used in any digital processor, image processor etc. In future we can design higher order Multiplier using this algorithm, to develop a fast computing device.

REFERENCES

[1] Rakshith Saligram, Rakshith T.R,"Optimized Reversible Vedic Multipliers for High Speed Low Power Operations", Proceedings of 2013 IEEE Conference on Information and Communication Technologies (ICT 2013).

[2] Aniruddha Kanhe, Shishir Kumar Das, Ankit Kumar Singh," Design and Implementation of Floating Point Multiplier based on Vedic Multiplication Technique" 2012 International Conference on Communication, Information & Computing Technology (ICCICT), Oct. 19-20, Mumbai, India.

[3] Parth Mehta, Dhanashri Gawali, Conventional versus Vedic mathematical method for Hardware implementation of a multiplier, 2009 International Conference on Advances in Computing, Control, and Telecommunication Technologies.

[4] Honey Durga Tiwari, Ganzorig Gankhuyag, Chan Mo Kim, Yong Beom Cho," Multiplier design based on ancient Indian VedicMathematics", 2008 International SoC Design Conference, 978-1-4244-2599-0/08/$25.00 ©2008 IEEE.

[5] Vaijyanath Kunchigi, Linganagouda Kulkarni, Subhash Kulkarni,"High Speed and Area Efficient Vedic Multiplier"

[6] Jagadguru Swami Sri Bharati Krishna Tirthji Maharaja," Vedic Mathematics", Motilal Banarsidas, Varanasi, India, 1986.

[7] A.Daniel Raj, S.Vijayalakshmi, P.Sathyamoorthy,"Efficient Design of 4-bit array multiplier using GDI low power cell" International Journal of Computer Technology and Electronics Engineering (IJCTEE) Volume 2, Issue 6, December 2012.

[8] M. Ramalatha, K. Deena Dayalan, P. Dharani, S. Deborah Priya, "High Speed Energy Efficient ALU Design using Vedic Multiplication Techniques" ACTEA 2009 July 15-17, 2009 Zouk Mosbeh, Lebanon.

[9] Devika Jaina, Kabiraj Sethi, Rituparna Panda,"Vedic Mathematics Based Multiply Accumulate Unit"2011 International Conference on Computational Intelligence and Communication Systems.

[10] Prof J M Rudagil, Vishwanath Amble, Vishwanath Munavalli, Ravindra Patil, Vinaykumar Sajjan"Design And Implementation Of Efficient Multiplier Using Vedic Mathematics" Proc. Of Int. Conf, on Advances in Recent Technologies in Communication and Computing 2011

[11] Rakshith T R, Rakshith Saligram," Design of High Speed Low Power Multiplier using Reversible logic: a Vedic Mathematical Approach", 2013 International Conference on Circuits, Power and Computing Technologies [ICCPCT-2013]

[12] Prabir Saha, Arindam Banerjee, Partha Bhattacharyya, Anup Dandapat,"High Speed ASIC Design of Complex Multiplier Using Vedic Mathematics", Proceeding of the 2011 IEEE Students' Technology Symposium14-16 January, 2011, lIT Kharagpur.

[13] L. Sriraman, T. N. Prabakar,"Design and Implementation of Two VariableMultiplier Using KCM and Vedic Mathematics", 1st International Conf. on Recent Advances in Information Technology I RAIT -2012.

[14] Hanumantharaju M.C, Jayalaxmi .H, Renuka R.K, Ravishankar .M,"A High Speed Block Convolution using Ancient Indian Vedic Mathematics" International Conference on Computational Intelligence and Multimedia Applications 2007.

[15] M.E.Paramasivam,Dr.R.S.Sabeenian,"An Efficient Bit Reduction Binary Multiplication Algorithm using Vedic Methods",978-1-4244-4791-6/10/$25.00_c 2010 IEEE.