Abstract
A new silicon based multi chip white LED PKG for high power application is designed, fabricated and tested. The package is composed of Al layer coated reflector cup, silicon base which has micro through via hole for interconnection, and micro lens. Compared to the most conventional single chip LED PKG, multi chip white LED PKG has many advantages in cost, density, size, thermal resistance and optical efficiency.

After numerical analysis, silicon based multi chip LED PKG which has 9mm X 9mm with 0.65mm size is fabricated using simple MEMS technology.

The thermal resistance of this new silicon package was about 4-5K/W from junction to case in simulation and this result could be comparable to that of other high power LED package. Also, this PKG platform has over than 60% increase in optical extraction efficiency.

The proposed multi chip LED PKG can find applications, such as a next generation solid state lighting, back light units etc. and etc.

1. Introduction
Light emitting diodes (LEDs) not only significantly reduce power consumption compared to incandescence, but also with longer lifetime, fast response speed, compact size, low maintenance cost and grater reliability. Therefore, they have gained widespread use since their inception in the early 60's. Moreover, special deposition techniques have made possible LEDs with much higher brightness than traditional devices. This opens up many new applications such as backlighting for displays, automotive lighting and new consumer products like flash for mobile camera or compact projects [1-4].

Nevertheless these possibilities, there are some remain problems like optical efficiency, thermal resistance, cost and brightness to completely substitute the conventional solid-state lighting like a fluorescent light, incandescent lights. Many researches are progressed to ameliorate the problems stated above in various fields. But most of the previous researchers on high brightness LEDs have focused on how to improve the chip characteristics [2,4]. Few of them discussed the package point of view. Among them, optical efficiency, multi chip package issue and cost are the representative problems to be improved before everything for commercializing. In LEDs, silicon based multi chip package is produced to overcome the problems related to the optical efficiency, thermal resistance, multi chip package issue and cost using lead frame type conventional package. However the conventional packages like lead frame type have the limitation of accuracy, cost, thermal resistance and expansion to the multi chip packaging [5]. Through suggested silicon based multi chip LED packaging, wafer level fabrication & packaging technology is realized. It can not only solve problems of conventional packaging structures but also tremendously improve the optical properties of LED packaging like optical efficiency, reduce the manufacturing cost of LED package using WLP (wafer level packaging) and increase the expansion possibility module package using silicon based platform.

In many research fields, MEMS (Micro Electro Mechanical System) technology is used to accomplish silicon based LED PKG structure which can be applied wafer level fabrication and packaging. However the existing LED package structures have critical problem which the color mixing for white color is difficult because of its difficulty of expansion limitation for discrete lead frame type package. Multi chip package for high power LED application like solid-state lighting are required that optimized chip distance for color mixing, high performance of thermal resistance and high optical extraction efficiency. Among various fabrication methods for multi chip LED package, lead frame type package and ceramic based package are generally used [5]. In case of lead frame type package, it has difficulty in expansion possibility for arrayed package. Additionally, it has high thermal resistance compared with another packaging technology. Ceramic based package has difficulty for expansion possibility for arrayed package because of its warpage in firing process. However, due to a lot of research in semiconductor fabrication process, silicon based LED package has many advantage like expansion possibility for arrayed package, thermal resistance, mass production, cost and so on. In this study, the new silicon based multi chip package is investigated. 9mm x 9mm with 0.65 thickness package array is fabricated and optimized chip distance is determined.

2. Design.

2.1 Design Concept for Silicon Based Multi-Chip Package.
Compared with conventional discrete LED package which based on phosphor, multi chip white LED package structure needs different concept of electrical, optical, and thermal design. So in this paper, new package concept is considered. The purpose of this paper is realized optimized high efficiency white LED package. This new LED package is composed of 4 LED chips (RGGB), Al coated reflector cup, and Cu plated trench for heat dissipation. Usually, green chip has lower lightness compared to blue & red chips. So 2 green chips are arrayed in 1 cavity. Aluminum has good reflectivity in visual wave length (over than 80% in reference). So Al is
coated on reflector surface. Because copper has superior thermal characteristics compared to silicon, Cu thermal trench is located below all of chips. Figure 1 shows schematic diagram of multi chip white LED package based on silicon fabrication technology.

Figure 1. Schematic diagram of multi chip white LED package.

2.2 Design for Optical Extraction Efficiency

For white LED package which has high efficiency and exact color rendering index (CRI), chip to chip distance, reflector and lens structure, size are considered. Chip to chip distance is most important value for exact white color.

Rectangular micro lens is adopted. Applying silicon fabrication process to get the LED packaging, rectangular shape microlens has more advantages than conventional circular shape microlens like high optical efficiency. Generally, the shape of cavity which is fabricated using KOH (Potassium hydroxide) or TMAH (Tetramethylammonium hydroxide) wet etching is generally rectangular in silicon wafer. It depends on silicon’s crystal structure. Applying the circular microlens to the rectangular cavity, the inscribed circle or circumcircle shape may be the most suitable suggestion. In Figure 2, (a) and (b) mean areas happened the optical loss when lens is the inscribed circle and circumcircle shape respectively. In case of the inscribed circle (a), it has to have lower fill factor between cavity and lens than rectangular lens. Its fill factor is always 0.785 regardless of length of cavity and lens diameter. High fill factor in packaging can improve the extraction efficiency of LED through reducing the optical loss. In case of circumcircle shape (b), it also has some disadvantages. First of all, the size of circumcircle is larger than area of cavity. Due to its size, the fill factor of LED packaging is diminished. It means fewer chips can be located in the same dimensions. It can give rise to a decrease of brightness of whole LED packaging and is serious problem for solid-state lighting applications. Second it must have lower optical efficiency. Generally light extracted from the LED chip experiences the several times reflection in the LED packaging before extrication from LED packaging. During the reflection, the area which is part (b) in figure 2 between lens and cavity contributes the reduction of the optical efficiency.

In case of white LED for solid state lighting application, power efficiency is showed radiant efficiency and wall-plug efficiency. The power efficiency is founded to be next equation.

\[
\eta_{power} = \frac{P}{IV} \quad \text{(Optical power emitted into free space)}
\]

\[
\eta_{power} = \eta_{external} \cdot \eta_{feeding}
\]

(1)

Where \(\eta_{external}\) represent external quantum efficiency and

\[
\eta_{feeding} = \frac{h\nu}{qV}
\]

represent feeding efficiency

The external quantum efficiency is founded to be next equation.

\[
\eta_{external} = \frac{P}{I \cdot e} \quad \text{(\# of electrons passed through LED)}
\]

\[
\eta_{injection} = \eta_{in.} \cdot \eta_{extraction}
\]

(2)

Where \(\eta_{injection}\) represent fraction of the electrons passed through the LED that are injected into the active region and \(\eta_{in.}\) represent ratio of the number of electron-hole pairs that recombined radiatively to the total number of pairs that recombined in the active region.

Finally, extraction quantum efficiency is expressed next equation.

\[
\eta_{extraction} = \frac{\# \text{ of photons emitted into free space per second}}{\# \text{ of photons emitted from active region per second}}
\]

(3)

In order to have high optical efficiency, reflector width, reflector thickness, and chip to chip distance is optimized. After numerical analysis using commercial 3-D simulation...
programs, 5.9mm of reflector width, 0.38mm of reflector thickness, and 0.9mm of chip to chip distance have been chosen. This value is considered geometrical limitation. Figure 3, 4 and 5 are show calculated simulation results.

2.3 Design for thermal resistance

In temperature point of view, it is very critical parameter in LED chip efficiency like flux, wavelength, forward vias voltage, and life. Internal chip temperature is estimated through parameter of thermal resistance. Case of multi chip white LED package, several LED chips are arrayed in limitation space. So chip array is more important parameter compared with conventional discrete LED package.

Thermal resistance is ratio of temperature raising on device to power consumption. This concept is expressed in figure 6.

\[
R = \frac{\Delta T}{Q}
\]

Where \( T_1 \) [K] represent temperature at node 1, \( T_2 \) [K] represent temperature at node 2, \( Q \) [W] represent heat flow, and \( R \) [°C/W]

In conventional single chip LED package case, the point which is applied electrical power is same point which is raised temperature. But in multi chip white LED package, the point which is applied electrical power is different point which is raised temperature. So, thermal resistance in multi chip package is re-defined.

\[
\Delta T = \sum_i \Delta T_i = \sum_i R_{ij} W_i
\]

Equation (5) is found that

\[
\Delta T = RW
\]

Thermal resistance of j chip is found to be next equation.
\[ R_j = \frac{\Delta T_j}{\sum_i W^i} \] (7)

Where \( W = \sum_i W^i \), \( \Delta T_j \) represent total power consumption which applied in package, and rising temperature of \( j \)-th chip.

In solid state lighting case, individual chips are applied different current. It happens by white balancing. In this paper, we applied 0.9W, 0.45W, 0.45W, and 0.2W power for red, green, green, and blue chip.

After numerical analysis using commercial 3-D simulation programs, red chip has a largest thermal resist, 6.2°C/W. Figure 8 shows this result.

During the parametric study, chip to chip distance, thickness of package, width of package, and thermal interface material (TIM) were chose the effective factor. And considering the optical extraction efficiency design results, we decide the parameter: chip to chip distance is 0.9mm, thickness of reflector cup is 0.35mm, and width of package is 9mm.

### 2.4 Design of silicon based multi chip LED package.

After optical and thermal analysis, as we mentioned above, the silicon based multi chip LED package which has 9mm x 9mm with 0.7mm thickness is designed. This package is composed 4 chips (1 red, 2 green, and 1 blue) in 1 cavity. 2 green chips are parallel connected on top surface. Total 5 masks are used for fabrication.

Au layer is chosen for anode and cathode on top electrode. This layer is used for chip die attach. Except electrode, top surface is coated Al layer for increasing reflectivity.

Figure 9, 10 and 11 show top view, bottom view and cross section view of package.
3. Fabrication.

Figure 12 shows simplified fabrication process to realize silicon based multi chip LED package. This process is composed two wafer process, one is base substrate process and the other is reflector cup process.

Base substrate fabrication starts with a <100> silicon wafer. First step is dry etching for bottom pad, trench, and via hole using ICP equipment. Etch depth is 20um, 150um, and 280um (a, b, c). The via hole diameter is 80um. Oxide is coated on etched wafer using oxidation process. This step makes insulation layer (d). The layer of Ti/Au is sputtered for seed layer. After this deposition process, Cu is electro plating for interconnection (e). After polishing process (f), Al layer is deposited in top surface for increasing reflectivity (g). Next step is Al, Au layer patterning process. Metal layer is patterned using standard photolithography and wet-etched in Al/Au etching solution (h). The last step in base substrate process is Au/Sn patterning process, which is performed for eutectic bonding with base substrate and reflector cup substrate.

Reflector cup process start with a <100> silicon wafer on which has a 1500 A thickness silicon nitride film. First step is anisotropic wet etching of silicon (Si) for reflector using THAH (Tetramethyl ammonium hydroxide) solution. Etch depth is 350 µm (a, b). The layer of Ti/Au is evaporated for eutectic bonding layer (c). The last step is metal deposition process for increasing reflectivity. According to this deposition process reflector which has reflectivity, over 70% at all wave length is realized. This result shows in figure 13. Finally, figure 14 shows the realized multi chip LED package.
Conclusions

A new concept of multi chip LED package which is composed Al coated silicon reflector, 80um diameter via hole, and thermal trench for heat spreading have been founded to be suitable structure for solid state lighting application. We obtained 9mm x 9mm with 0.65 thickness package. This package is realized with simple wafer level package technology. The thermal resistance of this new silicon package was about 4–5K/W from junction to case in simulation and this result could be comparable to that of other high power LED package. Also, this PKG platform has over than 60% increase in optical extraction efficiency.

The proposed multi chip LED PKG can find applications, such as a next generation solid state lighting, back light units.

References