Impact of Patterning Strategy on Mask Fabrication Beyond 32nm

Shoji Mimotogi, Tomotaka Higaki, Hideki Kanai, Satoshi Tanaka, Masaki Satake, Yosuke Kitamura*, Katsuyoshi Kodera, Kazutaka Ishigo, Takuya Kono, Masafumi Asano, Kazuhiro Takahata and Soichi Inoue

Process and Manufacturing Engineering Center, TOSHIBA CORPORATION Semiconductor Company

8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan
Phone: +81-45-776-5212 FAX: +81-45-770-4102
E-mail: shoji.mimotogi@toshiba.co.jp

Abstract

Mask specifications of the pitch splitting type double patterning for 22nm node and beyond in logic devices have been discussed. The influences of the mask CD error and the mask induced overlay error on wafer CD have been investigated in both cases of bright field and dark filed. The specification for intra-layer overlay alignment is much smaller than inter-layer one. The specification of mask CD uniformity for dark is more challenging. In order to overcome the technology gap between single patterning and double patterning, many things will have to be improved.

Keywords: double patterning, mask specification, low-k1 lithography, 22nm node

Introduction

Optical lithography will soon meet the resolution limitation. Immersion lithography has extended the limitation of optical lithography. However, the numerical aperture of immersion scanner will soon reach a ceiling. To extend the optical limitation, we will have to use some process techniques such as double patterning, pitch splitting, spacer process, double exposure and so forth.

The k1 factor is becoming small as the technology node advances: k1=0.4 for 45nm, k1=0.35 for 32nm. Eventually, k1 is below 0.25 for 22nm logic node. We are now constructing the patterning strategy for 22nm logic node. Mask specifications are strongly affected by the patterning strategy. Appling the double patterning such like pitch splitting make a big difference in location accuracy of EB writing. To minimize the cost including mask fabrication, we have to select the method of double patterning.

In this presentation, we will provide the patterning strategy and mask spec and discuss the cost effectiveness.

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Patterning Strategy for 22nm node and beyond

In this section, the patterning strategy for 22nm and beyond in logic devices are discussed. Figure 1 shows the relationship between minimum half pitch and numerical aperture using ArF exposure tool. The k1 value is called process factor and the minimum value is 0.25. The theoretical resolution limit is on the 0.25k1-line. However, the actual resolution limit is higher k1-value, about 0.35 for L/S, about 0.40 for C/H. The maximum NA of ArF water immersion tool is 1.3 or 1.35. High index immersion has many problems so far and EUV lithography will take much time to be ready. To resolve the 35nmL/S for 22nm node with single patterning, the hyper NA tool with over 1.8 is needed. As there is such a NA limitation, we have to consider the "double patterning" method. The "double patterning" can make the resolution limit extend to 0.25k1 and beyond. Table 1 lists the intermediate metal half pitch and lithography candidates for each node. We can use water immersion for 45nm and 32nm node. There are several candidates for 22nm and 16nm node, "double patterning" with water immersion, EUV lithography, high index immersion and so on. We will focus on the double patterning as one of the candidates for 22nm and beyond.

Figure 2 shows the classification of "double patterning" processes. We can classify the double patterning process into two types. One is "edge patterning", and another is "pitch splitting". In the edge patterning process, spacer process and double development process have been proposed. In spacer process, after dummy patterns are built, sidewalls are made on each side of dummy patterns. In double development process, using positive-tone development and negative-tone development, we can obtain the double frequent patterns.

There are two types in pitch splitting process, such as dark field and bright field. In the pitch splitting process, target patterns are divided into two masks. The process flow includes first imaging, hard-mask transfer, resist-coating and second imaging. The pattern has randomness in logic devices, especially, in metal layer, the pattern layout is complicated. Therefore, we'd like to shed light on the pitch splitting process from the viewpoint of mask spec.

Target design rules for 22nm node are listed in Table 2. In AA and M1/Mx layer, minimum pitch is 70nm. In GC and CS/Via layer, minimum pitch is 90nm. The GC-pitch can be relaxed to the contacted pitch where one contact hole is between gates. The pattern layout of GC is relatively simple. Thus, not only the pattern dividing but also the spacer process might be used in this layer. In the other layer, the pitch splitting might be useful method due to the layout complexity. Thus, we will further focus on the line and space pitch splitting because of the tight design rules.

Mask Specification

We discuss the mask specification for pitch splitting type double patterning as one of the most difficult technologies in 22nm node. Figure 3 shows the typical process flow of pitch splitting. Left side is bright field process and right side is dark field process. Process flow is as following. First, first imaging is done using first mask. After development, resist trimming or shrinking is done. Then second imaging is done using second mask. At that time, there is overlay error between the first

imaging and the second imaging. The overlay error causes the space CD difference in bright field case. In dark field case, the overlay error causes the line CD difference. Thus, the overlay error degrades the CD uniformity.

A formula of CD variation in the pitch splitting process is proposed [1]. In case of the bright filed, CD variation are denoted by the following equations,

$$\left[3\sigma(Line)\right]^2 = (3\sigma_{Litho})^2 + (3\sigma_{Trim})^2 + (3\sigma_{HM})^2 + (3\sigma_{RIE})^2 + \frac{9}{4}(L_1 - L_2)^2 \quad (1)$$

$$\left[3\sigma(Space)\right]^2 = 9OVL_0{}^2 + (3\sigma_{OVL})^2 + \frac{1}{2}\left\{(3\sigma_{Litho})^2 + (3\sigma_{Trim})^2 + (3\sigma_{HM})^2\right\} + (3\sigma_{RIE})^2 \quad (2)$$

where L_1 is the final line CD in the first patterning and L_2 is the final line CD in the second patterning. The σ's are the components of CD variation in each process step. The OVL_0 and σ_{OVL} denote the mean error and deviation from mean in overlay between the first patterning and second patterning, respectively. The space CD is directly influenced by the overlay error, as described in equation (2). In case of dark field, CD variation are denoted by the following equations,

$$\left[3\sigma(Space)\right]^2 = (3\sigma_{Litho})^2 + (3\sigma_{Shrink})^2 + (3\sigma_{HM})^2 + (3\sigma_{RIE})^2 + \frac{9}{4}(S_1 - S_2)^2 \quad (3)$$

$$\left[3\sigma(Line)\right]^2 = 9OVL_0{}^2 + (3\sigma_{OVL})^2 + \frac{1}{2}\left\{(3\sigma_{Litho})^2 + (3\sigma_{Shrink})^2 + (3\sigma_{HM})^2\right\} + (3\sigma_{RIE})^2 \quad (4)$$

where S_1 is the final space CD in the first patterning and S_2 is the final space CD in the second patterning. The line CD is directly influenced by the overlay error, as described in equation (4).

Total CD budget has to be constructed by using equations (1)-(4). We showed an example of CD budget for pitch splitting process in case of bright field case in table 3. This is for 22nm and the final CD is 35nmL/S. First column is difference of mean values between the first patterning and the second patterning. Second column is deviation from mean value. Final column in Table 3 is mean difference plus 3sigma. The deviations for line and space are calculated by using the equations (1) and (2). Total CD budgets for line and space are 15% in the final CD. Lithography-related CD budget is listed in Table 4, based on the total CD budget. Total litho CD budget is 10% or 3.5nm in 3sigma. The mask CD budget is 6.5% or 2.275nm in 3sigma. Total overlay error in 3sigma is 2.5nm on wafer. Mask induced overlay error is allowed 2.0nm in 3sigma on mask.

Figure 5 shows the alignment tree of double patterning for 22nm node. For example, the intermediate levels are illustrated in Fig.5. The left side is single patterning case. The overlay accuracy is denoted by 3s. In this case, M2 is simply overlaid to V2 layer. In double patterning case, first M2 imaging M2(1st) is overlaid to average position of V2(1st) and V2(2nd). Second M2 imaging M2(2nd) has to be overlaid to M2(1st) due to its tight overlay spec as shown in Table4. Inter-layer overlays of double patterning, such as M2(1st)-V2(1st) or M2(1st)-V2(2nd), are a little larger than 3s. Inter-layer alignment such as M2(2nd)-V2(2nd) is larger than 3s because of indirect-overlay. The specifications of overlay in 3sigma are shown in Table 5. The specifications for Inter-layer alignment are required from cross-sectional assumption. The specification for intra-layer is required from CD budget described above. The specification for intra-layer overlay

M2(1st)-M2(2nd) is very challenging.

Figure 5 shows how to decide the amount of the trimming or shrinking for 22nm node. The graph in Fig.5 represents the lithography window with +/- 3.5nm resist CD tolerance at 140nm pitch. The exposure condition is described in Fig.5. The lithography window strongly depends on the resist CD. Our criterion for lithography window is 5% exposure latitude. Thus, we can set the resist CD within the range from 50nm to 90nm in resist line CD. In bright field case, we decide to set the resist line CD 50nm. In dark field case, we decide to set the resist space CD 50nm. The summary of litho CD, biasing amount, final CD is listed in Fig 5. Thus, the amount of trimming or shrinking is about 15nm. Figure 6 shows the mask spec of CD uniformity for 22nm node. As the slice level is low for 50nm line, MEF is not so large. As the slice level is high for 50nm space, MEF is so large. The amount of +/-6.5%CD is assigned to mask CD error budget. Taking account of the MEF, we calculate the spec of mask CD error. The specification for dark field case is more challenging.

Figure 7 shows the summary of mask specification. The lines in Fig.7 denote shrink trend of O/L and CDU, respectively. The shrink trend is 70% by advancing node. Our requirement for mask specification rapidly shrinks for 22nm node. Especially, the specification of alignment error is very hard. In order to overcome the technology gap between 32nm and 22nm node, we will have to do many things.

Cost Estimation

Figure 8 shows the number of ArF exposure and the cost estimation for patterning. Number of ArF-Imm exposure rapidly increases for 22nm node due to double patterning. Thus, the process cost increases. As the design rule shrinks, the chip area that has same function shrinks. The defect induced yield increases as chip size shrinking. Since the die cost is defined as the cost to obtain same function, the die cost is not so expensive in 22nm and beyond.

Conclusions

We discussed the mask specification of pitch splitting type “double patterning” in logic devices as one of the candidate for 22nm node and beyond. The specification for intra-layer overlay error is estimated from the total CD budget. The specification for mask CD uniformity is estimated from the lithography window and CD budget. The specification for intra-layer overlay error is much smaller than inter-layer one. The specification for the mask CD uniformity in dark field is more challenging than that in bright field. Also, we estimated the cost of the double patterning. Although the double patterning is thought to be double cost, the die cost is not so expensive.

References

[1] Mircea Dusa et al., ”Pitch doubling through dual-patterning lithography challenges in integration and litho budgets”, SPIE6520 65200G,2007

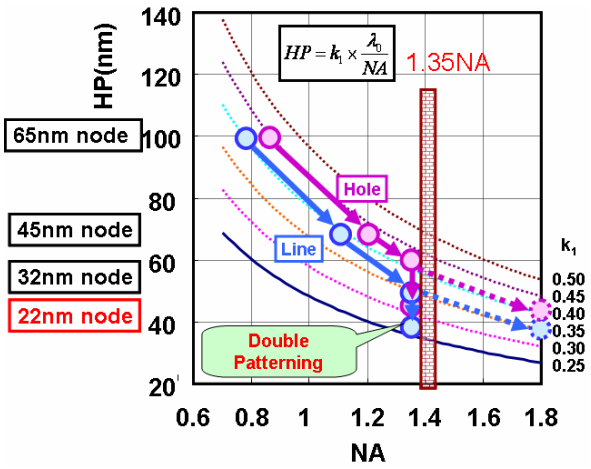


Figure 1. Relationship between half pitch and numerical aperture using ArF exposure tool with various k_1-factors

Node	IM-Metal HP(nm)	Lithography Tool
65nm	100	ArF-Dry
45nm	70	ArF-Imm.
32nm	50	ArF-Imm.
22nm	35	DPT/EUV/HII/etc.
16nm	25	DPT/EUV/HII/etc.
11nm	17	EUV/etc.
8nm	12	EUV/etc.

Table 1. Lists of the ground rule (IM-metal half pitch) and lithography candidates for each node.

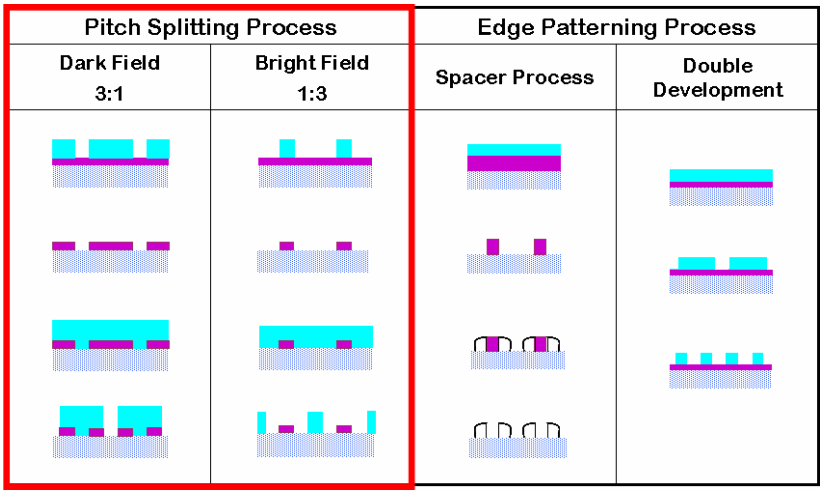


Figure 2. classification of "double patterning" process.

	Min. Pitch	Double Patterning Method	
AA	70nm	Pitch Splitting	Bright Field
GC	90nm	Pattern Dividing or Edge Patterning	Tip-to-tip cutting or Spacer Process
CS/Via	90nm	Pitch Splitting	Dark Field
M1/Mx	70nm	Pitch Splitting	Dark Field

Table 2. Patterning strategy of each level for 22nm node.

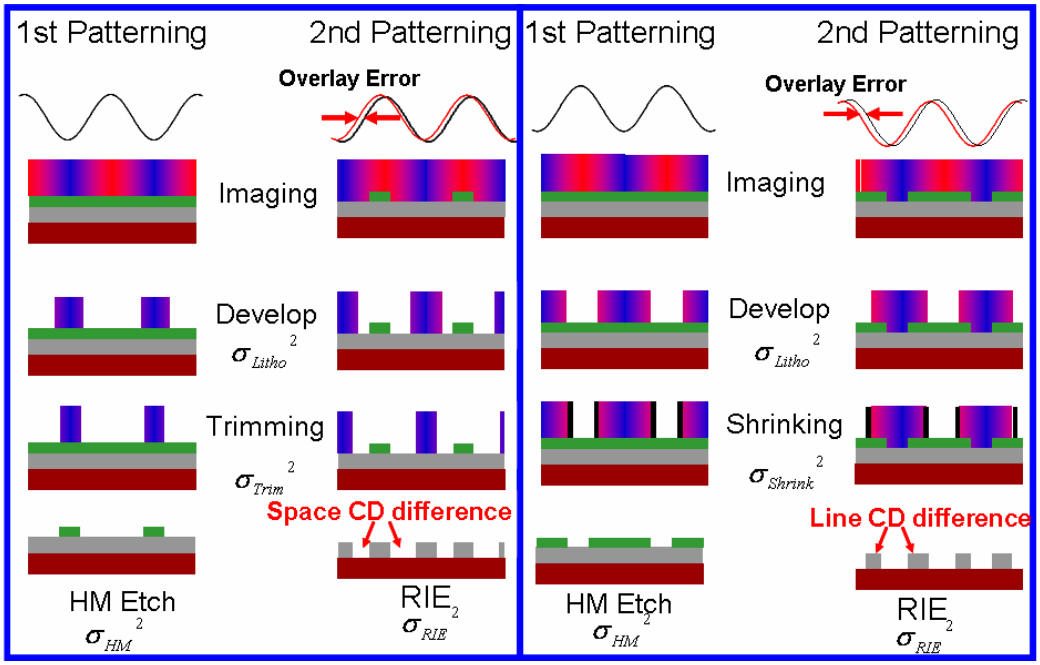


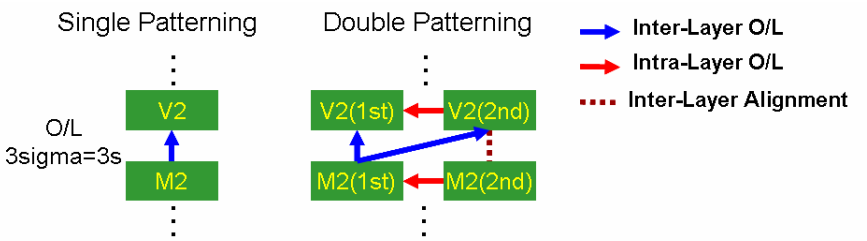
Figure 3. Process flows of pitch splitting. The left side is bright field case and the right side is dark field case.

	$\|\Delta mean\|$(nm)	3σ (nm)	$\|\Delta mean\|+3\sigma$ (nm)
Litho	0.21	3.50	3.61
Trimming	0.21	1.05	1.16
HM	0.21	1.05	1.16
L1-L2	0.63		
OVL	0.49	2.45	2.94
RIE	0.21	2.63	2.84
Line	0.53	4.72	5.24
Space	-0.53	4.72	5.25

Table 3. Total CD budget for "pitch splitting" process.

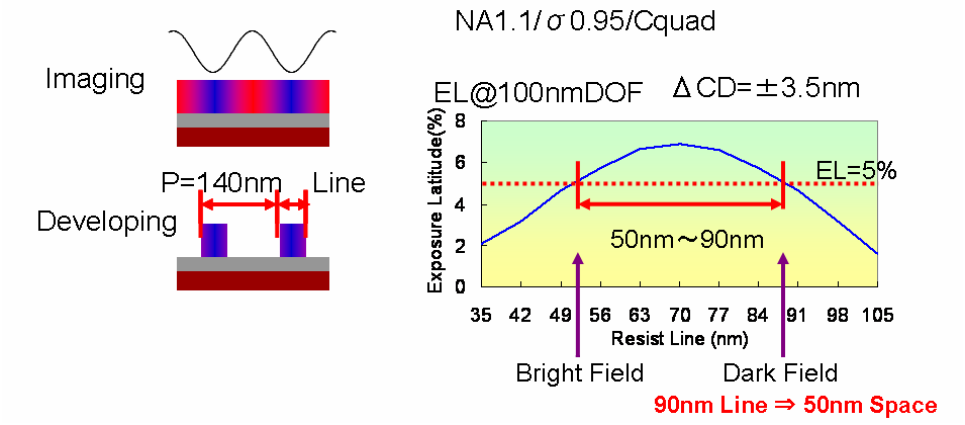
Item			±%	± nm
CDU	Total		15	5.25
	Litho In 3sigma	Total	10	3.50
		Mask	6.5	2.275
		Non-Mask	3.5	1.225
Overlay In 3sigma		Total	100	2.5
		Mask	20	2.0

Table 4. Lithography related CD budget for "pitch splitting" process.



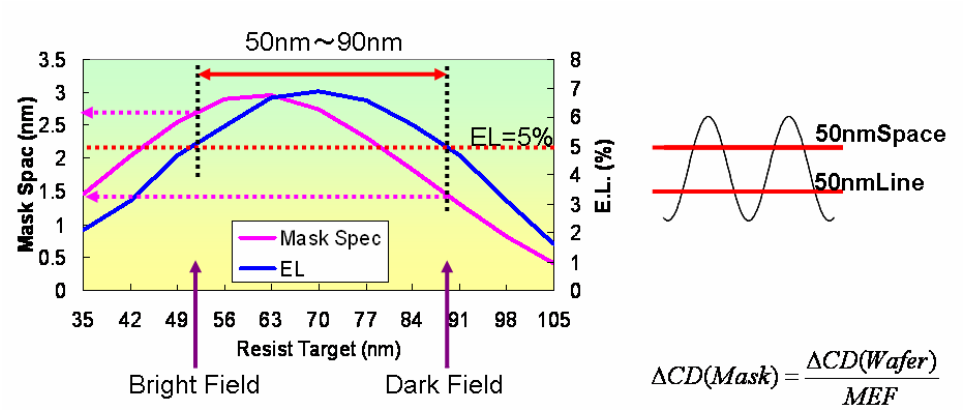
	O/L 3sigma	Spec. 3sigma	Source
M2(1st)-V2(1st),V2(2nd)	3s×√3/√2=3s×1.2	<10.0nm	Assumption
M2(2nd)-V2(2nd)	3s×√5/√2=3s×1.6	<10.0nm	Assumption
M2(2nd)-M2(1st)	3s	<2.5nm	CD budget

Figure 4. Alignment tree of double patterning for 22nm node.



	Litho CD	Biasing Amount	Final CD
Bright Field	Line 50nm	Trim 15nm	Line 35nm
Dark Field	Space 50nm	Shrink 15nm	Space 35nm

Figure 5. Amount of trimming or shrinking for 22nm node.



	Litho CD	ΔCD(Wafer) +/-6.5%	MEF	ΔCD(Mask) on Mask
Bright Field	Line 50nm	2.275nm	3.6	2.6nm
Dark Field	Space 50nm	2.275nm	7.0	1.4nm

Figure 6. Mask specification of CD uniformity for 22nm node.

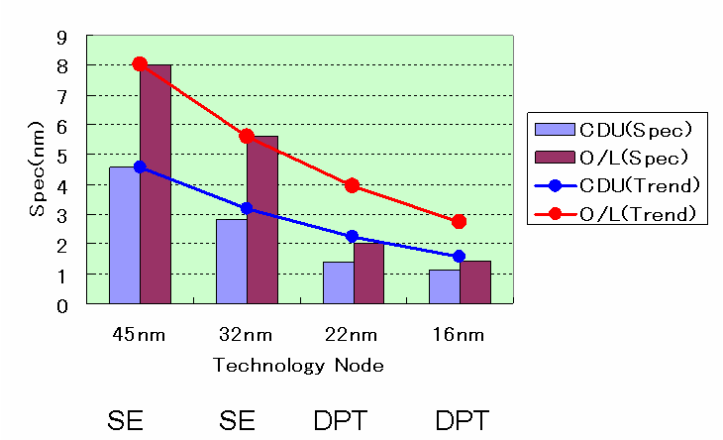


Figure 7. Requirement for mask CD uniformity and mask induced overlay error.

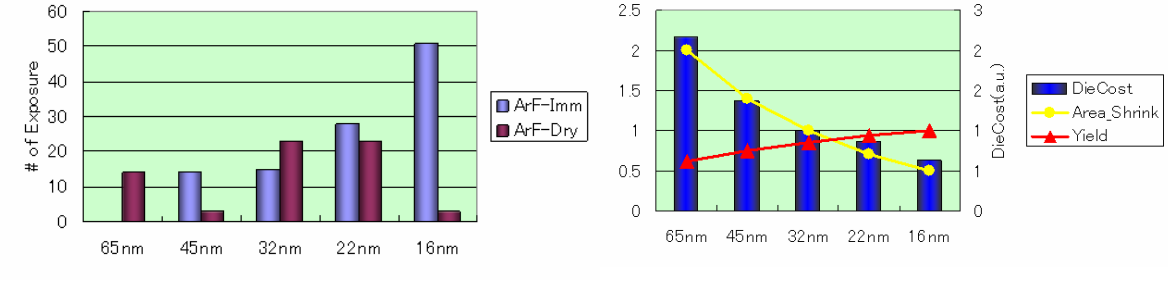


Figure 8. Number of ArF exposure and the cost estimation.