Design of Folded Cascode Operational Amplifier (Op-Amp) with Common-Mode Feedback (CMFB) for Pipeline ADC.

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Abstract

This work proposed a design of folded cascode operational amplifier (op-amp) with common-mode feedback (CMFB) circuit for Pipeline Analog-to-Digital Converter (ADC) with high gain and large unity bandwidth. The folded cascode topology with CMFB has been implemented in CMOS 0.13 µm Siltegra process technology with 1.8 V supply voltage. The simulation results show that the DC gain is 62.69dB, the phase margin (PM) is 68.36 degree, and the unity gain bandwidth (UGB) of 133.1 MHz is achieved. The power consumption of this op-amp is only 0.3 mW and 22.6 V/µs of slew rate with 72.4 ns settling time. The performance of schematic is evaluated using Cadance simulations.

Keywords
Op-Amp, Folded Cascode, CMFB and pipeline ADC.

1. Introduction

Pipeline analog-to-digital converters (ADCs) have become the most trendy ADC architecture for sampling rates as it has proven attractive for high-speed and low-power-analog-to-digital conversion with medium resolution requirements [1, 2]. Pipeline ADC consists of a cascade of stages, which have a low resolution ADC, DAC and amplifier, that consecutively convert the analog input into the digital sign, while processing the data in pipe-lined manner. This architecture is widely used in such areas likes wireless communication systems, images processing applications [1-4] and etc.

Amplifier or operational amplifier is a core element of pipeline ADC. Op-amp can be intended into several topologies which are multi-stage, telescopic, folded cascode and gain boosted op-amp [5]. In order to improve the gain of an amplifier, the cascode structure is applied. For this work, folded cascode topology is opted for main op-amp design since in the literature review [6-8], this topology allows the input common-mode level to be close to the power supply voltage compared to others op-amp topology. The folded cascode topology provides high output swings, wide input common-mode range and ideally suited to operate in low voltage supply circuits [8,9].

2. Circuit Implementation

2.1 Folded Cascode

Customarily, the folded cascode design had barely with a pair of PMOS type or else NMOS type at the input of op-amp by considering the limits of input common mode range (Abo, 1992). Figure 1 illustrates the folded cascode amplifier, which is the main op-amp designed for pipeline ADC with NMOS inputs. This input type gives the large output gain compare to PMOS type of input. The 1pF of capacitor load is used in this circuit design thus to stabilize the phase of op-amp circuit.
The operation of folded cascode comprises of one differential pair consisting of NMOS transistor M9 and M10. The MOS transistor which is M1 and M2 presents the DC bias voltage of CMFB circuit. Whereas M3, M4, M5, M6, M7, M8 composed of low-voltage cascode and it works by connecting to the DC bias voltage. The gain of the folded cascode architecture is given by:

\[ A_v = G_{m9} \left\{ [G_{m3}r_{o3} - (r_{o9}||r_{o1})] \| [G_{m5}r_{o5}r_{o7}] \right\} \] (1)

2.2 Common Mode Feedback (CMFB)

CMFB circuit is important for a proper operation of fully differential amplifier. From the previous research work [10-14], CMFB is required to fix the voltages at high impedance node in the circuit to the desired values besides increasing the CMRR performance of the differential amplifier through the accuracy of the CMFB circuit [13].

As depicted in Figure 2(b), the CMFB circuit is proposed from the conventional CMFB circuit [10] that shows in Figure 2(a). As of [10] the conventional CMFB is proposed a single detection CMFB with used the PMOS input type since its leaning for the limitation of input range. For this work, the conventional CMFB circuit has been modified to the double detection CMFB circuit in order to stabilize the output of common-mode voltage for op-amp. Refer to Figure 2(a) the pair of transistor M13 and M14 are modified to be a double detecting which assigns as M12 in Figure 2(b) and its used to feedback from the folded cascode op-amp. Meanwhile, M13 and M14 is an input of CMFB, which attaches to the output of a folded cascode op-amp and M15 is a task for a reference voltage.
3. Result and Discussion

The AC analysis is performed to determine the gain, unity gain bandwidth (UGB) and phase margin. The DC gain, phase margin and also unity gain bandwidth are measured using DC operating point and AC analysis as shown in Figure 3 and 4. Meanwhile, the slew rate and settling time are obtained by Transient analysis as in Figure 5.

The gain and phase margin curves of op-amp are demonstrated in Figure 3 and Figure 4 which exhibits a DC gain of 62.69dB and phase margin is 68.36° with the unity gain bandwidth (UGB) 133.1MHz.
A transient analysis was performed by obtaining the rate of change of output with time; slew rate and settling time. As illustrated in Figure 5 and Figure 6, the slew rate of op-amp is 22.6 V/µs and 72.4 ns of settling time.
The simulation result is summarized as in Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>Technology</td>
<td>130nm Silterra process</td>
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<tr>
<td>Supply voltage</td>
<td>1.8 V</td>
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<tr>
<td>DC Gain</td>
<td>62.69dB</td>
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<tr>
<td>Phase Margin</td>
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<tr>
<td>Gain Bandwidth</td>
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<tr>
<td>Slew Rate</td>
<td>22.6 V/μs</td>
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<td>Settling Time</td>
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<td>Load Capacitor</td>
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<tr>
<td>Power Dissipation</td>
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</tr>
</tbody>
</table>

4. Conclusion

The design of folded cascode operational amplifier with common mode feedback using 0.13μm Silterra process technology is presented in this paper. With load capacitor 1pF, the design demonstrates a DC gain 62.69dB with gain bandwidth 133.1MHz and phase margin of 68.36°. This work can be apt for Pipeline ADC.

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References


