A 65-nm CMOS 1.75–15 GHz Stepped Frequency Radar Receiver for Early Diagnosis of Breast Cancer

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Abstract—A 65-nm CMOS receiver tailored for breast cancer diagnostic imaging is demonstrated for the first time. The receiver shows 31-dB conversion gain, $\text{NF} < 8.6 \text{ dB}$, $P_1 \text{dB} > -28 \text{ dBm}$, IIP3 $> -12 \text{ dBm}$ and IIP2 $> 22 \text{ dBm}$ over a band from 1.75 to 15 GHz. A programmable injection-locked divider generates quadrature LO signals with a I/Q phase error $< 1.8^\circ$ over three octaves without requiring any calibration or tuning. The receiver shows a flicker noise corner as low as 40 Hz, achieving a dynamic range of 106 dB.

Index Terms—CMOS, radar imaging, UWB receiver.

I. INTRODUCTION

MICROWAVE radar imaging has recently been investigated for medical applications, in particular for the detection and early diagnosis of breast cancer [1]–[7]. Breast cancer is the most incident tumor among female population [8]; early time prevention is a key factor in delivering long term survival to patients [8]. As compared to the more commonly used X-ray mammography (i.e., X-ray imaging of the compressed breast), microwave radar imaging is an attractive alternative, as it avoids the use of ionizing radiations and breast compression, that cause health hazards and discomfort to patients. Radar microwave imaging leverages the contrast between the dielectric properties of healthy and cancerous tissues [9] to identify the presence and location of significant scatterers [1]–[7]. The concept is to illuminate the breast with an ultra wideband (UWB) pulse and collect the backscatter. From the shape and the time of arrival of the reflected pulse, information on the position and size of the scatterer are retrieved. By performing a set of measurements over different antenna positions, and by processing the obtained data in a digital beam focusing fashion, a high-resolution image of the dielectric properties of the breast tissues can be derived [1]–[7].

Recent works, e.g., [4], [6], [7], show the feasibility of this technique employing commercial network analyzers (VNA) to synthetically generate UWB pulses by transmitting a set of narrowband stepped frequency continuous waveforms (SFCW) over a wide range of frequencies, while receiving the backscatters from the breast. At each measurement step, a single-frequency tone is transmitted and received. Time-domain waveforms are then retrieved by means of IFFT. Consequently, the required radar transceiver has peculiar features: the frequency generation circuits, the transmitter output stage and the input stage of the receiver must be capable of operating on a very broad range of frequencies, $B$. The higher the bandwidth, the better the achieved resolution, as it will be clearer in Section II. On the other hand, since the irradiated signal is, at each measurement step, a purely sinusoidal waveform, the baseband section of the receiver can have a bandwidth as narrow as desired. Hence, the noise bandwidth of the system can be extremely narrow, which allows for a very large dynamic range.

A necessary condition to turn microwave radar imaging into a mass screening diagnostic tool for early breast cancer detection is to replace the bulky and expensive VNA with a low-cost dedicated CMOS integrated circuit [1]. The development of a custom integrated circuit is key in the perspective of an increase of the system performance, and of a reduction of its size and cost. In this paper, we present a 65-nm CMOS receiver operating over three octaves from 1.75 to 15 GHz, able to collect the signals reflected by the breast with a high dynamic range of 106 dB [10], paving the way to the replacement of the VNA in the setup. The transistor-level design is described in detail, along with a complete experimental characterization of the fabricated receiver prototypes. System-level considerations are also reported to get more insight in the various design choices that have been taken.

The paper is organized as follows. In Section II, the radar system-level requirements are mapped into circuit-level specifications for the receiver. In Section III, the transistor-level design of the receiver is discussed. Experimental results carried out on fabricated prototypes are reported in Section IV, while conclusions are drawn in Section V.

II. RECEIVER REQUIREMENTS

A thorough system analysis has been carried out in [11]. To get insight into the system requirements, we start from the pa-
rameters that set the resolution of the imaging system, as this is, ultimately, the feature of interest. The achievable resolution in the slant-range, \( \Delta r_s \), i.e., in the direction of wave propagation, is directly related to the overall bandwidth of the system, \( B \), as

\[ \Delta r_s \approx \frac{v}{2B} \]  

where \( v \) is the wave velocity in the medium. The resolution in the cross-range, \( \Delta r_c \), i.e., on the plane orthogonal to the direction of wave propagation, is \[13\], \[14\]

\[ \Delta r_c \approx \frac{R}{l} \frac{v}{B} \]  

where \( l \) is the equivalent synthetic aperture length of the antenna array, and \( R \) is the target range. From (1) and (2), it is clear that the larger the overall bandwidth of the system, \( B \), the better the resolution of the obtained image. As in the breast the wave velocity is approximately \( v \approx 10^8 \text{ m/s} \) \[9\], the depth of a typical normal, non-lactating human breast is in the order of 4 cm \[15\], and assuming a feasible \( l \geq 10 \text{ cm} \), an overall system bandwidth of 13 GHz translates in a resolution of 4 mm, which is adequate to detect even the smaller tumors \[16\].

Achieving the desired spatial resolution is not enough to guarantee a successful detection of the tumors. To understand why, let us refer to Fig. 1, where the scenario of a realistic numerical breast phantom is shown. The antenna is supposed to be placed at 1 cm from the breast skin, and the 4-mm-diameter tumor target is placed at different distances from the antenna. Finite-difference time-domain (FDTD) electromagnetic simulations have been carried out \[11\]. The simulated round-trip attenuation of a signal in the antenna-skin-antenna path \( (H_S(f)) \) is shown in Fig. 2 along with the attenuation experienced by the signal in the antenna-tumor-antenna path \( (H_T(f)) \). Clearly, the breast skin acts as a shield, reflecting most of the transmitted waves with little attenuation and small dispersion \( (|H_S| \approx 20 \text{ dB almost independently of frequency}) \). On the contrary, the attenuation of the tumor backscatter strongly increases with frequency. From the analysis of the results in Fig. 2, we conclude that the radar receiver must feature a dynamic range in excess of 100 dB. As a consequence, an analog-to-digital converter (ADC) with a resolution in excess of 16 bit is needed in the system. A direct-conversion architecture is chosen for the radar receiver, since such a high-resolution ADC will not display a large bandwidth. Note that the SFCW radar approach used in the system is compatible with this architectural choice, as it allows for very narrow system noise bandwidths. Assuming a transmitter output power of \(-14 \text{ dBm}\), the maximum received input signal is dictated by the skin reflection, and it is thus around \(-34 \text{ dBm}\). Consequently, the receiver compression point \( (P_{1\text{dB}}) \) is specified to be higher than \(-30 \text{ dBm}\). To guarantee a dynamic range in excess of 100 dB with a noise bandwidth of 1 kHz, the receiver must feature a noise figure lower than 10 dB. To further put the dynamic range issue in perspective, notice in Fig. 2 that the tumor backscatter is in excess of 100 dB smaller than the skin reflection only at the higher frequencies. This means that, once the measured frequency-domain data is converted in the time-domain by means of IFFT, the signal-to-noise ratio will improve because of the higher energy of the tumor scatter at the lower frequencies. In addition, the IFFT provides an intrinsic processing gain roughly equal to the number of data points.

The narrow baseband bandwidth dictated by the SFCW approach and by the high dynamic range requirement make the main drawbacks of a direct conversion architecture, namely second-order distortion and 1/f noise, potential show-stoppers. Breast cancer imaging is supposed to be performed in a screened medical environment \[17\], it is reasonable to assume that no signals other than those generated by the proposed system occupy the spectrum, relaxing the required intermodulation performance of the receiver. Still, a large in-band blocker is there, due to the reflection of the breast skin. As discussed in detail in \[11\], the in-band \(^2\text{IIP2} \) is specified to be greater than \(20 \text{ dBm}\). At the same time, the 1/f noise corner frequency must be kept as low as possible, as described in Section III.

In a high-resolution imaging system, random phase offsets between I and Q channel are extremely critical and lead to errors in the evaluation of the tumor location and detection. Hence, the allowable quadrature phase mismatch (less than 1.5°, as singled out in \[11\]) turns out to be the most stringent specification for the receiver: achieving such a high quadrature precision from 1.75 to 15 GHz is a strong challenge.

2Both downconverted tones and intermodulation product within the baseband bandwidth.
A block diagram of the proposed receiver is shown in Fig. 3. The signal path is made of a wideband LNA, linearized transconductors, quadrature current-mode passive mixers, and baseband transimpedance amplifiers (TIAs). A programmable divider/quadrature generator (DQG) provides quadrature signals to the mixers over the entire 1.75 to 15 GHz frequency range out of a LO signal spanning the higher octave (i.e., 7 to 15 GHz).

Compared to wideband receivers for wireless communications, e.g., software-defined radios [18], [19] or WiMedia UWB systems [20], [21], the presented circuit addresses peculiar issues and design challenges. First, it features a bandwidth that is more than two times wider. Second, it requires an extremely high instantaneous dynamic range, because of the strong undesired skin backscatter, which is an in-band signal coexisting with the very weak tumor echo. Consequently, the dynamic range cannot be dealt with by varying the receiver gain, as usually done, for example, in cellular systems. Third, the quadrature accuracy is extremely important, as the imaging process is based on phase measurements. It is vital that the performance is consistent and homogeneous in the entire band without offsets or jumps in the quadrature error for different portions of the covered spectrum. Finally, the narrow baseband bandwidth allowed by the SFCW approach requires a very low flicker noise corner, while CMOS transistors notoriously feature large flicker noise.

A. Low Noise Amplifier

The LNA must provide wideband input matching and gain, while featuring a low noise figure. To achieve the required performance from 1.75 to 15 GHz a three-stage design is used. The first stage is responsible for the input matching and the noise performance. A multi-section input matching network could have been used as in [22]. However, the combination of a wide fractional bandwidth and a relatively low frequency at the lower edge of the band calls for large inductors, that would be impractical. The employed topology is instead a common-gate/common-source noise canceling amplifier [23], [24], whose schematic is shown in Fig. 4. The noise canceling stage allows to decouple the matching requirement from the noise figure performance. The noise generated by the matching device $M_1$ is canceled without impairing the useful signal by setting $Z_1/|Z_2| = g_m2R_S$, where $R_S = 50 \, \Omega$ is the source resistance. The common-gate branch is biased with 2 mA, while the common-source branch is biased with 7 mA. The widths of transistors $M_1$ and $M_2$, both featuring minimum channel length, are 40 $\mu$m and 80 $\mu$m, respectively. Biasing transistor $M_3$ has a higher overdrive voltage ($W_3 = 10 \, \mu$m, $L_3 = 0.12 \, \mu$m) as compared to $M_2$ to decrease its noise contribution. The combination of the series inductor $L_1 = 520 \, \mu$H and the common-gate stage $M_1$ ($g_{m1} \approx 20 \, mS$) results in good matching over a wide 1.5 to 20 GHz frequency range.

The schematic of the second and third stage of the LNA is shown in Fig. 5. The second stage of the LNA is biased with 6 mA. It is a fully differential pair to improve the signal balance and add gain. The third stage is biased with 12 mA. It is a pseudo-differential stage for better linearity.

All three stages use shunt-peaked loads to expand the bandwidth. The values of the load inductances and resistances are shown in Table I. Since the loads are intrinsically low-$Q$, the inductors are stacked square coils, resulting in a very compact layout, that saves area and minimizes the coupling issues between the LNA stages. The resistance $R_2$ is implemented as a parallel combination of three resistances of value $R_1$ to guarantee good matching for the noise canceling condition, at least at the lower frequencies. A plot of the post-layout simulated gain of the LNA is reported in Fig. 6. The gains of the first and second stage are 15 dB and 5 dB, respectively. The third stage has a relatively low 2 dB gain at lower frequencies, that peaks to 8 dB at about 17 GHz. Such an arrangement is used to equalize the bandwidth roll-off due to the preceding stages, and to expand the overall bandwidth of the LNA. The designed amplifier features a bandwidth that is more than two times wider compared to state-of-the-art noise canceling LNAs, see, e.g., [24].
Fig. 6. Simulated gain of the LNA.

**TABLE I**

<table>
<thead>
<tr>
<th>Component Values of the LNA Shunt-Peaked Loads</th>
<th>$L_1$</th>
<th>$L_2$</th>
<th>$L_3 = L_4$</th>
<th>$L_5 = L_6$</th>
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<td>Inductance [pH]</td>
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<td>700</td>
<td>900</td>
<td>550</td>
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<tr>
<td>Area [$\mu$m$^2$]</td>
<td>56x56</td>
<td>50x50</td>
<td>56x56</td>
<td>42x42</td>
</tr>
<tr>
<td>Resistance [$\Omega$]</td>
<td>225</td>
<td>75</td>
<td>170</td>
<td>34</td>
</tr>
</tbody>
</table>

Fig. 7. Schematic of the I-path downconverter (Q-path is identical).

**B. Low 1/f Noise Corner Quadrature Downconverter**

Resistively-degenerated transconductance ($G_m$) stages are used in the I/Q paths to convert the LNA output voltage into current, as shown in Fig. 7. Each $G_m$ stage is biased with 8 mA, and makes use of a $R_{\text{deg}} = 46$ $\Omega$ degeneration resistor. Self-biased active loads are employed: this configuration avoids the need of an auxiliary common-mode feedback control loop.

Current-mode passive mixers are capacitively coupled to the transconductor outputs (cf. Fig. 7). This choice results in both good linearity and good noise performance, preventing the flicker noise of the commutating devices to corrupt the downconverted signal [25]. A large and constant swing of the LO signal across the band is essential to achieve good mixer performance. The proposed DQG plays a key role in this, as discussed in the following Section III-C.

The use of passive mixers is not sufficient to address the high flicker noise of MOS transistors. Typically, current-mode mixers are loaded by baseband transimpedance amplifiers (TIAs), based either on common-gate stages or on op-amps with resistive feedback. The flicker noise of the devices of the TIAs is not suppressed, ultimately setting the flicker noise corner of the receiver. To overcome this limitation, the chopper stabilization technique is used to reduce the flicker corner below 100 Hz. Chopper stabilization is a widespread technique, usually applied to voltage amplifiers [26]–[29]. However, to the best of the authors’ knowledge, its use with TIAs in a downconversion mixer is unprecedented. The combination of passive current-mode switches and chopper stabilized TIAs results in a highly linear, low noise downconversion mixer with a very low flicker noise corner.

The schematic of the proposed TIA is shown in Fig. 8. The amplifier is based on a common-gate stage. Compared to an op-amp with resistive feedback approach, this choice allows to decouple the input and output common-mode voltages. As a consequence, the input common-mode voltage can be kept low, which is beneficial for the mixer switches (nMOS transistors), without impairing the output swing. Local feedback (transistors $M_3$ and $M_5$) is used around the common-gate input stage (transistors $M_2$ and $M_3$) to decrease the differential TIA input resistance, $R_{\text{in,TIA}}$, as

$$R_{\text{in,TIA}} \approx \frac{2}{g_{m3}g_{m5}R_{\text{01}}}. \quad (3)$$

The input branches of the TIA are biased with 250 $\mu$A each, such that a differential input resistance of 35 $\Omega$ is achieved at a small power consumption. The input currents are mirrored to the output branches. Eventually, resistors $R$ perform the current-to-voltage conversion.

**C. Programmable Divider/Quadrature Generator**

As discussed, the local oscillator (LO) quadrature accuracy is the most stringent specification for a receiver tailored for stepped-frequency microwave imaging. The quadrature error must be small, and constant over the entire wide receiver bandwidth. Sudden changes in the I/Q phases cannot be tolerated, even if they occur for few frequencies in the wide covered span.

Accurate generation of quadrature signals over multiple octaves can be achieved by using static frequency dividers by two. However, this technique cannot be used in the proposed radar receiver because of the high frequencies involved. Apart from the power consumption of the divider yielding the frequencies for the higher octave, the generation of the LO signals at twice the frequency, i.e., from 15 to 30 GHz, with extremely low phase noise (also a sensitive specification for the system [11]) and large tuning range, would require many power hungry VCOs to meet the requirements. The use of a polyphase filter to generate the I/Q phases in the higher octave is also a possibility. To meet the required quadrature accuracy over one octave while being robust to process spreads, the filter should feature more than three sections, thus introducing more than 18-dB losses. Since...
a large LO swing is required by the mixer switches, buffers would be needed to drive the polyphase filter and to regenerate the signal after it. Simulations suggest that such buffers would consume as much current as the entire proposed DQG. In addition, the LO signal would be tapped from different points of the circuit to cover the various octaves. As a consequence, the feed to the mixer could be uneven across the band in amplitude and, most importantly, in phase.

To address all the aforementioned issues, we devised an innovative solution, made of a cascade of two programmable injection-locked dividers that can divide by 1 or 2. A PLL (not implemented in this design) is supposed to generate signals over the higher octave, namely from 7.5 to 15 GHz. The DQG is then capable of producing quadrature signals over three octaves starting from the PLL output.

The block diagram of the DQG is shown in Fig. 9. Two regenerative buffers (RBs), based on injection locked ring oscillators, drive the first programmable divider. An interstage buffer made of two-stage tapered CMOS inverters interfaces the two programmable dividers. The interstage buffer is ac-coupled to the output of the first programmable divider, and the input inverter is biased at its logical threshold by means of replica biasing. A regenerative buffer eventually drives the mixers. The injection locked regenerative buffer intrinsically operates at large output swings, hence providing a large drive to the mixers with minimum amplitude variations across the band. The interface between the LO distribution and the mixers is the same regardless the DQG is dividing by 1, 2, or 4. This avoids discontinuities in the operation of the DQG due to changes in the loading of the LO distribution chain. The architecture of the DQG, made of a cascade of several injection-locked stages, has the advantage of progressively improving the quadrature accuracy [30], such that every stage is contributing to reduce the quadrature error in any used configuration. Moreover, the use of injection locked circuits based on inductorless ring oscillators results in very wide locking ranges [31]. As a consequence, the DQG does not need any calibration nor tuning.

The schematic of the RB is shown in Fig. 10. The core of the circuit is a two-stage differential ring oscillator in which the delay cells are differential static CMOS latches with input buffers as delay elements. Although the RB is basically a digital circuit in its structure, a full custom design is needed to guarantee the correct operation up to 15 GHz. Analog techniques are also required. An example is given by the injection buffers of the RB, shown in Fig. 10. The buffers are essentially CMOS inverters. However, to make them operate correctly in the required frequency range, even in presence of input signals with less than rail-to-rail swing, ac-coupling through capacitors $C_{c1} = 310 \, \text{fF}$ and $C_{c2} = 120 \, \text{fF}$ is employed, which makes the inverters work as analog amplifiers. This is similar to the approach reported in [20]. Note that two $RC$ decoupling sections are used in cascade, as opposed to connecting one terminal of both $C_{c1}$ and $C_{c2}$ directly to the input. The chosen arrangement in fact reduces slightly, but effectively, the capacitive loading on the driving stage. Moreover, it allows for a more compact layout since the smaller $C_{c2}$ can be conveniently placed in the neighborhood of the pull-down nMOS, leaving more space for the larger $C_{c1}$. The bias voltages of the nMOS and pMOS transistors are obtained by means of current mirrors, shared among the buffers.

The schematic of the programmable divider is shown in Fig. 11. Similarly to the RB, the programmable divider is built around a two-stage differential ring oscillator. The topology of the delay cell is also similar (cf. Fig. 12), although the transistor size is differently optimized in each block. The possibility of having a programmable divider is based on the multiphase injection locking concept [32]. Depending on the phase progression of the signals fed to the divider, harmonic or super-harmonic injection locking occurs, enabling either division by 1 (same input and output frequency) or frequency division by 2. Different division ratios are hence obtained by reconfiguring the injection network, as shown in Fig. 13. In the divide-by-one mode, a complete quadrature sequence $(0^\circ, 90^\circ, 180^\circ, 270^\circ)$.
180°, and 270°) must be injected at the four nodes of the ring oscillator. Consequently, nodes “A” (cf. Fig. 13) are grounded and quadrature phases are injected into the ring oscillator through pseudo-differential pairs. As shown in Fig. 12, the pull-up transistors of the delay inverters of the ring oscillator are effectively made larger, as compared to the divide-by-two configuration, to counteract the undesired pull-down effect of the injection devices (M_1 through M_4) in Fig. 13. The latter would in fact tend to decrease the output common mode voltage of the ring oscillator, and in turn the oscillation amplitude. In the divide-by-two mode, nodes “A” in Fig. 13 are floating. A signal with 0° phase is fed to both injection devices M_{11} and M_{12}, that thus operate as a single transistor connected across the output nodes of one of the delay cells of the ring oscillator. Similarly, a signal with 180° phase is fed to injection devices M_{13} and M_{14}. Such a direct injection arrangement enables superharmonic injection-locking operation [31], and consequently frequency division by 2. The injection devices M_{11} through M_{14} are ac-coupled to the phase distribution multiplexers, which are built out of tri-state CMOS gates. The dc bias voltage fed to the injection transistors is tailored for divide-by-1 and divide-by-2 operation. It is important to emphasize, however, that these bias voltages are set by design, and that no tuning is required for the DQG to operate over three frequency octaves.

A test buffer, made of three stages of resistively loaded differential pairs, interfaces the differential DQG input to an external single-ended signal, as shown in Fig. 3. This buffer will be removed once a PLL, directly connected to the DQG, is integrated along with the receiver.

A careful layout is essential at guaranteeing accurate quadrature phase generation. Apart from aiming at layout symmetry, other strategies have been put in place. All paths have been made balanced with respect to the capacitive parasitics. Every employed capacitor has been screened with grounded lines to reduce the undesired cross-coupling between paths carrying signals with different phases, reduce the Miller effect, and balance the parasitic capacitances. Every long interconnection has been similarly screened. Finally, every circuit cell (e.g., the delay cell in the divider and RB) has been also screened, such that every corresponding MOS device in different cell instances is loaded with similar parasitic capacitances.

The simulated amplitude of the DQG output signal is shown in Fig. 14. The peak-to-peak amplitude is roughly 1 V over the entire frequency range of operation. The plot refers to any signal out of the four phases generated by the DQG. The simulation includes the post-layout parasitics and has been performed in the nominal technology corner. It has been performed at frequencies 20% higher than the nominal ones to verify that the design exhibits a sufficient speed margin to be robust once implemented in silicon.

IV. MEASUREMENT RESULTS

The proposed radar receiver was implemented in a 65-nm CMOS process. Chip prototypes were fabricated and assembled in chip-on-board fashion for testing. All the pads were wire-bonded with the exception of the input pad of the LNA, which has been probed. A microphotograph of the die is shown in Fig. 15, where the various functional blocks are highlighted. The active area is as small as 870 × 550 μm².

The supply voltage is 1.2 V. The current drawn from the supply is 34, 16, and 2 mA for the LNA (including bias circuitry), G_m stages, and TIAs, respectively. The DQG draws 51 mA. The overall power consumption of the receiver is thus 124 mW.

The measured conversion gain (CG), LNA input return loss, and receiver NF are reported in Fig. 16 across the entire frequency range. The CG is as high as 31 dB, the input matching
Fig. 16. Conversion gain (CG), noise figure (NF) and input reflection coefficient ($S_{11}$).

Fig. 17. Measured conversion gain (CG) as a function of the intermediate frequency for different LO frequencies.

The measured conversion gain as a function of the intermediate frequency is reported in Fig. 17 for different values of the LO frequency. The latter are chosen to span the three modes of operation of the DQG. In any case, the baseband bandwidth, limited by the TIA, is 800 kHz.

Several linearity tests have been carried out. The measured $S_{11}$ is lower than $-9$ dB, and the noise figure ranges from 6.4 to 8.6 dB with an average value of 7.6 dB.

The measured conversion gain as a function of the intermediate frequency is reported in Fig. 17 for different values of the LO frequency. The latter are chosen to span the three modes of operation of the DQG. In any case, the baseband bandwidth, limited by the TIA, is 800 kHz.

Several linearity tests have been carried out. The measured $P_{1\text{ dB}}$ is shown in Fig. 18. From 2 to 15 GHz it is greater than $-28$ dBm, well above the $-34$ dBm maximum received signal that we expect from the analysis in Section II.

Two-tone measurements are performed to assess the intermodulation performance of the receiver. Since, as discussed in Section II, medical imaging is performed in a screened environment, the required third-order intermodulation performance of the receiver is quite relaxed. However, although the desired signal is the only one being received, and although it is a purely sinusoidal tone, still there might be some spurious tones associated with it. Assuming the transmitted signal is generated by an integer-$\nu$ PLL with a reference frequency of some 10 MHz, some reference spurs might be there as undesired interferences.

The spurious themselves would be out of the TIA band, and thus be filtered out, but their intermodulation product would corrupt the desired signal. To assess this scenario a two-tone test has been carried out with tones at 25- and 50.05-MHz offset from the LO, for various LO frequencies. The IIP3 measured in this condition is reported in Fig. 18: it is greater than $-12$ dBm across the LO frequency range. As a consequence, the maximum relative level of the PLL spurs ($S_{i}$) that can be tolerated is

$$S_{i} \leq -3P_{\text{RX}} - 2 \frac{\text{IIP}3 - P_{a}}{3} = -19 \text{ dBc} \quad (4)$$

where $P_{\text{RX}} = -34$ dBm is the maximum signal we expect to receive, and $P_{a} = -134$ dBm is the maximum distortion we can tolerate to have a 100 dB dynamic range. Clearly, the third-order intermodulation distortion performance of the proposed radar receiver results in very loose spurious specifications set on the radar transmitter.

As opposed to third-order intermodulation distortion, second-order intermodulation distortion is critical for the proposed direct-conversion receiver, as the skin backscatter acts as a strong in-band interferer (cf. Section II). IIP2 has been measured setting the two tones such that both the tone frequencies and the intermodulation products fall within the TIA band. The result is shown in Fig. 18 for seven chip samples: the median value is 30 dBm while the worst case is 22 dBm. In any case the performance is within the specification singled out in Section II.

The $1/f$ noise is a potential show-stopper in this system, due to the extremely narrow baseband bandwidth and the direct-conversion architecture. The $1/f$ noise corner frequency has been measured with the aid of an external ADS1282 ADC. The ADC is an oversampling converter, and it embeds both an anti-alias filter and a decimation filter. Consequently, it sets the noise bandwidth of the receiver at 1 kHz. The $1/f$ noise corner frequency has been measured to be 1 MHz to avoid any aliasing (the ADC sampling frequency is 4 MHz), and yet prevent $1/f$ noise folding. A plot of the measured input-referred noise power density is shown in Fig. 19. The $1/f$ noise corner is as low as 40 Hz, an unprecedented result for wireless receivers. The input-referred
TABLE II
SUMMARY OF THE MEASURED PERFORMANCE AND COMPARISON WITH THE STATE-OF-THE-ART.

<table>
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<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$P_{0d}$ [mW]</td>
<td>124</td>
<td>236</td>
<td>680</td>
<td>&lt;115</td>
<td>230</td>
<td>425‡</td>
</tr>
</tbody>
</table>

†Evaluated from reported sensitivity, noise bandwidth, and SNR. ‡One channel of timed array. *Complete transceiver.

Fig. 19. Measured input referred noise PSD with the chopper stabilization of the TIA OFF and ON (measurement taken for $f_{c2}$ = 5 GHz, i.e., DQG in div-2 configuration).

noise, integrated over the 1-kHz ADC band, and combined with the measured $P_{1dB}$, gives a dynamic range in excess of 106 dB, showing that the performance of the proposed receiver is adequate to process simultaneously the strong skin backscatter and the weak echo from the tumor.

In a high-resolution imaging system, the quadrature phase and gain mismatches are very critical impairments. The measured I/Q phase and gain mismatches of seven samples are shown in Fig. 20. The quadrature error is less than 1.5° across the band while the gain imbalance is lower than 0.8 dB. In Fig. 20, note that a clear systematic gain mismatch is observed. Such a behavior was traced back to a layout error, resulting in a mismatch in the parasitic resistances of the input traces of the TIAs in the in-phase and quadrature paths. Once the systematic gain error is removed from the data in Fig. 20, the residual gain mismatch is limited to few tenths of dB. The good quadrature accuracy achieved over such a wide frequency range confirms that the proposed DQG is capable of excellent performance.

The measured performance of the proposed receiver is summarized in Table II, and compared to that of state-of-the-art wideband wireless receivers. The receiver in [33] is part of a timed-array for radar imaging, e.g. it implements the dual approach (time-domain as opposed to frequency-domain) with respect to the proposed receiver. The works in [18] and [19] report receivers for software-defined radios, while in [20] and [21] receivers for UWB WiMedia radios are presented. Overall, it is not easy to make a fair comparison because of the different applications these broadband receivers are tailored for. However, we note that the proposed receiver features quite a low power consumption while showing a comparable overall performance with respect to the other works. Moreover, it features an unprecedented low $1/f$ noise frequency corner.

V. CONCLUSION

A 65-nm CMOS receiver for breast cancer imaging is presented. The receiver operates from 1.75 to 15 GHz. The large bandwidth together with a dynamic range in excess of 106 dB and I/Q phase mismatches less than 1.5° results in a resolution of 4 mm, adequate to detect even the smallest tumors. To the best of authors’ knowledge, this is the first low-cost dedicated CMOS integrated circuit for this application. Most importantly,
it is the first research step towards the design and implementation of custom hardware for clinical trials that may enable future mass screening programs.

REFERENCES


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