A 90 nm CMOS Low-Power 60 GHz Transceiver With Integrated Baseband Circuitry

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***Abstract*—This paper presents a low power 60 GHz transceiver that includes RF, LO, PLL and BB signal paths integrated into a single chip. The transceiver has been fabricated in a standard 90 nm CMOS process and includes specially designed ESD protection on all mm-wave pads. With a 1.2 V supply the chip consumes 170 mW while transmitting 10 dBm and 138 mW while receiving. Data transmission up to 5 Gb/s on each of I and Q channels has been measured, as has data reception over a 1m wireless link at 4 Gb/s QPSK with less than 10^{-11} BER.**

***Index Terms*—Millimeter-wave integrated circuits, direct-conversion transceiver, CMOS, low-noise amplifier (LNA), mixer, power amplifier, voltage-controlled oscillator (VCO), phase-locked loop (PLL), 60 GHz, decision feedback equalizer.**

I. Introduction

With mobile devices becoming more powerful and including more storage than ever before, new applications are emerging that require fast wireless data transfers while consuming very low power. Communication in the 60 GHz band offers an attractive potential solution to meet the needs of these applications, and researchers have made significant progress in the design of CMOS mm-wave circuitry. For example, Floyd *et al*. described an integrated mm-wave front-end implemented in a SiGe process in [1], while other demonstrations have used CMOS technology [2]–[6].

Despite this progress, many challenges to achieving the energy efficiency required of multi-Gb/s communication between mobile devices remain. For example, in many past mm-wave publications, key components such as the frequency synthesizer and/or the baseband have been omitted from the integrated solution, making it difficult to characterize the power and performance tradeoffs inherent in a complete system. Furthermore, complete 60 GHz transmitters with both high output power ($\sim$ 10 dBm) and efficiency ($>$ 10% PAE) have yet to be demonstrated in CMOS, and generating and distributing a local oscillator (LO) with sufficient voltage swing typically requires substantial power dissipation. Similarly, although an integrated baseband was described in [7], the power dissipation of a baseband suitable for wideband mm-wave communications remains unquantified.

In order to address these challenges and highlight some of the critical remaining issues, this paper presents the design of one of the first integrated, energy-efficient 60 GHz transceivers including baseband circuitry. This 90 nm direct conversion design (Fig. 1) includes the RF and baseband (BB) signal paths as well as an integrated phase-locked loop (PLL) and LO distribution network. Building on work such as [7], the transceiver also includes baseband circuitry utilizing mixed-signal techniques similar to those used in high-speed electrical links in order to maximize energy efficiency.

By utilizing the available bandwidth at 60 GHz as a single channel, the transceiver was designed to allow 10 Gb/s communication using QPSK modulation. Except where noted, the transceiver operates from a 1.2 V supply, consuming 170 mW in transmit mode and 138 mW in receive mode. Section II describes the techniques used in the transmitter to achieve $>$ 10 dBm output power while maintaining this relatively low power consumption. Section III discusses the design of the mm-wave receiver and introduces a transmission-line based ESD protection circuit used in the low-noise amplifier (LNA) to enable packaging. Section IV then describes the mixed-signal techniques used in the baseband to reduce power consumption at multi-Gb/s data rates. The challenges of low-power LO generation and distribution are then described in Section V. Finally, measured results for the entire transceiver are presented in Section VI, followed by concluding remarks in Section VII.

II. Transmitter

Achieving both high output power and efficiency in transmitters remains a significant challenge at mm-wave frequencies. This is further complicated by the need for power combining of I and Q signals in the quadrature transmit chain, which can be a significant source of loss. Both of these challenges are addressed in this transmitter design in order to enable a low power mm-wave transceiver for mobile applications. Furthermore, a

Manuscript received April 23, 2009; revised July 31, 2009. Current version published December 11, 2009. This paper was approved by Guest Editor Zhihua Wang. This work was supported by the National Science Foundation Infrastructure Grant No. 0403427, DARPA, C2S2, Cascade Microtech, VTT, and Berkeley Design Automation. Chip fabrication was donated by STMicroelectronics.

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Digital Object Identifier 10.1109/JSSC.2009.2032584

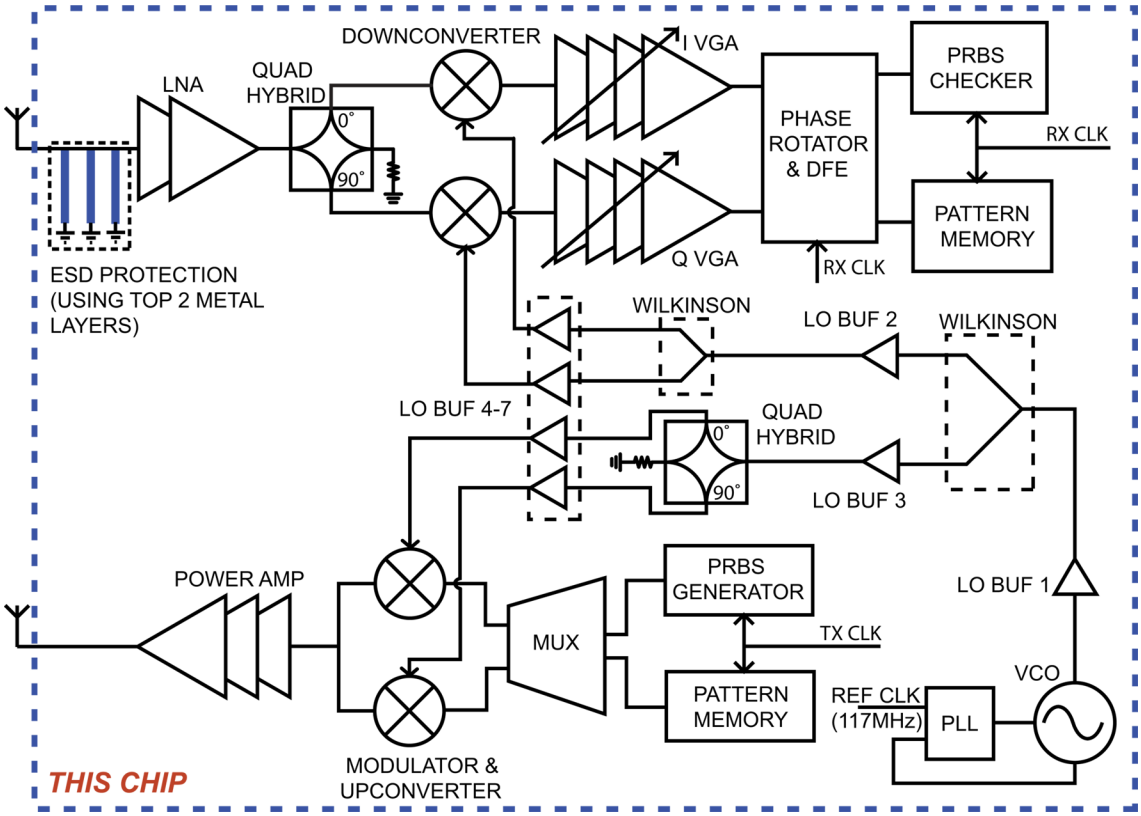

Fig. 1. Transceiver block diagram.

key feature of the RF portion of the transmit section (mixer and PA) is that it employs a transformer-based architecture. Compared to conventional transmission-line based matching network design, this approach reduces silicon area, with comparable insertion loss. The transmitter design consists of a digital baseband pattern generator, integrated digital-to-analog (DAC)/mixer structure, power amplifier (PA), and on-chip voltage-controlled oscillator (VCO) and PLL. Since we are not targeting a particular standard and using the entire 60 GHz band as a single channel, no reconstruction filter was used in this design.

The digital data from the on-chip PRBS generator is fed to the modulator, which consists of a fully differential combined DAC-mixer structure (Fig. 2). The modulator uses a double-balanced Gilbert quad whose tail current sources are digitally switched by the input data. This structure reuses the DAC current for the mixer and improves linearity by omitting the transconductance (g_m) stage of a conventional mixer. The LO signal derived from the VCO is converted to differential mode using a low-loss (1 dB) transformer and fed into the LO port of the Gilbert cell. The mixer nominally requires -4 dBm of LO drive at the transistor gates. This power is primarily determined by the input impedance of the LO port and the voltage swing required for good conversion gain. This has some important implications in the design of the LO distribution, as will be seen in Section V.

In order to achieve high data rates, the transceiver employs QPSK modulation, and hence the outputs of both an in-phase (I) and a quadrature (Q) up-conversion mixer must be combined into a single RF output. A convenient way to achieve this

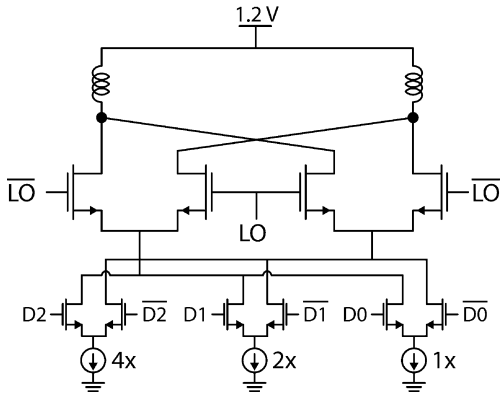

Fig. 2. Three-bit digital-to-RF modulator.

combination is through current-mode summation, achieved by directly connecting the outputs of the two mixers as illustrated in Fig. 3. However, current mode summation is challenging at 60 GHz due to the low output impedance of the transistors (even when they are in saturation). To achieve low-loss current summation, it would seem that a matching network is required to bring the input impedance of the PA down significantly below the output impedance of the mixer ($\sim$100 Ω in this design). However, if the transformation ratio is too high, such a matching network would have significant insertion loss. The design of this matching network therefore inherently involves a tradeoff between achieving low-loss current summation while maintaining low insertion loss, and thus there is an optimum impedance that

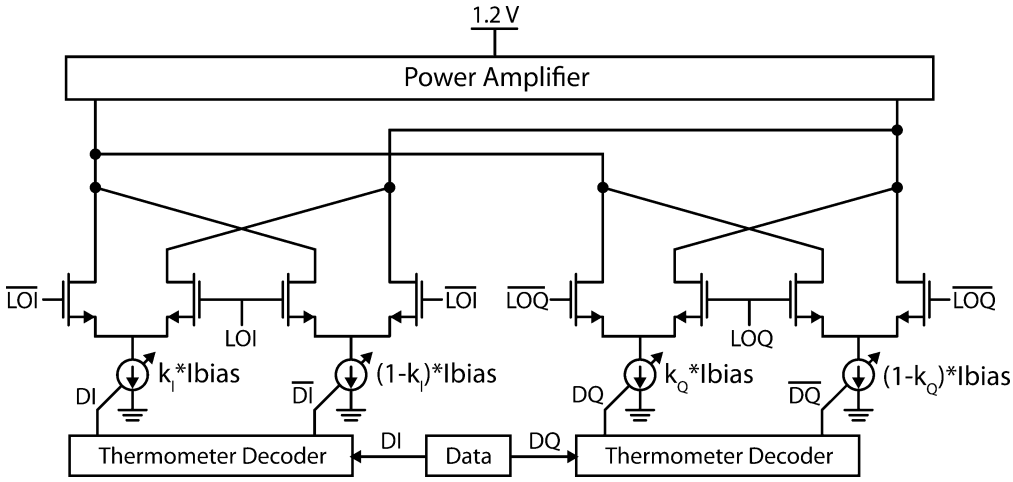

Fig. 3. Quadrature modulator using thermometer coding to improve matching. The modulator allows QPSK, 16QAM, and 64QAM, but for this transceiver only QPSK modulation was used. The bias current is programmable to allow for power back-off.

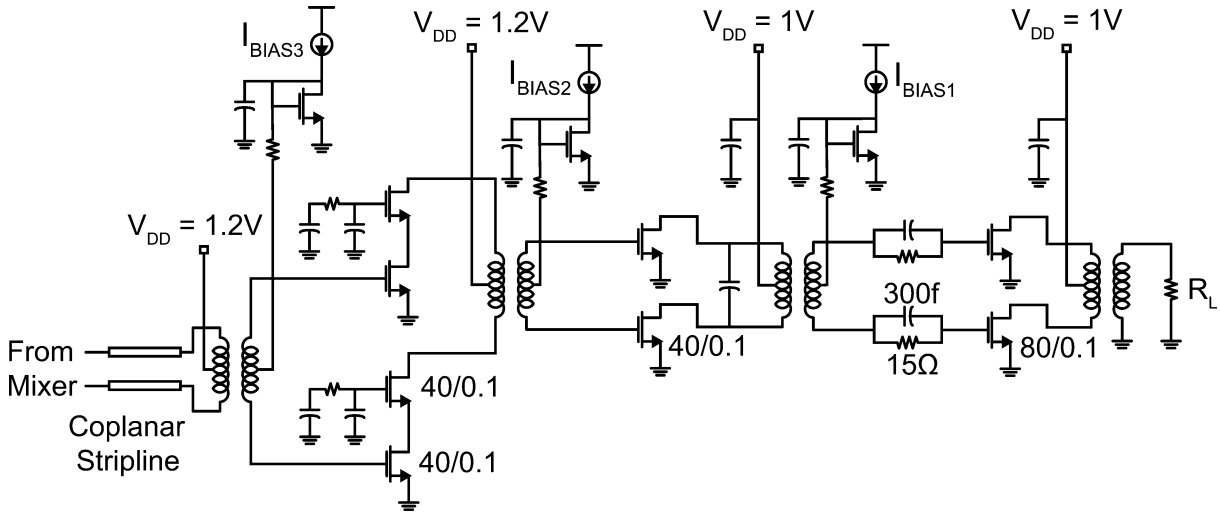

Fig. 4. Transformer-coupled PA schematic. A 1 V supply voltage is used on the output stage and its driver for improved reliability.

balances these two loss components and provides maximum power to the PA. Matching the input impedance of the power amplifier to this optimum value is crucial to minimize loss. This impedance transformation was achieved by the use of a transformer composed of two loop inductors stacked vertically to provide high coupling factor. However, connecting the differential outputs of the I and Q mixers to the input transformer of the PA creates appreciable lead inductances. If unaccounted for, these leads would cause unwanted impedance transformation and thereby increase combination loss. In order to avoid this, these leads have been modeled as edge-coupled differential striplines and absorbed into the impedance matching network design. The modulator is designed to provide -2 dBm output power and has a measured power consumption of 19.2 mW under nominal settings.

The combined output from the quadrature mixer is fed to a transformer-coupled, pseudo-differential power amplifier (Fig. 4). This design is an improved version of the PA presented in [8]; specifically, an extra cascode driver stage (both common-source and common-gate devices are 40 μm/0.1 μm) has been added to increase the power gain of the amplifier chain so that it can be driven by the on-chip mixer. In addition to gain enhancement, the cascode configuration has better stability, and its higher reverse isolation maintains the input impedance of the PA (and hence the impedance seen by mixer) largely independent of any possible loading variations down the chain. The last two stages are common-source configurations to increase output power. However, to reduce power consumption and enhance efficiency, the driver common-source devices (40 μm) have been scaled by a factor of two in comparison to the output devices, with optimized transformers performing the necessary inter-stage impedance matching with minimum possible loss. The output transformer performs both impedance matching to the external 50 Ω load, as well as differential-to-single-ended conversion. It employs two vertically-coupled loop inductors of diameter 42 μm. The measured minimum insertion loss (derived from S-parameters) of the transformer is 0.9 dB. The PA is operated from a 1 V supply in order to improve reliability, and has a simulated small signal gain of 14 dB at 60 GHz; the power gain of the PA has been verified by measuring the output

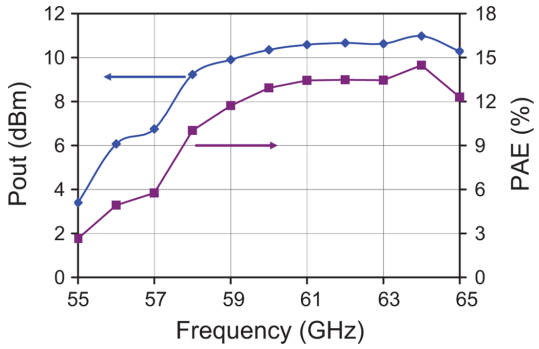

Fig. 5. Measured transmitter output power and derived PA PAE.

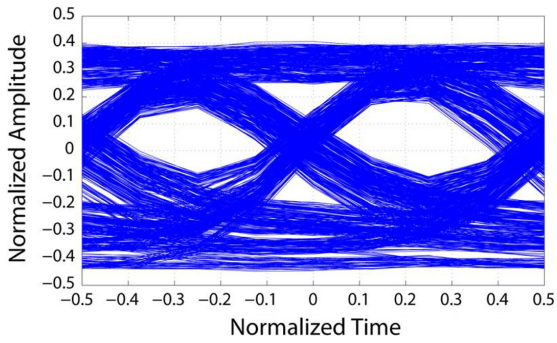

Fig. 6. Measured transmit eye diagram of the I-channel while transmitting 5 GS/s in QPSK.

power of the modulator in a separate test chip. The PA achieves 11 dBm of output power with a peak PAE of 14.6% (Fig. 5).

The entire transmitter chain was tested using QPSK modulated signals created by on-chip PRBS generators (one generator for the I-channel data, and one for the Q-channel data). The 60 GHz output from the transmitter was down-converted using an external fourth-harmonic mixer and the eye diagram was observed on an oscilloscope. However, due to the availability of only a real down-conversion mixer (as opposed to a quadrature mixer which can provide both I and Q), the eye-diagram could be traced only for either the I-channel or the Q-channel, but not both simultaneously. Fig. 6 shows the eye diagram[1] when transmitting 5 Gb/s on the I-channel. Thus, with the same data rate being transmitted on the Q channel, this would be equivalent to 10 Gb/s QPSK transmission.

One of the advantages of a transformer-based design for the PA is that it also offers inherent ESD protection. At 60 GHz, conventional ESD protection diodes can have significant losses, degrading the output power in the case of a transmitter, or the noise figure in the case of a receiver. However, at 60 GHz, the sizes of the transformers required are fairly small, with winding diameter mostly between 30–70 μm. ESD transients typically last on the order of a few μs (MHz frequencies). Therefore, at these low frequencies, the secondary winding of the transformer looks like a short circuit that shunts the ESD current to ground. Since the magnetic coupling of the 60 GHz transformer reduces to very low values at MHz frequencies, there is very little voltage transfer to the primary side and hence the active devices do not see the voltage or current spikes. However, the main limitation of the transformer when used as ESD protection is the transient current handling capacity of the metal traces, which in this design are 8 μm wide. Nonetheless, as will be described further in Section VII, ESD testing of the transmitter indicates that the transformer provides adequate protection against a 400 V machine model (MM) [9] event.

[1]Some of the amplitude noise visible in the eye-diagram was traced back to loss of frequency lock between the two instruments generating the 60 GHz LO used on-chip for up-conversion and the 15 GHz LO signal used with the external fourth-harmonic down-conversion mixer. The frequency drift between the two instruments locking creates a low-frequency beat signal that manifests as amplitude noise in the transmitted eye diagram.

III. Millimeter-Wave Receiver

The receiver design consists of an ESD-protected, two-stage, cascode LNA, quadrature hybrid, I/Q downconversion mixers, and a four-stage variable-gain amplifier (VGA). The receiver shares the VCO and PLL with the transmitter. The basic building blocks of the LNA, mixer, and VGA follow the same design presented in [10]. ESD protection was however added to the LNA as a part of the input matching network in order to enable packaging (Fig. 7). The ESD protection network consists of three 300 μm shorted shunt stubs, which at the <1 GHz frequencies where most of the ESD energy is concentrated [11] shunt the ESD-induced input current to ground. At mm-wave frequencies, these same shunt stubs form a ladder matching network that causes an impedance transformation. This extra transformation requires some adjustment of the existing transmission line based matching network to maintain a 50 Ω match, but the overall insertion loss is increased by only 0.7 dB from 55–65 GHz. The design of this ESD protection circuit is described in greater detail in [12].

This ESD circuit was designed to provide protection against both the human body model (HBM) [13] and the machine model (MM). However, MM ESD events cause significantly higher current levels than HBM events and generate a bidirectional damped oscillation that can destroy resistive metal structures with thin metal layers. Therefore, the design of the protection network is largely driven by achieving sufficient protection against these MM events. Specifically, the protection network uses three stubs (rather than a single stub) in order to distribute the large ESD currents and to progressively lower the voltage as the ESD event propagates toward the LNA. Furthermore, in order to ensure sufficient current handling capability, each of these stubs is implemented using the top two metal layers strapped together with vias. The resulting simulated voltage at the gate of the nMOS device in the LNA due to a MM ESD event is less 0.3 V (Fig. 8), and ESD tests (described further in Section VII) performed on the fabricated transceiver chip confirm protection against up to 400 V MM events.

One of the largest drawbacks of transmission-line based designs like this receiver are their large required area. It is thus important to find ways of reducing this area where possible. In this design, in order to extract the RF I and Q signals, the output of the LNA is split using a quadrature hybrid that is designed to provide 50 Ω input and output matching. Standard hybrid designs have branch-lines with dimensions on the order of $\lambda/4$, which is large even at 60 GHz. It is possible to reduce the size of the branch-lines by employing shunt capacitive loading [14], but this requires high characteristic impedance branch-lines in

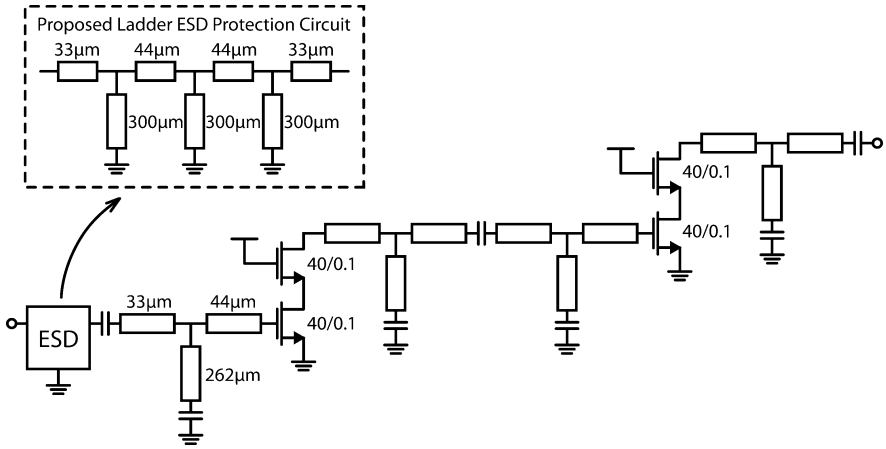

Fig. 7. Schematic of LNA using transmission line based ESD protection merged with input matching network. The design of the inter-stage and output matching networks is described in detail in [10].

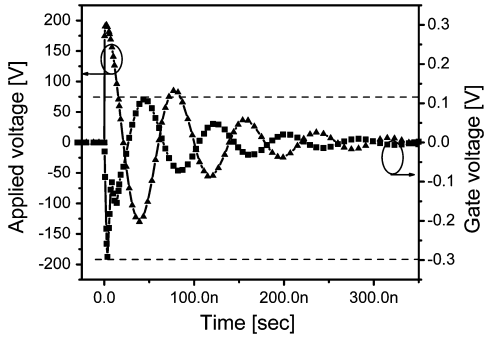

Fig. 8. Simulated ESD transient voltage applied to LNA (200 V MM) and resulting voltage transient appearing at the MOS gate.

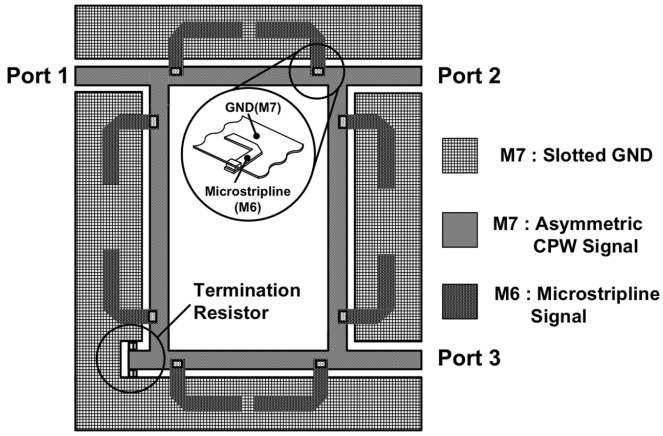

Fig. 9. Hybrid layout detail.

order to maintain 50 Ω input and output matching. Thus, in this design the branch-lines are realized using asymmetric coplanar waveguide (ACPW) transmission-lines in order to achieve high characteristic impedance with low spacing between signal and ground conductors. This design reduces substrate losses and helps to alleviate discontinuity effects at the branch-line junctions. To minimize phase errors from process variations, distributed microstrip shunt-stubs are used to realize the desired capacitors.

Fig. 9 shows the detailed structure of the hybrid; this quadrature hybrid consumes only 20% of the area of a conventional design. 3-D EM simulations indicate that this hybrid achieves 2 dB insertion loss and 4% phase error over 7 GHz of bandwidth. In order to enable further characterization, the hybrid was also fabricated as a stand-alone test structure. Measured S-parameters of this standalone hybrid after 3-port de-embedding [15] are shown in Fig. 10. The worst case measured insertion loss across the band was 2.5 dB for the I channel and 4 dB for the Q channel. The worst case measured magnitude error between I and Q across the band was approximately 1.5 dB. These errors are partially due to the fact that the matching was shifted down to 58 GHz from the expected center frequency of 60 GHz.

A layout error in the test structure made it difficult to measure phase differences accurately. Instead, the phase error can be approximated based on the measured isolation and return loss magnitudes. The hybrid can be analyzed using *ABCD* parameters based on even-odd mode analysis from the direct measurement of the isolation between Port 2 and Port 3 [16]. Using this analysis and the S-parameters in Fig. 10, we can estimate that the I-Q phase error is maximally bounded at 13 degrees. Because we assume that the isolation is only dependent on phase error and impedance variation, this estimated I-Q phase error bound is somewhat pessimistic, as will be shown later through a more accurate measurement in Section VI. Since the ACPW structure has asymmetric field distribution over the oxide layers, the main discrepancy between simulation and measured results is most likely caused by an error in the modeling of the substrate stackup used in the EM simulation.

IV. High-Speed Baseband

As this transceiver design is targeted for high data rates, the baseband must operate at GHz frequencies while providing functions such as phase rotation to account for phase differences between the transmit and receive LO as well as equalization to counter ISI. Utilizing complex modulation schemes and a traditional ADC/DSP-based implementation approach would, however, require baseband power consumption on the order of 100 mW or more [17]–[19]. Instead, we chose to use a

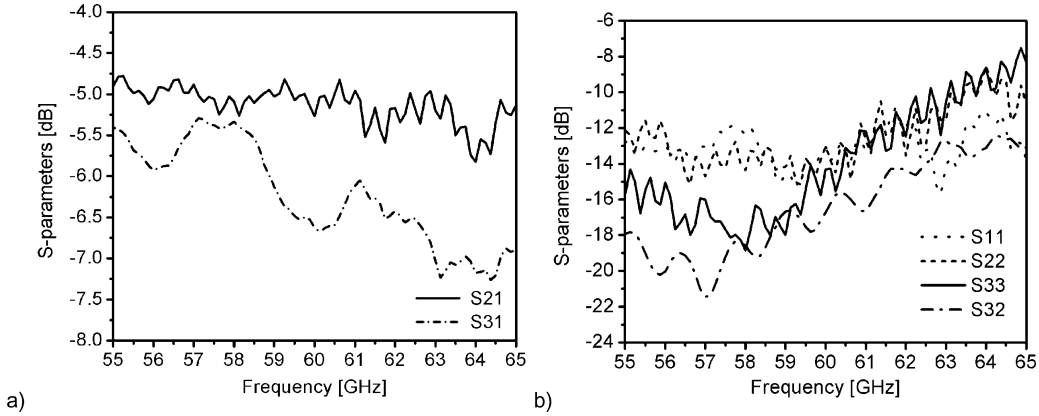

Fig. 10. Measured hybrid S-parameters: (a) insertion loss, (b) isolation and matching.

simple modulation scheme and follow the approach taken by high-speed chip-to-chip links. Specifically, the baseband uses only as many comparators as are required to extract the data while performing mixed-signal processing around those comparators to counter non-idealities in the transceiver and the channel.

In order to compensate for the phase difference between the transmit and receive LO, the mixed-signal baseband includes a digitally programmable analog phase rotator (Fig. 11). The phase rotator consists of a switched bank of current-summed transconductance (g_m) stages whose polarities and input sources are selected digitally in order to perform a vector summation. With the phase quadrant selected separately by polarity controls, achieving $\sim 5^\circ$ phase resolution requires the gains of the I and Q channels to be controlled with 4-bit resolution. In a direct implementation [20] [Fig. 12(a)], this would require 16 g_m cells for each of the rotator's amplifiers; i.e., each output would be driven by 32 g_m cells (16 from I input and 16 from the Q input). However, since the phase rotator's gain should not vary with the phase setting [i.e., the rotator's output should remain on the unit circle; see Fig. 12(b)], all 32 of these cells will never be turned on simultaneously. Therefore, the direct implementation has extra parasitic drain capacitance (by a factor of $\sqrt{2}$) that leads to a similar increase in the phase rotator's power dissipation for a given bandwidth. Therefore, in this design we leverage knowledge of the phase rotator's functionality by allowing 8 of the cells to choose between the I and the Q inputs, resulting in only 24 total cells per output [Fig. 12(c)]. Note that instead of shutting down the tail current source when the "0" input is selected, a common mode voltage is connected to the input in order to keep the output common mode constant. Finally, the quadrant selection is implemented by a Gilbert cell which is hard switched by the polarity control signal. Each phase rotator achieves a simulated bandwidth of more than 3.5 GHz when loaded by the DFE current switches and comparators (described next) with a measured current consumption of 1.2 mA.

Even under line-of-sight conditions, the receiver must also be able to counter channel non-idealities such as reflections that result in residual ISI (Fig. 13). In order to counter such ISI, a 5-tap mixed-signal complex decision feedback equalizer (DFE) was implemented. Much like high-speed link DFEs [21], this

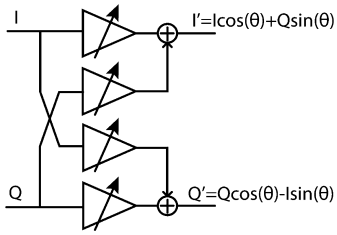

Fig. 11. Phase rotator block diagram.

design uses a mixed-signal half-rate architecture with a loop unrolled [22] first tap in order to move the critical timing path purely into the digital domain. Since the equalizer is complex and must handle ISI from all four possible previous QPSK symbols (Fig. 14), the unrolled first tap uses 4 comparators with tunable thresholds. Since there are a total of 16 comparators (4 per clock phase, per I/Q channel), the comparators use near minimum-sized devices to minimize power consumption, which introduces a 3 sigma voltage offset of about 100 mV. An 8-bit current-mode offset cancellation DAC is employed to cancel the DC offset as well as serve as the first tap of the DFE operation. DFE summation for the rest of the taps is implemented as current mode addition at the output node of the phase rotator. Each tap coefficient is controlled by a 6-bit current mode DAC, and each phase rotator output is loaded by eight switched-current cells (four for the direct feedback, and four for the cross-channel feedback). When clocked at 2.5 GHz (10 Gb/s QPSK), the entire mixed-signal baseband consumes only 12 mW.

V. LO Generation and Distribution

Low-power generation and distribution of LO signals is a challenge in all mm-wave transceiver designs. To generate a stable LO, this transceiver uses a fixed division ratio, charge-pump-based PLL with a 117 MHz reference (making a crystal or MEMS source feasible) and a target loop bandwidth of 4 MHz. Since the transceiver is designed to utilize the entire 60 GHz band as a single channel, programmable division ratios are not required in the PLL. In order to remove the need for a power-hungry 60 GHz divider, a push-push oscillator is used, leading to the PLL topology shown in Fig. 15. The most challenging aspects of this design are the VCO and the first divider that must

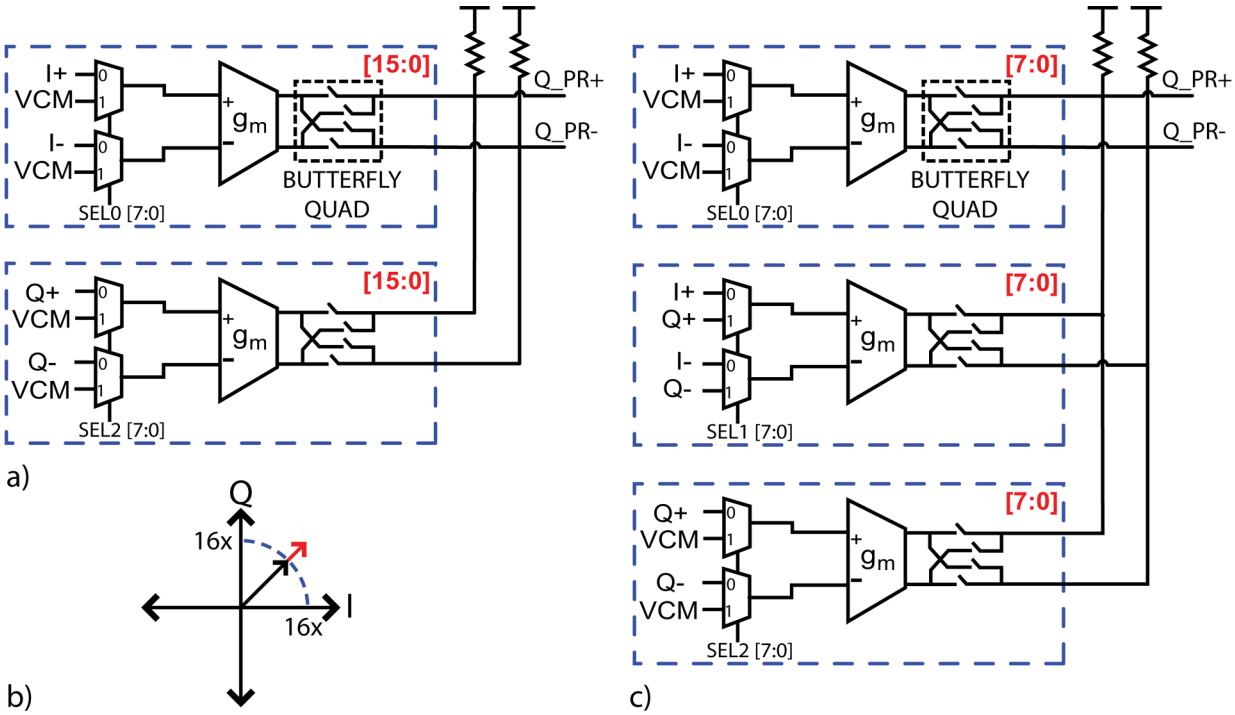

Fig. 12. Phase rotator detail: (a) direct implementation, (b) unnecessary gain variation with direct implementation, (c) g_m-cell sharing implementation. The input MUX is implemented by pMOS transistors since the voltage level at the input is approximately 0.8 V.

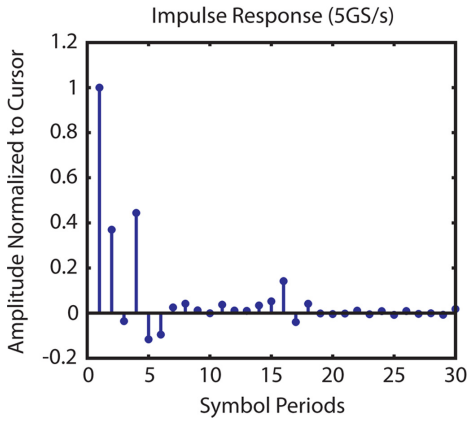

Fig. 13. Impulse response of a LOS channel (I channel to I channel) measured with a directive antenna.

operate at very high frequencies while maintaining good power efficiency. The core of the oscillator (Fig. 16) is based on a differential Clapp topology tuned to 30 GHz. nMOS varactors are utilized in the resonant tank to allow tuning for process variations. The differential outputs of the core are pushed into a secondary resonant tank that extracts the single-ended second harmonic at 60 GHz from the common mode. Due to the inductors, all three terminals of the MOS transistors in the oscillator core can have very large swings. To limit these swings for reliability, the VCO is operated from a 0.7 V supply and draws 12 mA. It has a measured tuning range of 4.4 GHz (59.6–64 GHz) at the push-push output, as shown in Fig. 18. The tuning range is shifted up in frequency due to overcompensation of the expected parasitics in the design. The simulated output power at 60 GHz is −9 dBm, whereas the measured power is 6 dB lower. The precise source of this discrepancy is presently unknown, although simulations show that this phenomenon can be explained by a reduction in the loaded Q of the resonant tank.

The first divider in the chain is the most challenging to design since it must operate with a 30 GHz input signal. A static CML flip-flop has a much wider locking range but is simply not fast enough to achieve division with a 30 GHz input. Instead, a "pulsed-latch" topology [23] is used which can achieve higher speeds of operation by the use of a single CML latch and two delay stages. In this 90 nm technology it was not necessary to use inductive shunt or series peaking techniques inside of the pulsed-latch in order to achieve the desired speed. Instead, a triode region pMOS load was employed to allow tuning of the divider performance to ensure divider lock over PVT variations, while at the same time reducing the required area. The 30 GHz divider schematic is shown in Fig. 17 and draws 8 mA from a 1.2 V supply. The master-slave design in the 15 GHz divider reuses the CML latch from the 30 GHz divider and consumes a total of 4.25 mA from a 1.2 V supply. The remaining divider chain is composed of TSPC and standard cell D-FF dividers. Including the VCO, the entire PLL consumes 26.3 mW.

The measured output spectrum of the locked PLL is shown in Fig. 19. The high spur levels of −23 dBc are likely due to supply injection, which couples onto the VCO control node through the loop filter, as well as due to mismatch in the charge pump. The phase noise spectrum of the locked PLL is shown in Fig. 20. From this measurement it appears that the actual loop bandwidth

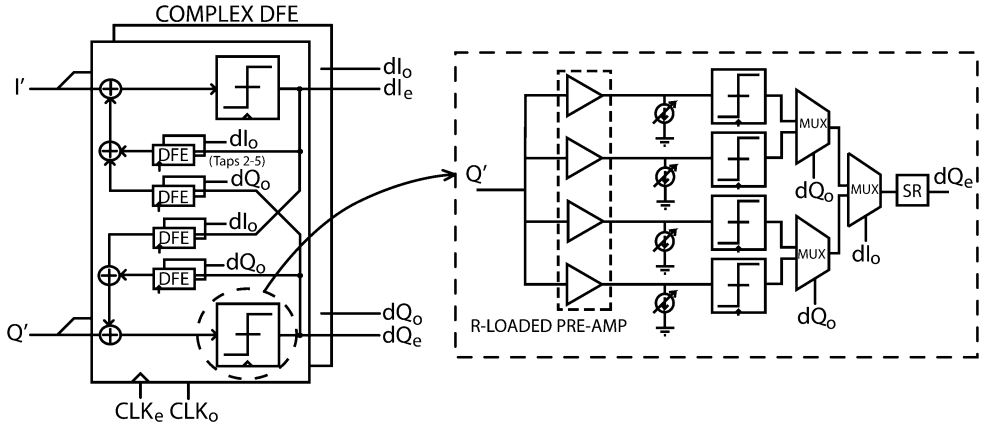

Fig. 14. Five-tap complex DFE with unrolled first tap. The DFE/slicer circuits operate on both edges of the baseband clock (o. odd, e. even).

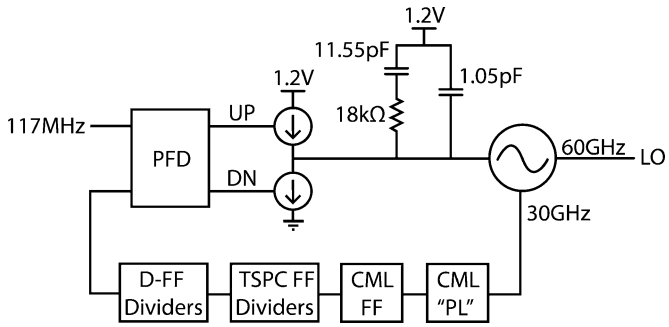

Fig. 15. Constant-N charge pump PLL block diagram.

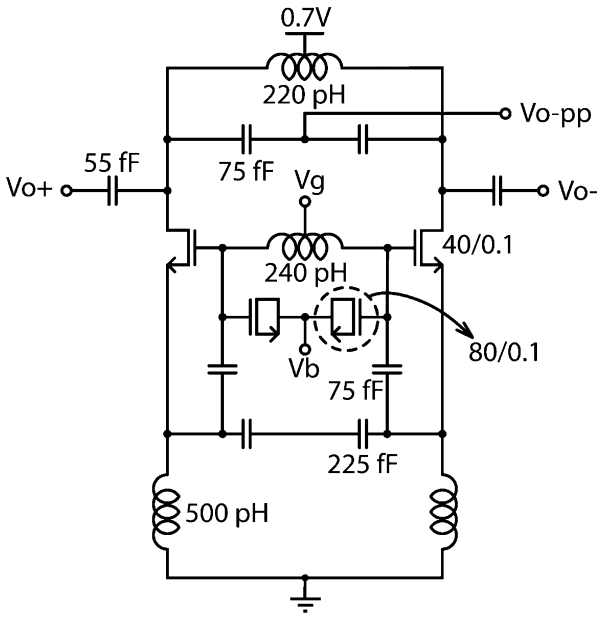

Fig. 16. VCO schematic. For reliability, the VCO is operated from a 0.7 V supply.

is closer to 1–2 MHz.[2] The phase noise of the VCO can be estimated from this plot by looking well outside the loop bandwidth. At a 10 MHz offset from the 60 GHz carrier, the phase noise is −112 dBc/Hz. This leads to a FOM for the oscillator [calculated with (1), below] of −178.4 dB.

$$\mathrm{FOM} = L\{\Delta f\} - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log\left(\frac{P_{\mathrm{DC}}}{1mW}\right). \quad (1)$$

Once the LO has been generated by the PLL, the challenge of distribution still remains. In this design, the VCO is shared between the transmitter and receiver and must feed both in-phase and quadrature mixers, thus requiring power splitting and/or quadrature signal generation. On the transmitter side, the quadrature splitting is performed in the LO path, while on the receiver side the quadrature separation is performed in the RF path in order to maximize our ability to reuse existing blocks. The LO path (Fig. 21) was designed in a 50 Ω CPW transmission line environment to allow routing the signal over long distances. The 60 GHz output from the VCO is first split into the transmit and receive sides using a Wilkinson divider. On the receive side, another Wilkinson divider splits the signal into two LO signals in phase. On the transmit side, a 90° hybrid (Fig. 9) splits the signal into two LO signals in quadrature. The cascode amplifiers in the LO path provide sufficient gain to overcome the losses of the passive splitters and transmission lines and to provide some margin for variations in VCO output power. To allow for design reuse, all buffers are sized and biased identically, consuming approximately 7 mW each.

The complete LO path consumes 50 mW, which is a substantial portion of the total transceiver power and is larger than the power consumption of the PLL itself. Thus, optimization of the LO distribution to reduce its power consumption is an important area for further research. For example, although the LO chain power might be reduced by alternative architectures that require fewer buffers (e.g., quadrature or fundamental-frequency VCOs with higher output power), these architectures tend to significantly increase the core VCO/PLL power consumption [3], [4]. Furthermore, regardless of the topology used, the final four buffers must provide sufficient voltage swing to the four mixers, thus setting a lower bound of the power dissipation of the LO distribution. As was mentioned in Section II, the transmit mixer requires −4 dBm of LO power, while the receive mixer presents a lower impedance at the LO port and requires −2.5 dBm of LO power for high voltage swing and conversion

[2]The fast roll-off in phase noise near 2 MHz offset is likely due to excess 1/f noise in the charge pump.

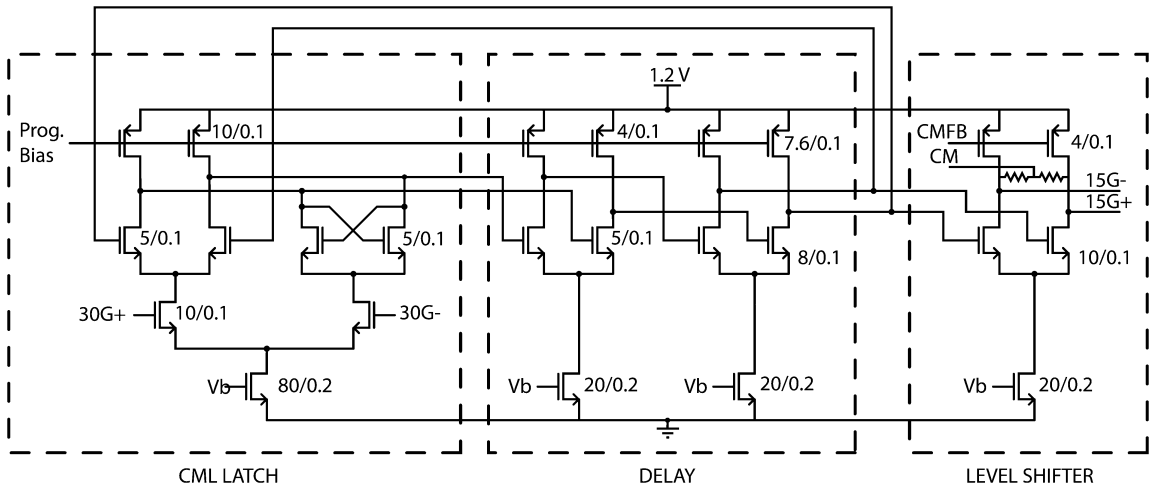

Fig. 17. CML pulsed-latch divider schematic.

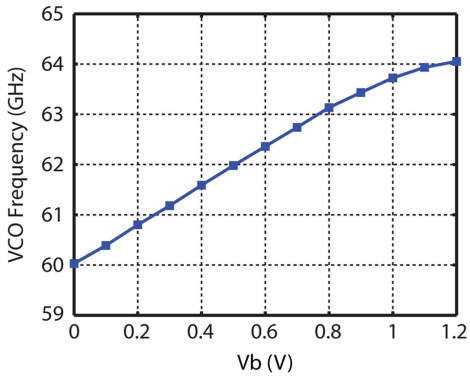

Fig. 18. Measured VCO frequency tuning range ($\mathrm{Vdd} = 0.7$ V, $\mathrm{V_g} = 0.65$ V).

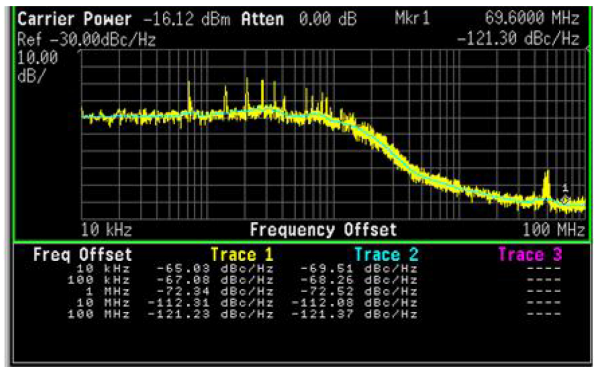

Fig. 20. Measured PLL phase noise spectrum.

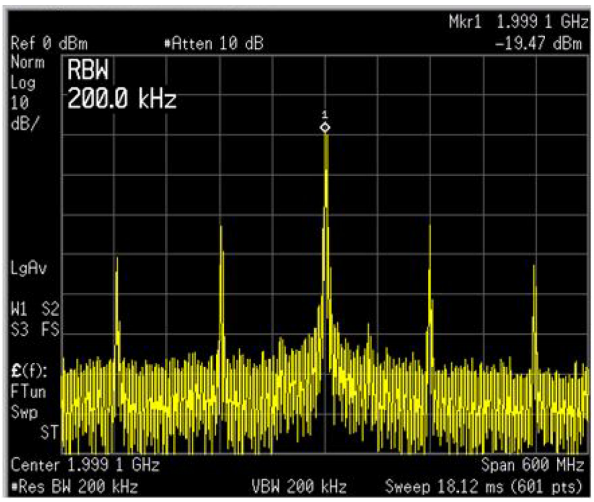

Fig. 19. Measured spectrum of the locked PLL. In simulation, the charge pump alone causes −35 dBc reference spurs.

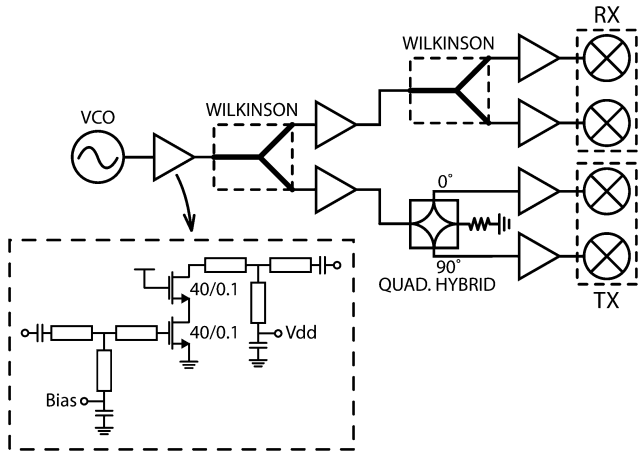

Fig. 21. LO distribution network with amplifiers providing 7 dB gain and power splitters each having 4–5 dB effective loss (3 dB from splitting and 1–2 dB loss). The distribution network is designed to provide at least 10 dB gain from the VCO output to each mixer despite power splitter and transmission line losses.

gain. Moving away from a 50 Ω environment would allow the designer to optimize the size and bias of the final four buffers to provide the required voltage swing to the mixers with lower DC power consumption. Since this design used a 50 Ω environment to facilitate design reuse, the final four buffers are thus overdesigned and consume more than 50% of the DC power in the chain. Preliminary calculations show that a factor of two reduction in DC power consumption is possible in these final four buffers with a proper redesign, with power reduction limited by the low output impedance of transistors at 60 GHz and finite quality factor of matching network components. Furthermore,

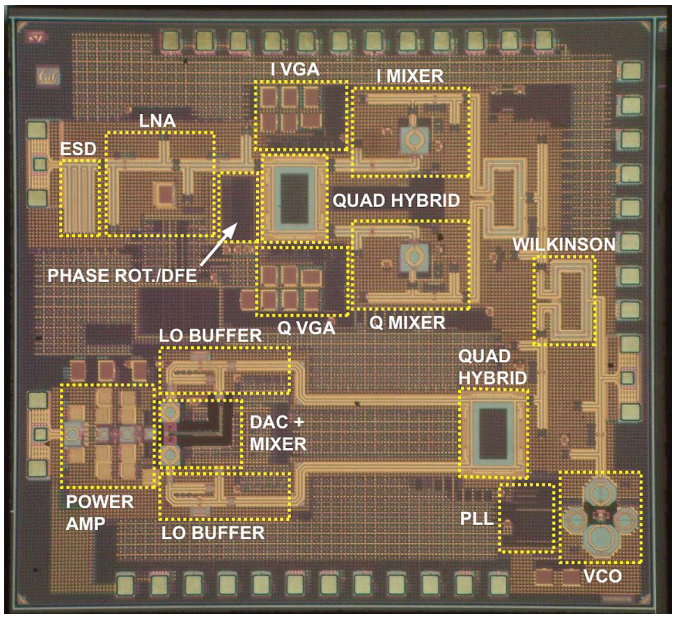

Fig. 22. Transceiver die photo.

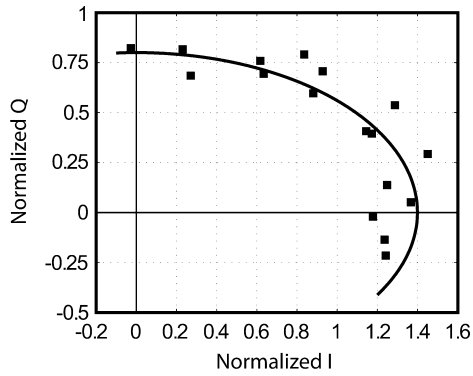

Fig. 23. Measured phase rotator first quadrant constellation (normalized).

the power consumption of the remaining buffers in the chain can also be reduced by using transmission lines with Z_o higher than 50 Ω as long as low loss can be maintained in the matching networks and transmission lines.

VI. Transceiver Testing Results

The transceiver was fabricated in a standard one-poly-seven-metal (1P7M) 90 nm CMOS process with no special RF options. The die measures 2.5×2.75 mm^2 (Fig. 22) and was bonded in a chip-on-board configuration to enable DC signals and clocks to be driven through a PCB while directly probing the 60 GHz signals using a probe station. Communication between transceiver chips was tested in 3 stages: loop-back, chip-to-chip over a wire, and chip-to-chip wireless. In the loop-back mode, a single transceiver chip was used to test and debug individual components, with the output from the PA on the transmitter side directly wire bonded to the input of the LNA on the receiver side. Using the loop-back mode allows us to transmit controlled signals into our receiver for debug purposes. In the wired and wireless modes two transceiver chips were used, one serving as the transmitter, and the other as the receiver to achieve communication between two separate chips. In the wired mode, a 3 m 1.85 mm coaxial cable was connected between the PA on the transmitting chip and the LNA on the receiving chip. In the wireless mode, each transceiver was connected to a 25 dBi horn antenna placed approximately 1 m apart. Since this design does not include control loops such as carrier recovery or clock and data recovery, these functions were performed manually during testing.

Using the on-chip PRBS generators/checkers, data transfer rates were tested in each of the three configurations described above in order to find the maximum data rate possible without receiving any errors. Due to limited testing time, data bursts were limited to 10^{11} bits, and thus we define the maximum data rate here as the maximum achieved data rate while receiving no errors in those 10^{11} bits. Furthermore, the bit error rates (BER) we report are limited to 10^{-11} due to this limited measurement time and not due to any inherent design limitation. The highest data rates achieved are 7 Gb/s in loop-back mode, 6 Gb/s over the wired channel, and 4 Gb/s over the wireless channel.

These data rates are clearly below our target of 10 Gb/s—the principal limitation to increased data rates appears to be noise on the global 1.2 V supply caused by the digital baseband test circuitry (such as the PRBS generators and checkers) coupling into the inputs of the VGAs. Although this principal limitation would be relatively straightforward to resolve by splitting and/or regulating the supplies of the RF/mixed-signal baseband, examining additional limitations stemming from the RF and baseband provides further insights into the operation of these circuits.

The phase rotator constellation (Fig. 23) illustrates the non-idealities present in the RF path. The constellation is constructed by sending separately identifiable signals on I and Q in loop-back mode and varying the phase setting codes in the receiver. The signals received on the I and Q channels are then measured using the baseband receiver by sweeping the thresholds of the comparators and plotting the CDF of the signal [24]. In this way we can identify the cross talk between the I and Q channels. The solid curve shows a best fit line through the measured constellation, which should ideally be a quarter-circle. From Fig. 23 we can identify two effects. First, there is an amplitude mismatch between I and Q. Second, we can see that I and Q are not truly in quadrature, but are in fact separated by $\sim 100^\circ$. This is most likely due to the I-Q phase mismatches in the transmit and receive hybrids. As described in Section III, this phase mismatch has an upper bound of 13°. However, with this more accurate measurement we see that the phase mismatch is closer to 5° for each hybrid. Measuring the phase rotator constellation also allows us to find the phase rotator transfer curve (Fig. 24) more accurately by deembedding the effects mentioned above. Doing so reveals that the phase rotator is fairly linear, although the measurements are still relatively noisy due to limited averaging.

As evident in the BER plot in Fig. 25, another limitation to the achievable data rate is a baseband timing offset between the I and Q channel. Interestingly, although this timing offset has several sources, the majority of the offset is actually generated in the RF path. First, there is some gain and phase mismatch in the hybrid, which on the receive side is in the signal path. The more interesting cause of baseband I/Q timing mismatch comes from the upconversion mixer in the transmitter. From Fig. 3 we can see that there are eight large transistors forming

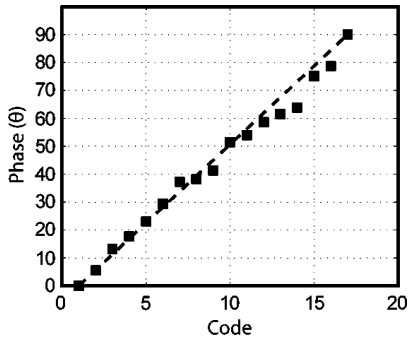

Fig. 24. Measured (squares) and ideal (dashed line) phase rotator transfer curve.

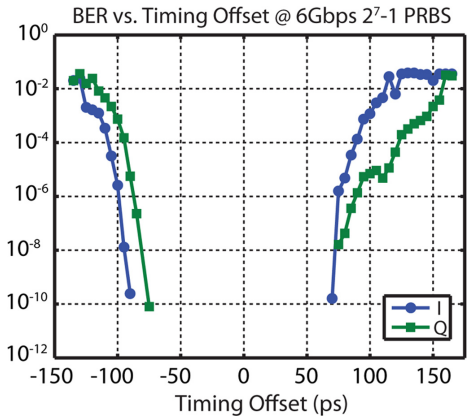

Fig. 25. BER versus receive clock timing offset for 6 Gb/s transmission of 2^7-1 PRBS over the wired channel.

the switching quads that must be placed in close proximity to each other to reduce parasitics. This makes symmetric routing of the mixer inputs and outputs practically impossible. Furthermore, the I and Q mixer outputs are simply shorted together, leading to complex loading conditions that contribute to timing mismatch. While the mixer's output lead inductances can be somewhat taken into account in the PA input matching network, the asymmetry cannot be accurately corrected. Unfortunately, the only way to isolate the outputs would be to use an isolating power combiner which would add significant area overhead and introduce additional loss. In all, the mismatch between I and Q due to all effects in the upconversion mixer is approximately 14 ps. In addition to the RF-induced I/Q timing mismatch, due to a layout error, the lengths of the wires connecting the I and Q VGA outputs are imbalanced, which contributes to the timing mismatch as well.

As mentioned in earlier sections, both the LNA and PA were designed with ESD protection circuitry, either explicit as in the case of the LNA, or inherent as in the case of the PA. To validate these circuits, ESD tests were performed on the transceiver based on the MM, which, as described in Section III, is more difficult to withstand than HBM. A 200 pF capacitor was charged to the given voltage to model the charged metallic handler and then discharged into the DUT using a mechanical switch. DC needle probes were used to contact the pads with the positive side of the charged capacitor on the signal pad and the negative side on the ground pad. Both the LNA and PA ESD protection were tested repeatedly using this setup. Based on our tests, both the LNA and PA were adequately protected for 400 V MM ESD events.

TABLE I
POWER BREAKDOWN

Block	Power (mW)	Block	Power (mW)
LNA	18	TX DAC/Mixer	19.2
Mixers	15.6	PA	82.2
VGAs	23	VCO	9.8
DFE and Phase Rotator	12	Dividers	17.3
VCO	9.8	LO Buffers	36
Dividers	17.3	Bias and Clock Dist.	5
LO Buffers	36	**TOTAL TX**	**169.5**
Bias and Clock Dist.	6.3		
TOTAL RX	**138.3**		

VII. CONCLUSION

This paper describes the design and characterization of an integrated 90 nm CMOS 60 GHz transceiver including RF and BB signal paths as well as LO generation and distribution. Energy efficiency is one of the key challenges to utilizing 60 GHz transceivers in mobile applications, and hence was a principal focus in this design. Leveraging mixed-signal techniques originally developed for high-speed electrical links enabled a baseband receiver signal path that dissipates only 12 mW at 5 GS/s. At the transmitter, tapered transistor sizing in the PA and current sharing in the modulator provide significant efficiency improvements. Finally, although LO generation and distribution remain challenging, the power consumed in these circuits can be substantially reduced by moving away from 50 Ω designs.

To enable low-cost packaging of such a transceiver, ESD protection of even the mm-wave pads is highly desirable, and hence this design featured a simple transmission line-based ESD protection circuit that adds only 0.7 dB of additional insertion loss at the receiver. Similarly, utilizing transformer-based matching networks in the transmitter provides inherent ESD protection for the PA and leads to a significant reduction in area.

The transceiver operates from a 1.2 V supply and consumes 170 mW in transmit mode and 138 mW in receive mode (Table I). Using the on-chip $2^{31}-1$ PRBS generator and checker, a BER of $<10^{-11}$ (limited by measurement time) was measured for the transceiver while sending 4 Gb/s with QPSK modulation over a 1 m wireless channel with 25 dBi horn antennas. The same BER was measured while sending the same sequence at 6 Gb/s over a 3 m wired channel.

ACKNOWLEDGMENT

The authors would like to acknowledge the students, faculty and sponsors of the Berkeley Wireless Research Center, the National Science Foundation Infrastructure Grant No. 0403427, chip fabrication donated by STMicroelectronics,

DARPA, C2S2, Cascade Microtech, VTT, and Berkeley Design Automation for the donation of FastSPICE.

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