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1 GHz High Sensitivity Differential Current Comparator for High Speed ADC

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Abstract

A fast responding low power differential current comparator operating at 1 GHz clock speed is presented in this paper. The comparator proposed in this paper is composed of three stages. The paper presents a modified version of Wilson's current mirror comparator for the detection of very low current. This serves as the first stage which is current to voltage conversion followed by comparison stage and buffer stage. Working at a supply of 1.8 V, the comparator is capable of sensing a minimum difference of 4 nA for 6 µA reference current. In addition to low power dissipation this circuit shows a swift response resulting in a propagation delay which is less than 0.9 ns for an input difference of 0.1 µA. The current comparator is simulated using Cadence Virtuoso Analog Design Environment 0.18 µm CMOS technology

Keywords-*current comparator; Wilson's current mirror comparator; dynamic latch; kickback noise; ADC.*

INTRODUCTION

In recent years, Comparator on the mode of current has been focused by many researchers in CMOS technology [1]- [4]. As the mode of operation is shifted from voltage mode to current mode, it has become one of the most important blocks in numerous in digital and analog circuits. The various advantages of operation of comparators in current mode are the operating at very low voltages, better noise figure without compromising speed and bandwidth. Current mode comparators have a wide range of circuit applications like analog to digital converters and vice versa, neuromorphic electronic systems [5] where area is a key factor and also in circuits requiring low current comparison which can be able to detect minute current signals which can be useful for the sensors for sensing temperature, pictures etc. Current mode comparators work on the principle that if there is a differential current flowing through the comparator then the comparator is able to distinguish the level of difference in current with respect to the reference current. The principle seems to be simple but when it is actually implemented, the circuit will give the impression of very complex in nature. When the circuit is put into operation, then it was observed that for executing the principle is very difficult especially when the magnitude of the current is very less during high speed operation. The main factors of deliberating the design of circuit are the input impedance and time response. The paper further describes regarding Wilson's current mirror comparator in section II, and then the modified version of this comparator implemented in the paper is discussed in section III. In section IV, the complete modified architecture and in section V, simulated results of the circuits are conferred.

Review of Wilson's Current Mirror Comparator

The existed Wilson's current comparator circuit [1] is shown in figure 1. The circuit

performs two main tasks. Firstly, it carries out current subtraction of the input current from the reference current. Secondly, negative feedback in the circuit reduces the input impedance.

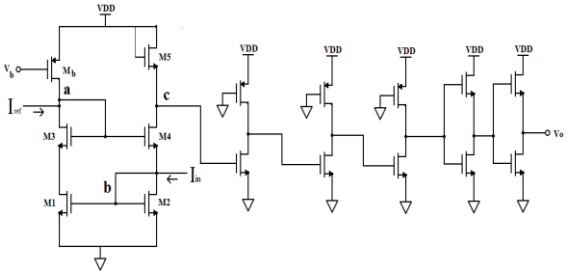

Fig.1. *Schematic of Wilson's current mirror comparator*

To improve the performance of the circuits, the MOSFETs M1-M4 are connected and a diode connected load is present in the form of the MOSFET M5. The reference current Iref is compared with the input current Iin by the circuit topology. The circuit topology working can be described as the reference current flows through M3 making the drain current of M1 and M2 equal to Iref, the drain current which is the output current, flowing through M4 becomes equal to the current difference between reference current and input current. Thus, if Iin is larger than Iref, the output current Io decreases thereby pulling up the voltage at the output node. But if Iin is less than Iref, the current at the output increases thus pulling up the voltage at the output. Employment of the negative feedback in the circuit provides low input impedance. Equation (1) gives the input impedance,

$$R_{in} \cong \frac{1}{g_{m2} + g_{m4} + g_{m1}g_{m4}(r_{o1} \| r_{oB})} \quad (1)$$

The above equation is further simplified if M1-M4 have the same transconductance, g_m, then equation (2) follows,

$$R_{in} \cong \frac{1}{g_m^2(r_{o1} \| r_{oB})} \quad (2)$$

PROPOSED CURRENT COMPARATOR

The proposed comparator can be divided into three stages which are stated in the following sub-section.

Current to Voltage Conversion Stage

There are some drawbacks of Wilson's current mirror comparator circuit like poor noise rejection of input power supply and similar limitations which a single ended topology faces during operation. At node c (figure 1), high offset current is observed due to limited voltage swing. This reduces the efficiency of the circuit during high speed operation for detecting very low range (in nano amps) of current. In order to improve from the above mentioned limitations of the circuit, modified version is proposed by implementing differential mode of current in lieu of single ended stage of Wilson current mirror [6] with added modification to improve the performance of the circuit.

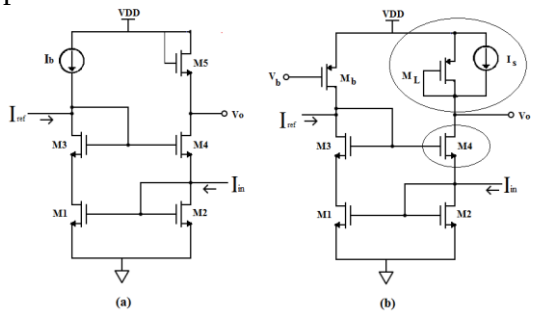

Fig.2. ***(a)****Circuit diagram of existing Wilson's current mirror comparator (b) Modifications made in Wilson's current mirror comparator*

For a wider voltage swing at the output the following changes are made as shown in figure 2(b): • The problem faced by NMOS load topologies in common-source stage is the voltage headroom limitation. The upper voltage swing is constrained to (VDD-VthN) instead of conveying the full VDD at the output, where VthN is the threshold voltage of the NMOS transistor. However replacement of NMOS to PMOS load architecture resolves this issue, providing better detection of low input

current difference. • Making (W/L)3 and (W/L)4 twice of (W/L)L, decreases the overdrive voltage of M4 since,

$$V_{OV4}\alpha \frac{1}{\left(W/L\right)_4} \quad (3)$$

hence the minimum voltage swing at the output decreases given by $V_{O(min)} = V_{OV4} + V_{OV2} + V_{thn}$.

- To increase the gain, Is which is equal to 0.63Id4, a constant current source is added to the circuit as shown in figure 2(b). This is because for a given $|V_{GSL}-V_{thL}|$, if the current decreases by a factor, say X, then $(W/L)_L$ must decrease which in turn lowers the load transconductance, given by the equation $g_{mL} = \sqrt{2\mu_P C_{OX}(W/L)_L I_{DL}}$, by the same factor, thus increasing the gain of the circuit.

Comparison Stage

This stage is subdivided into two stages: pre-amplifier stage and latch stage shown in figure 3. The latch stage regenerates the output to a full scale digital level. However due to coupling action of the large voltage level variation through the parasitic capacitance of the transistors to the input causes a disturbance in the input signal level resulting in evaluation error. In order to achieve quick response and high bandwidth, the pre-amplifier gain is kept low. The small signal differential gain in terms of device dimension is given by equation (4),

$$A_v \cong \sqrt{\frac{\mu_N (W/L)_N}{\mu_P (W/L)_P}} \quad (4)$$

where N and P represent NMOS and PMOS transistors respectively. The pre-amplifier is followed by a dynamic latch for high speed response.

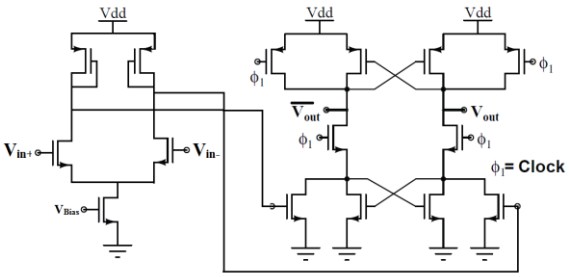

Fig.3. *Voltage comparison stage: Preamplifier and Dynamic Latch*

Buffer Stage

The third stage of the topology is the buffer stage employing two inverters connected in series to generate rail-to-rail voltage swing at the output..

ARCHITECTURE OF PROPOSED CURRENT COMPARATOR

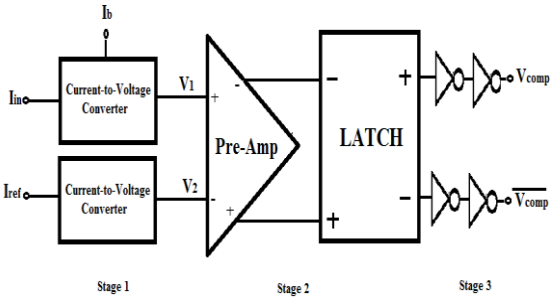

Fig.4. *Block diagram of proposed current comparator*

The complete block diagram of the proposed current comparator is shown in figure 4. The input and reference current are first fed to the circuit. A local reference current Ib is used in this stage which can be as low as 6 µA. The typical input current can be a pulse wave or a sinusoidal wave. Two separate Wilson's current mirror blocks generate two output voltage pertaining to two difference currents I_b-I_{ref} and I_b-Iin. The difference between the voltages is amplified by means of the pre-amplifier which also acts as protection against feedback noise from the latch. One of the benefits of using a differential circuit is that it brings the offset error to a minimalistic value. Dynamic latch is used for less delay working on 1 GHz clock speed. To regenerate the voltage logic at

the output, the latch outputs are passed to the buffer stage at the end.

SIMULATION RESULTS

The schematic design of the proposed comparator is obtained using Cadence Virtuoso design tool in 0.18 µm CMOS technology and simulated with Spectre environment. Fig. 5 shows the AC analysis of the circuit. The overall gain is 6.7 dB and the bandwidth is 3 GHz. The phase cross over at 0 dB is 75o . The propagation delay calculated through transient analysis is 0.87 ns under 0.1 µA input current difference. Table I summarizes the rise and fall delay. It can be inferred that with the increase in delay, input difference is also increased. Figure 6 shows the input and output waveforms of the comparator when a clock frequency of 1 GHz and reference current of 6 µA with a difference of 0.1 µA at its input, all computed at no-load condition is applied. The circuit is being operated at 1.8 V powersupply.

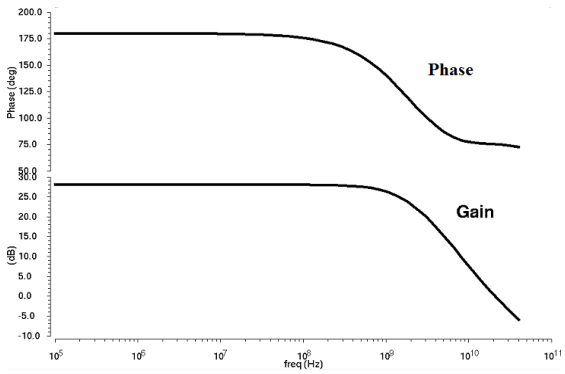

Fig.5.*Gain and phase curve of the pre-amplifier*

An average power dissipation of 269.9 µW is recorded at no-load condition. For a high frequency operation, a good power-delay product as well as offset is observed for the circuit.

Parametric analysis of the output voltage with varying input current less than 6 µA reference current is shown in figure 7. It has been observed with decrease in difference between input and reference current, the propagation delay increases as shown in figure 8. But if the input current difference is decreased beyond 2µA, the delay becomes nearly constant, as the delay time is generally determined for higher input difference from the rail-to-rail amplification.

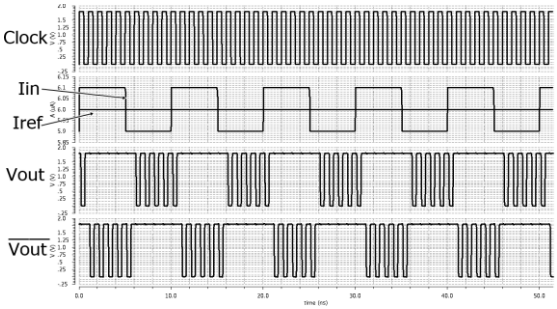

Fig.6. *Output response of the comparator for 1µA input difference and 250 MHz input frequency*

The minimum input offset recorded by the circuit is +/-4 nA operating at 1 GHz clock frequency. Thus highly precise current comparison can be expected. Table II shows the power and delay variation with respect to temperature.

Table I Propagation Delay of proposed comparator

Rise time	0.601 ns
Fall Time	1.130 ns
Total Propagation Delay	0.8655 ns

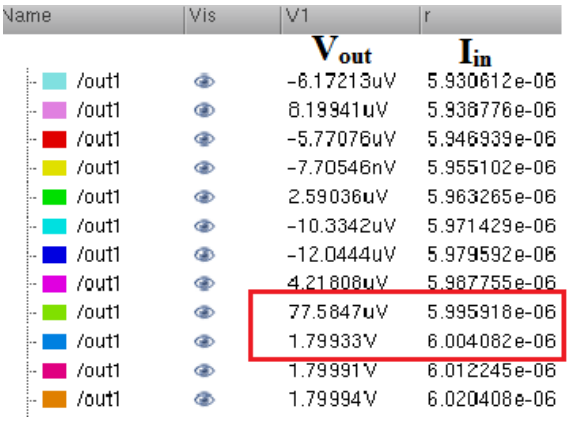

Fig.7. *Parametric analysis for input current sensitivity value determination when I_{ref} is 6 µA*

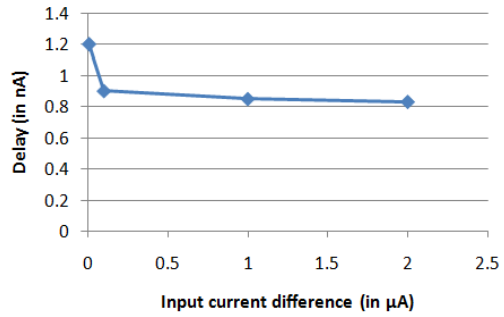

Fig.8. *Delay Vs Input current difference of comparator*

From the table III, the results of the proposed comparator and existing differential current comparator in [6] shows the power dissipation has reduced by approximately 61% and delay has reduced from 0.95 ns to 0.87 ns.

Table 2: *Power and Delay variation with input current frequency*

Temperature (^{0}C)	**Avg. Power Dissipation**	**Propagation Delay**
50	247.6 µW	0.844 ns
60	248.9 µW	0.849 ns
70	250.1 µW	0.852 ns
80	251.4 µW	0.853 ns
90	252.7 µW	0.856 ns
100	254.0 µW	0.857 ns

Table 2: *Comparison of the proposed comparator with prior differential comparator*

Parameters	**Comparator [6]**	**Proposed Comparator**
Avg. Power Dissipation	697 µW	269.9 µW
Propagation Delay	0.95 ns	0.87 ns
Technology	180 nm	180 nm
Supply Voltage	1.8 V	1.8 V
Maximum Operating Clock Frequency	500 MHz	1 GHz
Input Difference	0.1 µA	0.1 µA
Minimum Input Sensitivity	+/-8 nA	+/- 4 nA

The performance of the comparator influences the performance of Analog-to-Digital Converter (ADC). Thus to obtain a high speed high resolution ADC, the proposed comparator fits well with these requirements. Fig. 9 shows the simulated output of the proposed current comparator on implementation in a 1 GSPS 3-bit ADC. A current mode input to a Flash ADC employing the proposed comparator yield the thermometer code. The 7-bit thermometer code obtained from the comparator block is feed into the encoder for 3-bit binary conversion. A 7-to-3 MUX based TM2B encoder is used. The delay for calculated is 1.671 ns and the overall average power dissipation of the ADC is 2.224 mW.

CONCLUSION

In this paper, a differential current comparator operating at 1 GHz clock speed is capable of detecting very low current difference (as low as 4 nA)with enhanced speed and low power dissipation on the basis of simulated results. For current to voltage conversion a modified Wilson's current mirror topology is presented, the outputs from it are feed to a preamplifier for kickback noise protection followed by dynamic latch which is the ultimate comparison stage. This is followed by a series of inverters to get hold of a full rail-to-rail swing at the output. A working example of the comparator in 1 GSPS 3-bit resolution ADC is presented for performance overview. The comparator power-delay product is within reasonable range. Circuits like current steering DACs and high resolution ADCs can use this comparator especially since performance of the current comparison influences the overall performance

REFERENCES

1. Surachel Khucharoensin and Varakorn Kasemsuwan, "High-speed Low Input

Impedance CMOS Current Comparator" , IEEE, 2003.
2. Lin, Hongchin and Huang, Jie-Hau and Wong, Shyh-Chyi, “A simple high-speed low current comparator,” in International Symposium on Circuits and Systems, ISCAS, The IEEE Proceedings, Geneva, 2000, pp. 713–716.
3. B. M. Min and S. W. Kim, “High performance CMOS current comparator using resistive feedback network,” Electronics Left., vol. 34, no. 22, pp. 2074-2076, 1998.
4. Palmisano, Giuseppe and Palumbo, Gaetano, “High performance CMOS current comparator design,” IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 43, no. 12, pp. 785–790, 1996.
5. Banks, DJ and Degenaar, P and Toumazou, C, “Distributed current-mode image processing filters,” Electronics Letters, IET, vol. 41, no. 22, pp.1201–1202, 2005.
6. Santanu Sarkar, Swapna Banerjee, "500 MHz Differential Latched Current Comparator for Calibration of Current Steering DAC",IEEE Student's Technology Symposium, 2014.
7. B.Razavi "Design of Analog and Integrated Circuits",Tata McGraw Hill Edition 2007.

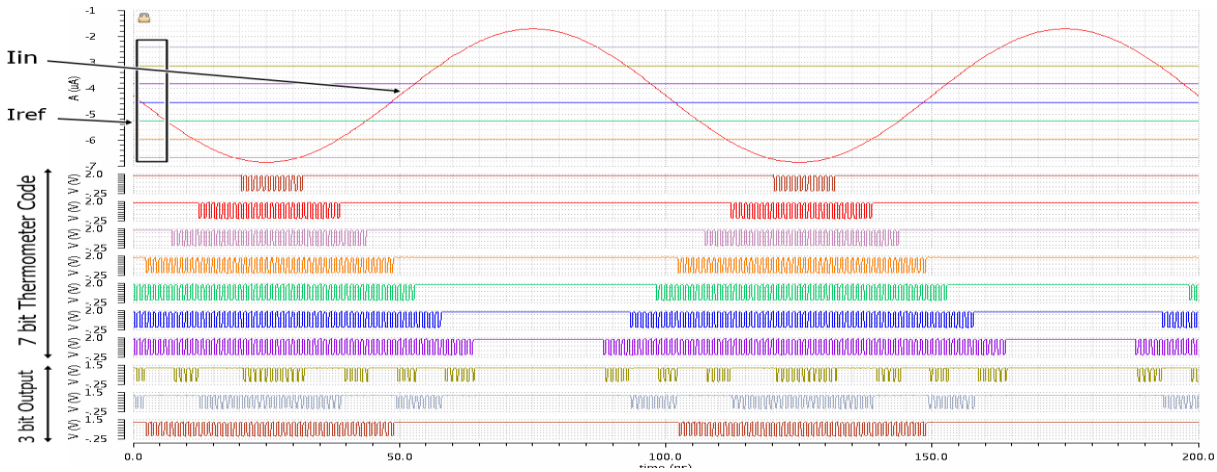

Fig.9. *Simulated input and out waveform of 1 GSPS 3-bit ADC employing the proposed comparator*