Total-Ionizing-Dose Effects on 3D Sequentially Integrated, Fully Depleted Silicon-on-Insulator MOSFETs

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***Abstract*— Effects of additional thermal budget associated with a three-dimensional (3D) fabrication sequence are evaluated for the total-ionizing dose radiation response of fully depleted silicon-on-insulator (FD-SOI) MOSFETs. Current-voltage and low-frequency (1/*f*) noise measurements are compared for (1) conventional planar FD-SOI MOSFETs, and (2) MOSFETs formed in the bottom layer of the 3D process and subjected to the process steps associated with formation of a second active layer. Similar radiation-induced voltage shifts and increases of 1/*f* noise are observed after irradiation for both types of structures. These similar changes in response show that the additional thermal processing involved with 3D fabrication has little effect on border-trap densities and radiation-induced charge trapping in gate and/or buried oxides of MOSFETs formed in the bottom layer of the 3D process.**

***Index Terms*— 3D integration, fully depleted (FD), silicon-on insulator (SOI), irradiation, total ionizing dose (TID), low-frequency noise.**

I. Introduction

3D SEQUENTIAL integration (3DSI) enables an active device to be stacked on another device in a sequential way to extend the capabilities of traditional planar technology [1]–[3]. Its high alignment accuracy depends primarily on precision lithography and stepper performance, making it possible to fabricate stacked fully-depleted silicon-on-insulator (FD-SOI) structures. However, this integration comes at the cost of additional thermal budget for the top layer processing [1], [2], which can potentially affect the device radiation response [4], [5]. In particular, furnace annealing above ~875 °C after gate oxidation and poly-crystalline silicon deposition can greatly increase the density of radiation-induced oxide-trap charge [6] and low-frequency noise of as-processed [7] and irradiated MOS devices due to enhanced O vacancy formation in SiO_2 [8]–[10].

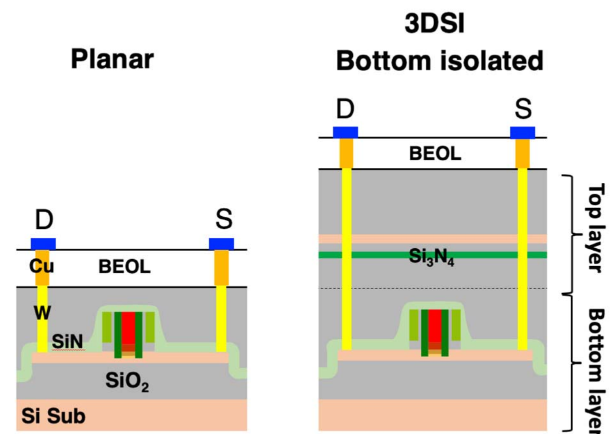

Fig. 1. Experimental structures of planar FD-SOI and bottom-isolated 3D integrated FD-SOI transistors. The dimensions of the devices are $W/L =$ 10 μm/80-1000 nm. The gate dielectric is 1 nm SiO_2/2 nm HfSiON. Bottom-isolated devices were fabricated through the 3D sequential process described above, except the process of a top transistor patterning is skipped. The BEOL structure is simplified for all devices.

In this letter, we evaluate whether the additional process steps required to fabricate the upper-layer transistor affects the radiation response of already-built transistors in the bottom layers of 3DSI FD-SOI MOSFETs. We compare measurements of total-ionizing-dose (TID) response and $1/f$ noise for conventional planar FD-SOI MOSFETs and bottom-isolated devices, shown schematically in Fig. 1. Similar front-gate threshold-voltage shifts and increases in low-frequency noise are observed for both types of devices. These results strongly suggest that the additional processing steps required to achieve 3D integration have little effect on the resulting charge trapping and border-trap densities in the gate and/or buried oxides of these devices.

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II. Experimental Details

A. Sample Fabrication

Devices were fabricated at CEA, LETI [3] on 300 mm SOI wafers (t_{BOX} = 145 nm) [1], [2]. The SOI layer of both types was undoped and thinned to t_{Si} = 7 nm. High temperature process steps include a 1 nm SiO_2/2 nm HfSiON gate dielectric fabricated at temperatures up to 950 °C, followed by deposition of 4 nm of TiN and 50 nm of poly-crystalline Si. Raised drains and sources are formed, followed by spike annealing at 1050 °C. Additional process details are provided in [1], [2].

B. Irradiation

Planar devices and 3D-integrated devices were fabricated on different wafers processed in the same run. All devices were irradiated at room temperature by using an ARACOR Model 4100 Irradiator at a dose rate of ~525 rad(SiO_2)/s using stepped doses up to 1 Mrad(SiO_2). During irradiation, the top gate voltage is V_g = 1.0 V; all other terminals are grounded. All measurements were performed in-source, so that the full irradiation and measurement sequence was completed in less than 1.0 h. After irradiation, all devices were annealed at room temperature to check for potential post-irradiation interface-trap charge buildup and evaluate the potential recovery rate of oxide-trap charge [4]. Drain-current vs. top-gate voltage $I_d - V_g$ characteristics were measured with a HP4156A parameter analyzer with drain voltage V_d = 0.1 V. V_{th} is defined here as the gate-voltage axis intercept of the linear extrapolation of the $I_d - V_g$ curve at the point of maximum first derivative. More than 5 devices of each type were evaluated for this study; representative results are shown.

C. 1/f Noise Measurements

Low-frequency noise measurements were performed on the top-gate transistors for each type of device. Measurements were performed at room temperature as a function of gate overdrive voltage, $V_{gt} = V_g - V_{th}$, with V_d = 0.1 V [6], [10]. The gate-voltage and frequency-dependence of the noise are parameterized via an expression of the form [10], [11]:

$$S_{Vd}\left(f, V_d, V_g\right) = \frac{K}{f^{\alpha}} \frac{V_d^2}{(V_g - V_{th})^{\beta}}. \quad (1)$$

S_{Vd} is the excess voltage-noise power spectral density and K is a constant. Noise due to carrier number fluctuations with constant spatial and energy distributions of border traps lead to $\alpha = 1$ and $\beta = 2$ [10], [11]; deviations from these dependences are typically due to non-uniform effective defect-energy distributions [6], [10], [12]. Values of α were 1.0 ± 0.2 over the range of all devices measured before and after irradiation. Values of β often changed with irradiation, as shown below. Effective densities of border traps per unit area and energy at Fermi level $D_{bt}(E_f)$ at the top-gate/dielectric interface can be estimated, to first order, via [10], [13].

$$D_{bt}\left(E_f\right) = \frac{C_{ox}^2 \cdot (V_g - V_{th})^2 \cdot LW \cdot \ln(\tau_1/\tau_0) \cdot f \cdot S_{Vd}}{q^2 V_d^2 k_B T}. \quad (2)$$

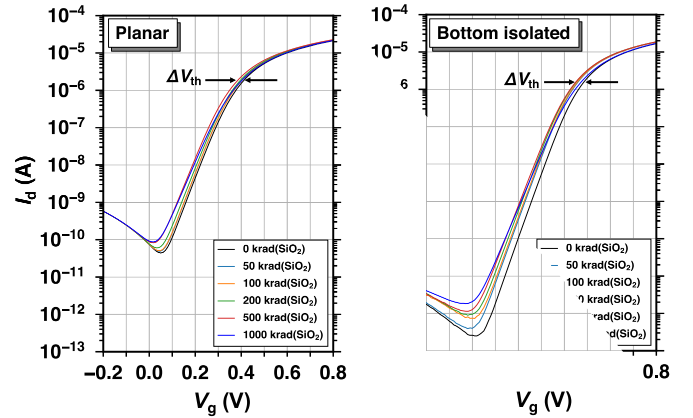

Fig. 2. Drain current I_d vs. V_g characteristics of planar (left) and bottom-isolated (right) transistors. W/L = 10 μm/10 μm for each device. Devices were irradiated with V_g = 1.0 V and other terminals grounded. The differences in pre-irradiation off-state leakage current in this figure are due to device-to-device variations. No systematic trends in off-state leakage were observed for the planar and bottom-isolated devices.

Here q is the elementary charge, C_{ox} is the gate oxide capacitance per unit area, L and W are channel length and width, k_B is the Boltzmann constant, T is the temperature and τ_1 and τ_0 are maximum and minimum tunneling times [13].

III. Results and Discussion

A. TID Response

Fig. 2 shows $I_d - V_g$ characteristics of planar and bottom-isolated FD-SOI transistors with channel dimensions of W/L = 10 μm/10 μm. To facilitate the comparison of the radiation responses of these devices, front-gate threshold voltage shifts ΔV_{th}, midgap voltage shifts ΔV_{mg}, and subthreshold stretchout $\Delta V_{so} = \Delta V_{th} - \Delta V_{mg}$ are shown in Fig. 3. Values of V_{mg} and V_{so} for the front-gate transistor characteristics are estimated, to first order, using the method of McWhorter and Winokur [17]. A negative shift in V_{th} is observed, due primarily to the electrostatic effects of hole trapping in the buried oxide on the front-gate transistor characteristics [5], [15], [16], [18]–[23], although some contributions from charge trapping in the high-K gate dielectric are also likely [24], [25]. The increase in subthreshold stretchout occurs primarily due to the combination of (1) radiation-induced interface traps at the front and back interfaces of the fully-depleted Si channel, (2) variations in electric field strength, direction, and/or degree of electrostatic coupling in different regions of dielectrics under gate control [4], [5], [16], [18]–[23], and (3) non-uniform charge trapping in the buried oxide layers [4], [5], [26].

Similar radiation-induced voltage shifts in Figs. 2 and 3 are observed in the planar and bottom-isolated devices. This similarity in response likely occurs because (1) the time at temperatures above ~875 °C is sufficiently short that significantly higher densities of O vacancies are not formed in the gate or buried oxides of either device [8], [27], (2) the Si_3N_4 layer is sufficiently distant that neither charge trapping or hydrogen transport processes often associated with Si_3N_4 (as observed, e.g., when Si_3N_4 is used as a spacer oxide [28]) affects the current-voltage characteristics of the bottom-isolated device,

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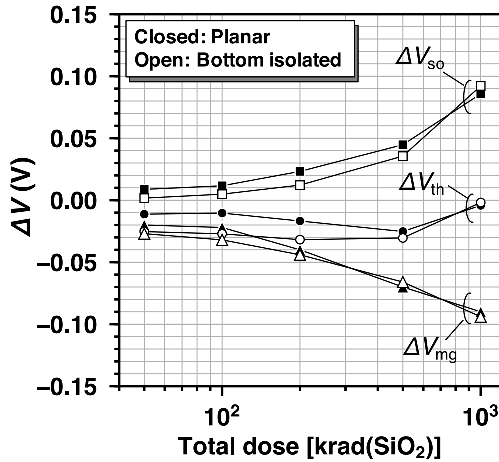

Fig. 3. Top-gate threshold voltage shifts ΔV_{th}, midgap shifts ΔV_{mg}, and subthreshold stretch-out ΔV_{so} for the devices of Fig. 2. Closed symbols represent planar devices, and open symbols denote bottom-isolated devices.

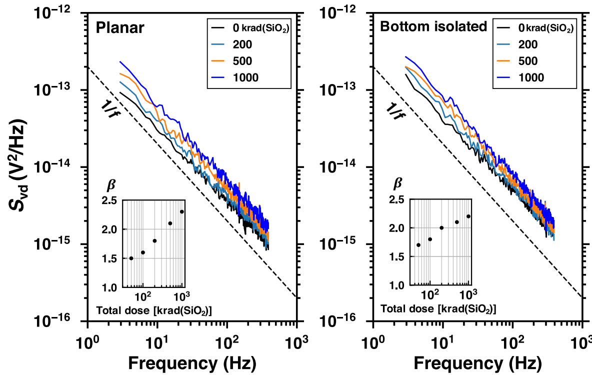

Fig. 4. Low-frequency noise before and after irradiation up to 1 Mrad(SiO_2) at an applied gate voltage of 1 V for the planar (right) and bottom-isolated devices (left) of Figs. 2 and 3. The bias conditions during the noise measurements are $V_d = 0.1$ V and $V_{gt} = 0.3$ V. $W/L = 10$ μm/10 μm. Values of β are shown in the insets at the lower left.

and/or (3) the thick oxide that overlies the bottom-isolated device is neither under gate control nor sufficiently coupled electrostatically [5], [16], [18]–[23] to the active channel to affect the device response.

Fig. 4 shows S_{Vd} as a function of f and V_{gt} before and after devices were irradiated to doses up to 1 Mrad(SiO_2) at an applied gate voltage of 1.0 V. Before and after irradiation, devices show similar noise magnitudes and frequency dependences. This indicates that similar densities of border traps are present in each device type before and after irradiation. Values of β are shown in the insets. As-processed devices of each type exhibit values of $\beta < 2.0$, indicating number-fluctuation noise with a defect density that increases toward the conduction band [6], [10], [12]. Devices irradiated to doses of ~200-500 krad(SiO_2) exhibit values of $\beta \approx 2.0$, indicating an approximately uniform defect density [6], [10], [12]. Devices irradiated to ~1.0 Mrad(SiO_2) exhibit values of $\beta > 2.0$, indicating a defect density that increases toward midgap [6], [10], [12].

Fig. 5 shows the effective density of radiation-induced border traps per unit area and energy at the Fermi level, ΔD_{bt}, based on Eq. (2), for the devices of Fig. 4 [10].

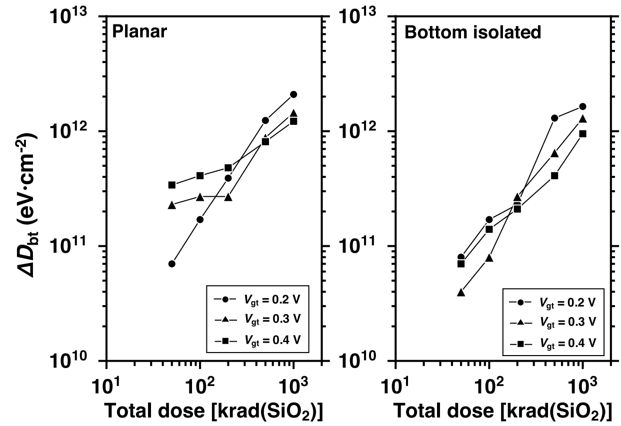

Fig. 5. Changes in effective border trap densities ΔD_{bt} for the devices of Fig. 4, calculated from Eq. (2), as a function of dose and $V_{gt} = V_g - V_{th}$. Initial, effective border trap densities before irradiation are $(1.6 \pm 0.2) \times 10^{12}$ cm^{-2}eV^{-1} and $(1.2 \pm 0.2) \times 10^{12}$ cm^{-2}eV^{-1} for planar and bottom-isolated devices, respectively.

These first-order estimates include electrostatic effects of trapped charge in the buried oxide on border traps near the top channel/gate dielectric interface, but neglect the potential effects of border traps near the buried oxide/back-channel interface. The measured noise, of course, includes the effects of defects at both interfaces. That similar noise magnitudes are measured before and after irradiation for both types of devices demonstrates that the additional thermal budget does not significantly affect pre- or post-irradiation densities of border traps in these devices.

Estimates of initial, effective border trap densities before irradiation are $(1.6 \pm 0.2) \times 10^{12}$ cm^{-2}eV^{-1} and $(1.2 \pm 0.2) \times 10^{12}$ cm^{-2}eV^{-1} for planar and bottom-isolated devices in Fig. 5, respectively. Effective border-trap densities in each type of device are approximately doubled by irradiation to 1 Mrad(SiO_2). These estimates of effective defect densities are similar to those obtained in previous studies of similar high-K gate stacks [10], [29]–[32], reinforcing the plausibility of the underlying assumptions in the first order estimates of ΔD_{bt}.

IV. Summary and Conclusion

Total-ionizing-dose and low-frequency noise measurements strongly suggest that similar oxide and border-trap densities are observed before and after irradiation in the gate and buried oxides of the devices studied in this work. Effective border-trap densities increase with irradiation similarly for each device type, with densities increasing towards the conduction band before irradiation and increasing toward midgap after irradiation to 1.0 Mrad(SiO_2). The similarities in front-gate threshold-voltage shifts and in the observed increases in low-frequency noise for the two types of devices strongly suggest that the additional processing step required to stack transistors in a 3D processing technology does not significantly affect pre- or post-irradiation densities of oxide, interface, or border traps in gate and/or buried oxides of these devices. These results are quite promising for the future development of highly-integrated, 3D technologies for space applications.

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