Design of a Low Noise Amplifier with Integrated Antenna for 60 GHz Wireless Communications

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Abstract—The integration of a Low Noise Amplifier (LNA) with on-chip antenna for 60 GHz short-range wireless applications is discussed in the paper. A 65 nm CMOS Silicon-on-Insulator (SOI) technology has been selected as target. With respect to the state of the art, the on-chip co-design of LNA and antenna permits avoiding a pre-defined constraint of 50 Ohm impedance matching. By relaxing the impedance matching specification a LNA with only two amplification stages has been designed to reach the desired power gain (>20 dB) and noise figure (<5 dB) with a power consumption and circuit complexity optimized vs. state-of-art LNAs with similar performances. A dipole antenna with coplanar strip feed has been also designed matching the 20 Ohm input LNA impedance and allowing an extra gain of 3 dB at 60 GHz with a limited on-chip area occupation.

Index Terms—LNA (low-noise amplifier), 60-GHz, CMOS Silicon On Insulator (SOI), On-chip antenna, Wireless Gbits/s

I. INTRODUCTION

The unlicensed multi-GHz band allocated world-wide around 60 GHz [1-5] will enable new wideband and interoperable communication services among consumer electronics, personal computing and mobile devices [24-30]: wireless fast internet access at several Gbits/s, uncompressed video communication, wireless USB connections, wireless video area networks. To this end the Federal Communications Commission (FCC) allocated a 7-GHz band in the radio frequency spectrum between 57 and 64 GHz [6]. Other countries worldwide have allocated the 60-GHz band for unlicensed wireless communications (Australia [7], Korea [8], Europe [9]), allowing a universal compatibility for the system operating in a band of 3 GHz. To exploit the potentiality of 60 GHz wireless communications the WirelessHD [3,4,11] consortium, based on the IEEE 802.15.3c standard for multi-gigabit WPAN, or the WiGig alliance [1,2], starting from the IEEE 802.11ad standardization effort, have been created.

Recent advances in silicon technologies offer the possibility of integrating into a single-chip a complete transceiver operating at millimeter-waves [10]. CMOS transceivers for 60 GHz applications have been recently proposed in literature [10-13]: in these cases the electronics is entirely realized in a single chip, whereas a 50 Ohm external antenna is utilized. This fact introduces a constraint in the design of Low Noise Amplifier (LNA) which has to be optimized for a 50 Ohm source impedance. However at 60 GHz there is the possibility of integrating on-chip the antenna thus further reducing the system size. When using the on-chip antenna some constraints of the LNA design, e.g. 50-Ohm input impedance, can be removed. The design space exploration becomes a key issue to find if new LNA architectures, vs. the state of the art, can be used allowing a better trade-off between different performance metrics such as power gain, noise figure, power consumption and circuit complexity. At state of the art LNA circuits with a gain around 20 dB and a NF below 10 dB are typically proposed [11,14].

To overcome the limits of the state of the art this work presents the design of a LNA plus on-chip integrated antenna in 65-nm CMOS SOI technology from STMicroelectronics.

The SOI CMOS technology shows very attractive performance for the millimeter-wave system-on-chip design, since the high active performance of MOS transistors are combined with the high-resistivity (HR) of the SOI substrate. Indeed, the feature that the circuit elements are isolated dielectrically allows the SOI technology to significantly reduce junction capacitances and the circuits to operate at high speed or substantially with lower power at the same speed. Moreover, the device structure also eliminates the latch-up in bulk CMOS and
improves the short channel effect immunity. As regard passive structures, the feasibility of transmission lines and antennas in SOI CMOS technology have been reported in [15,16]. The performance of antennas designed in SOI CMOS process is better than the same on standard CMOS process due to a reduced amount of energy stored in the supporting substrate.

Hence the CMOS SOI is a promising alternative in consumer markets vs. SiGe BICMOS and III-V HBT/HEMT technologies.

The rest of the paper is organized as follows. Section II presents the design and characterization by simulations of a new LNA architecture implemented in 65 nm CMOS SOI. The design of a dipole antenna with coplanar strip feed, integrated in the CMOS SOI 65-nm technology and matched with the proposed LNA, is discussed in Section III. Conclusions are drawn in Section IV.

II. LNA DESIGN IN 65 NM CMOS SOI

In this section the design of a LNA for the 60-GHz band is presented, the design choices and the simulation results at schematic level are discussed and compared to the state of the art. The LNA, whose schematic is reported in Fig. 1, has been designed to reach the maximum in terms of power gain and noise figure without taking into account the input and output matching as pre-defined constraints. This approach is possible due to the fact that at 60 GHz the antenna and the subsequent mixer can be integrated in the same chip. While 60 GHz mixer circuits have been already proposed in literature the design of on-chip integrated antenna is still an open issue and will be discussed in Section III.

By relaxing the input/output matching specifications a LNA with only two amplification stages has been designed to reach the desired power gain and noise figure with a power consumption and circuit complexity minimized vs. a reference 60 GHz three-stage LNA architecture we proposed in [14] and whose schematic is reported in Fig. 2.

To do this, the LNA has been implemented by considering the typical approach of millimeter-wave design. In detail, fixed the MOSFET current density close to 0.15 mA/μm [17,18] (for both stages), the equi-GA and equi-noise circles have been used to reach a compromise between the power available gain (GA) and the minimum noise figure. The LNA in Fig. 1 is composed by: i) a single-ended cascode stage, ii) a fully differential cascode stage, modified vs. conventional solutions in order to remove the staked transistor (common-source and common-gate) and thus reducing the problems due to low supply voltage in scaled technologies (1.2V of supply voltage in 65-nm CMOS technology). The full schematic of the two-stage LNA is shown in Fig. 1.

More in detail the first stage has been implemented in accordance with the power-constrained integrated input matching technique and with a MOSFET current density close to 0.15 mA/μm according to the latest advances in LNA design for the best noise figure [17,18]. The first stage provides a proper differential output signal to the fully differential second stage of amplification through an integrated interstage transformer that provides, in addition, the maximum power delivery from the first to the second stage of the LNA [19]. The transformer, see Fig. 3, consists of two octagonal and symmetrical coupled planar inductors, both with 24 μm of diameter, one turns each, 3 μm spaced and 6 μm wide. The primary spiral exhibits a self-inductance (L_TP) of 183 pH with an associated quality factor (Q_TP) [20] equal to 15.53, whereas the secondary spiral exhibits the same self-inductance (L_TS = 147 pH) with a Q_TS equal approximately to 30.04, at 60 GHz.

The second stage in Fig. 1 is a fully differential cascode, that allows the increase of the power gain and the benefits of the common mode rejection ratio (CMRR), converted into a common-source and common-gate stages (as shown in the Fig. 1) in order to have only two staked transistors between
V_DD and GND. In Fig. 4 the equi-G_A and equi-noise circles at 60 GHz for the first and the second stage of the LNA are shown. In particular an input (Z_IN) and output (Z_OUT) impedances of 20 Ω and (57.5+j358.5) Ω respectively, have been considered.

The circuit exhibits a power gain of 22.73 dB and noise figure of 4.86 dB at 60GHz as shown in Fig. 5. As for the linearity and the stability, the Stern’s factor (K) is always greater than 4. The total power consumption is equal to 26.64 mW with a 1.2-V supply voltage.

Compared to the 50-ohm input matched three-stage LNA architecture, realized in the same SOI technology, that we presented in [14] the proposed two-stage LNA circuit, thanks to a released constraint on the input matching, allows us to reach the same performance in [14] with a reduction of 25% of the power consumption and 32% of reduced chip area occupied by integrated inductors. Table I compares the performance of the proposed LNA in terms of Gain (dB), NF (dB), power consumption (mW) and working frequency vs. several LNA proposed in recent literature [14,21] operating at 60 GHz. With respect to the state of art the proposed 2-stage LNA offers the best trade-off between power gain, higher than 20 dB, noise figure, below 5 dB, and power consumption, below 30 mW.

![Fig. 4. Equi-G_A and equi-noise circles for the 60-GHz two-stage LNA](image)

![Fig. 5. Simulation results of the 60-GHz LNA: power gain and noise figure.](image)

### Table I
Comparison with state-of-art 60 GHz LNAs in 65 nm CMOS

<table>
<thead>
<tr>
<th>Process (CMOS)</th>
<th>Topology</th>
<th>Gain [dB]</th>
<th>NF [dB]</th>
<th>Power [mW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Our LNA</td>
<td>2-stage diff. cascode</td>
<td>22.8</td>
<td>4.86</td>
<td>26.64</td>
</tr>
<tr>
<td>[14] 65 nm SOI</td>
<td>3-stage diff. cascode</td>
<td>23.2</td>
<td>4.04</td>
<td>34.9</td>
</tr>
<tr>
<td>[21] 65 nm SOI</td>
<td>3-stage cascode</td>
<td>20.5</td>
<td>6.5</td>
<td>20</td>
</tr>
<tr>
<td>[22] 65 nm SOI</td>
<td>2-stage common source</td>
<td>12</td>
<td>8</td>
<td>36</td>
</tr>
<tr>
<td>[23] 65 nm</td>
<td>2 cascode = 1 common source</td>
<td>22.3</td>
<td>6.1</td>
<td>35</td>
</tr>
</tbody>
</table>

### III. ON-CHIP INTEGRATED CPS DIPOLE ANTENNA

The CMOS SOI technology is a good candidate to design the on-chip antennas for the 60-GHz application. In HR SOI substrates the losses are drastically reduced if compared to the bulk silicon technology, consequently, more energy will be provided to the antenna to radiate. The design presented herein makes use of M_{32} metal layers for the radiating structure and feeding line.

At the 60 GHz operating frequency the antenna reactance (\text{Im}(Z_A)) must be null and the real part of intrinsic antenna impedance (\text{Re}(Z_A)) must be matched to the LNA input impedance, that is 20 Ω.

The integrated antenna has been designed taking into account the following guidelines: i) the 65-nm SOI CMOS process by ST-Microelectronics has been used, ii) the 3D-EM design did not consider the pad effects since these parasitic effects will be removed by de-embedding during the measurements, iii) the knowledge of the effective dielectric constants are necessary to determine the resonant frequency.

The antenna we designed (see Fig. 6) is directly fed by a coplanar strip (CPS) input matching network. The 3D polar plot of the antenna gain obtained by means of 3D-EM simulations (HFSS Ansoft) is shown in Fig. 6. In detail, a maximum gain of 3.23 dBi and a return loss (S11) equal to -23.7 dB at 60 GHz, respectively, have been obtained.

In this design, the arm width is carefully selected to reduce the quality factor of resonance and obtain a wider operating bandwidth. A balanced CPS feed line has been selected as input of the dipole antenna, and its length is tuned in order to obtained the wished 20 Ω source impedance matching the LNA input impedance. The final 60 GHz fully integrated dipole antenna is realized with following parameters: dipole’s length = 760 μm (L_D), width = 22.76 μm (W_D) and 1.1 μm gap between the two dipole’s arms. The feeding line’s length is of 300 μm (L_{CPS}). The area occupied by the antenna is below 0.25 mm², which is suited for on chip integration.

The simulated radiation pattern of this antenna is mainly directed toward the SOI substrate, therefore, with a backside metallization the radiation pattern is directed outward the substrate. The distance between radiating arms and the reflector (355 μm ~ \lambda_g/4) is close to the optimal distance to prevent TM mode which reduces radiation efficiency. Finally, the dipole antenna has 68.8% of radiation efficiency, with peak directivity of about 3.
IV. CONCLUSION

The design of a LNA with integrated antenna for 60 GHz short-range wireless applications has been presented in the paper. A 65 nm CMOS Silicon-on-Insulator (SOI) technology has been selected as a promising alternative in consumer markets vs. SiGe BiCMOS and III-V HBT/HEMT technologies; due to its high-resistivity substrate the losses are drastically reduced if compared to the bulk silicon technology and more energy will be provided to the on-chip antenna to radiate. Since LNA and antenna are integrated on-chip the conventional 50 Ohm impedance matching specifications of the state of the art can be relaxed. This way a new two-stage LNA circuit has been designed to reach the desired power gain (>20 dB) and noise figure (< 5 dB) with a power consumption and circuit complexity optimized vs. state-of-art LNAs with similar performances. The LNA input impedance amounts to 20 Ohm. A dipole antenna with coplanar strip feed has been also designed matching the LNA impedance and allowing an antenna gain at 60 GHz of roughly 3 dB with on-chip area occupation below 0.25 mm².

REFERENCES

[3] IEEE 802.15.3c-2009: Wireless medium access control (MAC) and physical layer (PHY) specifications for high rate wireless personal area networks (WPANs), Sept. 2009

Fig. 6. 60-GHz SOI CMOS CPS dipole antenna a) geometrical parameters, b) design on the 3D-EM simulator, c) 3D polar plot