Multi-MGy Total Ionizing Dose Induced MOSFET Variability Effects on Radiation Hardened CMOS Image Sensor Performances

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***Abstract* — MOSFETs variability in irradiated CIS up to 10 MGy(SiO_2) is statistically investigated on about 65000 devices. Different variability sources are identified and the role played by the transistors composing the readout chain is clarified.**

***Index Terms*— ITER, CMOS Image Sensors, CIS, Fixed Pattern Noise, FPN, MOSFET, Total Ionizing Dose, TID, Readout chain, Radiation Effects.**

I. INTRODUCTION

CMOS Image Sensors (CIS) are today the main solid-state image sensor technology and they are widely used for the development of various scientific applications, thanks to their high performances, high integration capabilities and low power consumption [1]. Their demand is increasing in all those applications which require a radiation hardness at Total Ionizing Doses (TID) in the MGy(SiO_2) range, such as the development of critical remote handling systems in ITER fusion reactor, the monitoring and inspection operations in many nuclear facilities i.e. nuclear power plant, nuclear storage waste repository, particles physics and irradiation facilities (e.g. CERN).

Previous works have demonstrated not only that reaching a 10 MGy (1 Grad) radiation hardness with a CIS is feasible [2], [3], but also that a full camera composed of the FUsion for energy Radiation Hard Image sensor (FURHI) [4] and Imaging System (FURHIS) [5] demonstrators can be made radiation hard up to several MGy(SiO_2).

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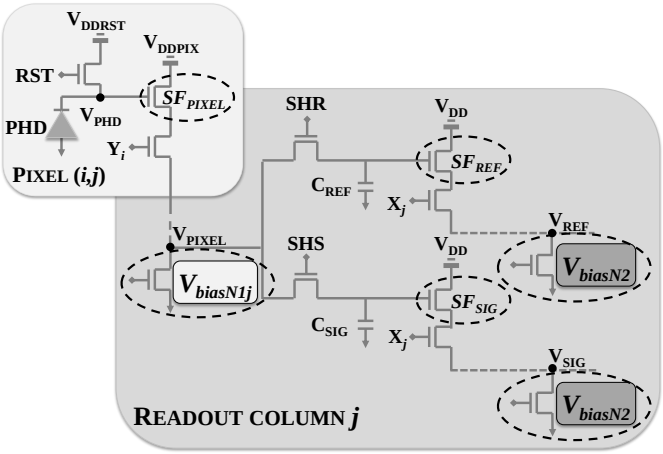

Fig. 1 Schematic of the readout chain in a CIS for the pixel *(i,j)*.

Even significant efforts have been done in the identification of radiation induced degradation mechanisms in CIS there are some aspects that are still to investigate. It is indeed known that the readout chain of a CIS 3.3 V P channel transistors exhibit very high threshold voltage (V_{th}) shift (about 500 mV) at TID beyond 100 kGy because of large gate oxide trapped charge induced V_{th} shifts, whereas 3.3 V N-channel transistors V_{th} is slightly influenced by interface state induced shift [2]. In order to mitigate the P-MOSFETs sensitivity, two different ways of improvement have been proposed: the first, explored in [3] consists in designing a full 1.8V CIS to limit the use of double gate oxides; the second one, which has been selected for the FURHI project, is to base the analog design only on 3.3 V N channel transistors [4]. The FURHI CIS characterization has revealed new imager performance degradation sources due the V_{th} MOSFETs variability. This aspect, addressed in [6] up to TID of 500 Mrad(SiO_2) on few tens structures evidenced that variability in the on-current is enhanced due to the impact of random dopant fluctuations on TID effects. However, beyond this work, very little is known about the TID variability of MOSFETs characteristics in the MGy range.

This work focuses on the non-uniformity and variability on FURHI CIS readout chain MOSFETs to evaluate the TID effects up to 10 MGy(SiO_2) with the aim to:

- Understand the Fixed Pattern Noise (FPN) sources enhanced by irradiation in order to improve the Radiation - Hardening - By - Design (RHBD) CIS techniques.

- Provide a statistical large-scale study (about 65000 devices per studied circuit) to better understand and anticipate the TID induce variability phenomena in MOSFET devices.

II. Studied sensor architecture/Experimental Details

The FURHI CIS was manufactured using a 180 nm CIS process with dedicated photodiode profiles and optimized in pixel devices using a Multi Project Wafer (MPW) access managed by imec-europractice. The MPW was chosen for this project as an indirect way to evaluate the sensitivity of the proposed RHBD techniques on the process variations.

The integrated image sensor itself is constituted of 256x256 pixels with three transistors per pixel. The whole circuit is radiation hardened by design by using Enclosed Layout Transistors (ELT) for all MOSFETs to mitigate Radiation Induced Narrow Channel Effect (RINCE) [7], sidewall leakages and junction leakages. Table I reports a summary of the tested structures and irradiation conditions. Two lots of the same design are studied and for some of the irradiation condition a comparison circuit-to-circuit was addressed in order to investigate the fabrication process variability and reproducibility.

TABLE 1 LIST OF TESTED STRUCTURES AND IRRADIATION CONDITIONS

READOUT CHAIN		**IRRADIATION CONDITION**	**TID (MGy)**
FURHI LOT1	#01 - #03	^{60}Co γ-ray, ON	0.4 – 1
	#02 - #04	^{60}Co γ-ray, OFF	0.4 – 1
	#09	10 keV X-ray, OFF	2 – 5 – 10
FURHI LOT2	#01 - #02	^{60}Co γ-ray, ON	0.1 – 0.5 – 1.1
	#03 - #04	^{60}Co γ-ray, OFF	0.1 – 0.5 – 1.1

γ-ray irradiations were performed at SCK-CEN using a ^{60}Co source; 10 keV X-ray irradiation where done at CEA, DAM-DIF. The ON irradiations are performed maintaining the sensor biased with nominal sequencing signals and continuous frames acquisitions whereas in the OFF irradiation the CIS was fully grounded.

The schematic of the readout chain of the studied CIS is reported in Fig. 1 where the two different stages of the readout process are highlighted. The signal, integrated in the photodiode (PHD), is correctly read if the voltages of the two bias transistors, V_{biasN1} and V_{biasN2}, are well optimized at each TID step. To do so the I-V characteristic of the two transistors is measured and then the optimum bias voltages are chosen in order to perform the measurements at the same current level (i.e. 10 µA for the V_{biasN1} and 200 µA for the V_{biasN2}).

The study on the readout chain degradation was performed thanks to the quasi-static electrical transfer function (ETF) measurements. The output voltage of the readout chain in each pixel as a function of the input voltage applied directly on its sense node (i.e. V_{DDRST} in Fig. 1) was measured by setting the RST and SHR transistors at 3.3 V whereas SHS transistor was grounded (with signal voltage, V_{SIG}, at 100 mV). In this way at the output of the readout chain the reference signal, V_{REF}, was measured.

We obtained:

$$V_{REF(i,j)}=V_{PIXEL\ (i,j)}-V_{GS|SF_{REF}(j)} \quad (1)$$

with

$$V_{PIXEL\ (i,j)}=V_{DD\_RST}-V_{GS|SF_{PIXEL}(i,j)} \quad (2)$$

making the hypothesis that the all switches (i.e. SHS, SHR, Y_i, X_j), RST and PHD contribution are negligible. From equations (1) and (2) it can be seen that the source followers, SF, transistors (see Fig. 1) play an important role in the V_{REF} measurement and that, at first approximation, their V_{th} mismatches can be the responsible of the non-uniformity which manifests itself as Fixed Patter Noise (FPN), i.e. the dark signal non-uniformity arising from electronic sources [8].

III. Effects of transistor-to-transistor mismatches

Fig. 2 shows the raw image captured during the ETF measure at V_{DDRST} = 2.8 V, i.e. hard reset conditions in the linear ETF region, in one of the 1 MGy(SiO_2) FURHI LOT1 irradiated sensor. It can be noted that after irradiation a severe degradation of the images is present, differently affecting the response of each pixel. It is possible also to distinguish two different effects: the first manifest itself as non-uniformity in the whole array affecting the edge of the sensors differently with respect to its center. This pattern, which is present in all circuits, is responsible for pixel non-uniformity, probably due to the metal density differences in the imaging area with respect to the edges of the array. A dark current enhancement in the center of the device in γ-irradiated CIS has been reported in [9], [10] and [11] for different technologies, resulting in a similar CIS non-uniformity than the one observed in the structures investigated here. The second effect that can be recognized from Fig. 2 is a column-to-column non-uniformity which is responsible of the column fixed pattern noise.

Eq. (1) and Eq. (2) show that the recorded output voltage depends on SF transistors and that it is possible to isolate the contribution of SF_{PIXEL} from the one of SF_{REF}. Indeed, looking at the signal along a column of the array allows obtaining the only contribution of SF_{PIXEL} since SF_{REF} is the same for each column. Fig. 3 shows the output signal along a column (black line); it can be seen that the response is parabolic. This shape gives the information of SF_{PIXEL} V_{th} non-uniformity which can be quantified by the amplitude of the signal variation along a column (Δ_1 ~ 90 mV in Fig. 3). The variability of these MOSFETs can be instead obtained taking the average of the standard deviations performed on short intervals (about 10 points) along the column (σ_1 ~ 5 mV in Fig. 3).

On the other hand, the signal along a row of the array is affected by both SF_{PIXEL} and SF_{REF} V_{th} mismatches. Fig. 3 reports the output voltage along a row of the array (grey line). It can be observed again that the non-uniformity has a parabolic shape, but, in this case, both the amplitude (Δ_2 ~ 250 mV) and the variability (σ_2 ~ 22 mV) are higher due to the fact that both SF_{PIXEL} and SF_{REF} MOSFETs contributions are present.

The same analysis was carried out in all the studied FURHI LOT1 samples at each dose (total 3.3×10^5 studied MOSFETs); the results are shown in Fig. 4.

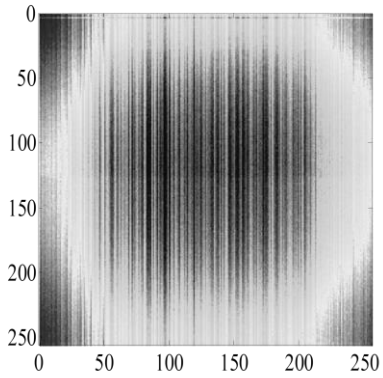

Fig. 2 ETF raw image (represented in logarithmic scale) captured at V_{DDRST}=2.8 V (hard reset condition) after 1 MGy (SiO_2) of irradiation in FURHI LOT1 #02 to show the arisen FPN with irradiation.

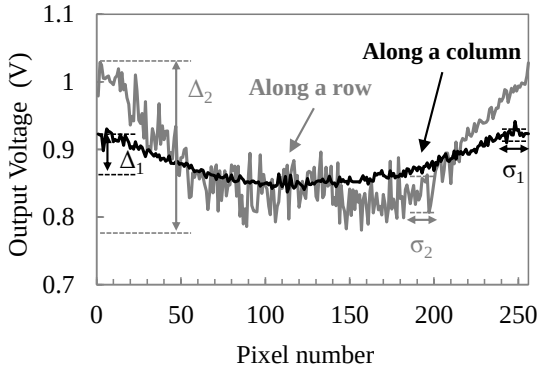

Fig. 3 Output Voltage along a column (black line) and a row (grey line) to show the V_{th} SF_{PIXEL} non-uniformity due to the metal density difference effect. From these curves it was possible to extract the FPN non-uniformity, Δ, and variability, σ.

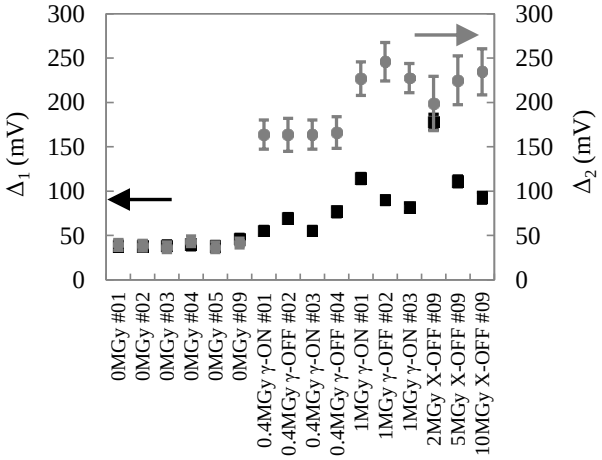

Fig. 4 Evolution of the average FPN amplitude along the columns (Δ_1) and along the rows (Δ_2) in the FURHI LOT1 circuits. The errors bars of each point correspond to the variability, i.e. σ_1 and σ_2.

It can be noted that the both Δ_1 and Δ_2 evolve with the TID without significant circuit-to-circuit variation at each TID step. On the other hand, whereas σ_1 remains almost unchanged in the whole set of samples (the only exception is the sample irradiated at 2 MGy where σ_1 is two times higher than the other samples), σ_2 increases with the TID. Indeed, whereas it is comparable to σ_1 in the non-irradiated circuits (~5 mV) it reaches ~ 30 mV above 1 MGy of irradiation. From these results, and looking at the readout chain schematic in Fig. 1, it is possible to individuate SF_{REF} as the main cause for the observed non-uniformity.

IV. Effect of Lot-to-Lot Variations

A. On the average response

Fig. 6 shows the ETF at the different TID. It can be noticed that the response is similar in both lots. Indeed, the ETF is shifted towards higher input voltages (effect due to the V_{th} shift of V_{biasN1} and V_{biasN2} MOSFETs with irradiation [3] [7]) and the electrical gain decreases with irradiation. At 1 MGy the degradation are lower in FURHI LOT2 being the MOVS stable at about 1.4 V and the electrical gain almost unchanged after 0.1 MGy.

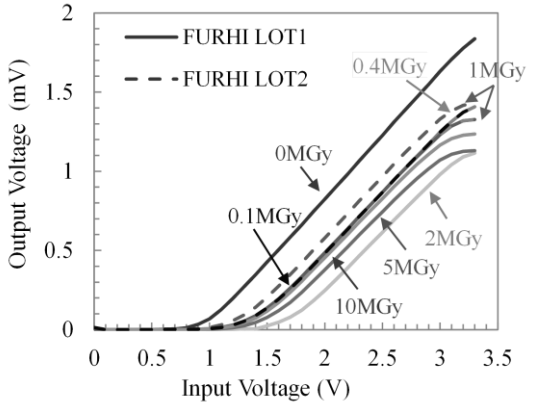

Fig. 5 Comparison of the mean ETF response as a function of the TID between FURHI LOT1 and FURHI LOT2.

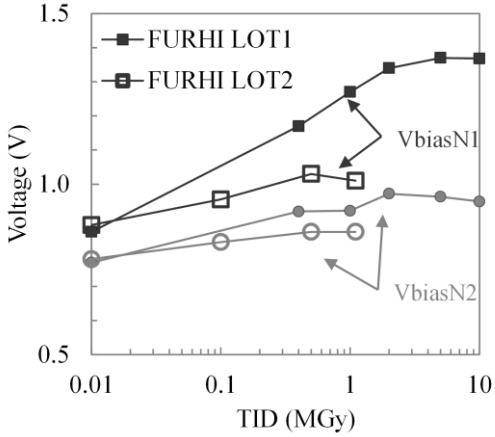

Fig. 6 V_{biasN1} and V_{bisaN2} MOSFET voltages as a function of the TID in FURHI LOT1 and FURHI LOT2.

This effect is more evident from Fig. 7, where the output voltage of V_{biasN1} and V_{biasN2} MOSFETs reported as a function of the TID. It can be observed that the V_{th} of the two transistors are shifted towards higher voltages being the shift higher in FURHI LOT 1 than FURHI LOT 2. At 1 MGy for example the shift of V_{biasN1} is 400 mV in FURHI LOT1 and 130 mV in FURHI LOT2 whereas V_{biasN2} is shifted of 150 mV in FURHI LOT 1 and only 80 mV in FURHI LOT 2 at 1 MGy. The higher degradation of V_{biasN1} is probably due to the fact that its dimensions are lower than V_{biasN2}.

B. On the mismatches induced degradations

The differences on the average performances in the two lots (which derive from the same design) is mostly attributed to a variation in the fabrication process due to the fact that the circuits are fabricated using an MWP. In order to better investigate on this effect a comparison of the non-uniformity and the variability presented in section III is here reported. The FPN comparison between the two lots is reported in Fig. 8 at a TID of about 1 MGy(SiO_2).

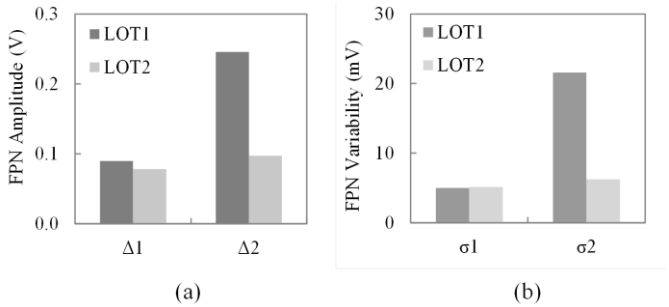

Fig. 7 Comparison of the FPN amplitudes (a) and variability (b) between FURHI LOT1 and FURHI LOT2 irradiated at 1 MGy(SiO_2) and 1.1 MGy(SiO_2) respectively.

As for the average response, it can be observed that FURHI LOT2 is less degraded than FURHI LOT1. Moreover, it seems that in this lot the only contribution to the FPN is due to the pixel-to-pixel non-uniformity, being the amplitudes along the columns and the rows almost the same ($\Delta_1 \sim 80$ mV and $\Delta_2 \sim 100$ mV) whereas $\Delta_2 \sim 3\ \Delta_1$ in FURHI LOT1 (see Fig. 8 (a)). As regards the variability, reported in Fig. 8 (b), it can be seen that it remains of the order of about 5 mV in FURHI LOT2, thus allowing to conclude that SF MOSFET of the column readout chains have not an impact on FPN in this lot, but that the variability sources are more attributed to in-pixel MOSFETs due to the density metal difference of the fabricated design. This result allows concluding that only the column readout MOSFETs have been influenced by the lot-to-lot fabrication process variation. This can be explained taking in account that, in a CIS fabrication process, the doping profile on an in-pixel MOSFET generally differs from the out-pixel ones thus indicating the out-pixel variation manufacturing process as the main cause of the FPN observed in FURHI LOT1.

V. Conclusion

In this work the FPN characterization in irradiated CIS up to 10 MGy(SiO_2) has been reported. The statistical study, performed on about 65000 MOSFETs per circuits (i.e. a total of about 6×10^5 devices), has allowed investigating the different FPN sources, clarifying the different role played by the transistors composing the readout chain. It has been showed that in this design an in-pixel FPN is present and that it is most likely due to the density metal difference between the edge and the center of the array. Even if this contribution is present in both lots with the same effect, it has been showed that its influence does not affect the CIS performances thanks to the differential readout architecture. On the other hand, the degradations in the readout chain leads to severe FPN degradation on one of the studied lot due to the non-pixel transistors. The root cause of this effect has to be searched between SF_{REF}, SF_{SIG} MOSFETs V_{th} mismatches. Moreover, the difference of performances of the two lots with regards to both average and statistical investigated parameters points to fabrication process variability as the cause of the enhanced FPN.

VI. References

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