An Interleaved Totem-Pole Power Factor Correction Converter

Eka FIRMANSYAH*, Satoshi TOMIOKA**, Seiya ABE***, Masahito SHOYAMA*** and Tamotsu NINOMIYA†

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Abstract: This paper explains about basic working principles, implementation problems, and experimental results of a new power factor correction (PFC) topology. In this proposed topology, a totem-pole boost PFC circuit that works under interleaved critical-conduction-mode (CRM) condition is presented. The circuit is developed towards high efficiency, high performance, low-cost, simple control scheme, and low conducted electromagnetic interference (EMI) PFC circuit. The application is targeted toward middle power applications that normally employs continuous or non-bridgeless interleaved boost converter.

Keywords: PFC, Bridgeless, Totem-pole, Boost converter, Critical-conduction-mode, Interleaved

1. Introduction

The critical-conduction-mode (CRM) interleaved boost topology gains widespread acceptance in power factor correction (PFC) application recently. It is because combination of CRM and interleave technique result in a PFC circuit with good characters as; zero current switch (ZCS) turn-off, nearly zero-voltage-switch (ZVS) turn-on, and simple control scheme\(^1\)-\(^4\).

The CRM-interleaved Boost PFC converter solves pulsating input current problem embedded to the CRM-Boost PFC converter. The referred converter input current is nearly as smooth as the infamous continuous-conduction-mode (CCM) boost converter\(^2\)-\(^4\). This quality can be achieved without dealing too much problem with the catch-diode reverse recovery current problem normally found in CCM boost PFC converter\(^3\).

All of those good characters not only result in good efficiency but also have possibility to reduce its conducted EMI signature. Even though the converter needs more components than single CRM-boost PFC converter, but it can be build of two smaller input inductors, reasonable size output capacitor, better thermal management, and less-ideal switches and diodes.

Enhance further the efficiency of the aforementioned converter is a great challenge dictates by stringent energy efficiency requirement in recent days. In this research, it is done by applying a form of bridgeless topology called the totem-pole topology.

2. The Bridgeless PFC

2.1 Basic Principle

Typical circuit of a CRM-interleaved boost PFC is depicted in Fig. 1. It consists of bridge diodes (D\(_{b1} - D_{b4}\)) and two boost converters connected in parallel\(^3\)-\(^4\).

Basic circuit of a bridgeless PFC can be seen in Fig. 2. It also contains two boost converters. In this topology, they are connected in series instead of parallel\(^3\).

Within bridgeless topology, the body-diodes of S\(_1\) and S\(_2\) provide return path to the input voltage similar to D\(_{b2}\) and D\(_{b4}\) in a conventional PFC. With this arrangement, the output voltage of both converters produce similar sign referenced to ground regardless of input voltage polarity.

Compared to conventional PFC, a bridgeless PFC does not need D\(_{b1}\) and D\(_{b3}\) in order to produce rectified output voltage. Exclusion of those diodes reduces conduction loss inside the converter. It gives
higher efficiency for the bridgeless solution compared to the conventional PFC converter\(^5\,\text{--}^7\).

### 2.2 Problems

Circuit in Fig. 2 has larger common-mode conducted noise than conventional boost PFC\(^6\). Therefore, the circuit is impractical to recent strict noise regulation.

Moreover, to implement interleaved function of a bridgeless PFC will need four boost converters; two in series to form a bridgeless PFC and multiplied by two to form interleaved function. It needs four switches, four diodes, and two to four inductors (depend on topology selection). Those are quite numerous numbers of components.

### 2.3 Preferred Topology

An interesting topology called totem-pole dual-boost PFC\(^8\) is presented in Fig. 3. This circuit is less suffer from high common-mode noise problem\(^6\,\text{--}^9\). Moreover, a bridgeless CRM interleaved boost PFC based on this topology, ideally, needs fewer components compared to the one based on the circuit in Fig. 2\(^7\).

It is stated that the referred circuit is only suitable for DCM (discontinuous conduction mode) and CRM operation. That is because in this topology, MOSFET's body-diode is used as boost converter catch diode. Normally, body-diode of a MOSFET has long reverse recovery time. It makes them unsuitable to operate under CCM condition\(^6\,\text{--}^9\).

Fortunately, the limitation does not upset this research. Because, the basic circuit of CRM-interleaved topology also works under critical conduction condition. With the advantage of less components are required in implementing interleave function, this topology becomes a good candidate to be the basic topology.

### 3. The Proposed Topology

#### 3.1 Building Block

Figure 4 shows schematic diagram of the proposed converter. It is basically similar to the circuit of Fig. 3. Additional inductor \(L_2\) and extra switch-leg \((S_3\text{ and }S_4)\) are required to implement interleave function. In this topology, \(D_1\) and \(D_2\) provide return path just like \(D_{b2}\) and \(D_{b4}\) of Fig. 1. Those diodes should be of normal line-speed rated\(^6\,\text{--}^9\).

Switches on the Fig. 4 can be grouped into positive-phase group \((S_2\text{ and }S_4)\) and negative-phase group \((S_3\text{ and }S_1)\). The positive-phase group operates as boost-switches during positive phase \(V_i\). During this period, body-diodes of the negative-phase group act as the catch diode. In this phase, return current is delivered by \(D_2\). The converter operation during this stage is illustrated by Fig. 5(a).

When \(V_i\) is in its negative phase, the opposite condition occurs. Through out this time, negative-phase group operates as the boost switches and the positive-phase group body diodes work as the catch diode. Return current is handled by \(D_1\). Figure 5(b) depicts this condition.

#### 3.2 Control Scheme

Figure 6 shows the control block diagram for the proposed converter. Its main part is similar to a conventional CRM-interleaved boost PFC. Therefore, commercially available controller for that con-
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The controller of a CRM-interleaved boost PFC needs only to monitor $V_L$ and the zero-current crossing instant time to fulfill its basic control function. In order to minimize conduction loss and component cost, the zero-current crossing detectors normally do not incorporate resistor sensing technique nor current transformer. Instead, they are normally implemented as secondary winding of the boost inductor\(^{10}\).

Some adaptations should be made in order to accommodate the bridgeless nature of the proposed converter. A phase detector to monitor $v_i$ is essential for the controller.

The phase detection signal is then used to direct PWM signal to appropriate switches. When positive phase is detected, PWM signal will be directed to positive-phase group ($S_2$ and $S_4$) otherwise it will be sent to negative-phase group ($S_1$ and $S_3$).

Moreover, this signal is also needed to direct zero-current crossing signal to its detector. This modification is to accommodate a fact that the converter input inductors are now located in the ac side. It makes the zero-current crossing signals alternate their phase each time $V_i$ changes its polarity. As the main controller needs certain logic condition in determining the beginning of the next switching cycle, the detector windings are now modified to be center-tapped windings with some additional components as shown in Fig. 7. The modified circuits need signal from the phase detector in order to operate properly.

4. Practical Problems

4.1 Reverse Recovery Current of Body Diodes

The proposed converter utilizes MOSFET’s body diodes to be used as its catch diodes. It should be noted that body diode characteristics are not as good as a well-designed diode. This body diode is actually side effect intrinsic to the MOSFET structure.

This results in condition as depicted in Fig. 8. It is shown in Fig. 8(a) that conventional CRM-interleaved boost PFC, which employs fast-recovery
diodes, generates negligible negative current in its input inductor. However, Fig. 8(b) shows that significant negative current can be seen in the proposed converter as it uses MOSFET’s body diode for its catch diode. The negative current is a consequence for higher recovery charge resides inside the body diodes. It is common for a MOSFET’s body diode to have ten times more recovery charge compared to a dedicated fast recovery diode. This situation gives quite significant penalty towards converter efficiency as described in Fig. 9.

4.2 Voltage and Current Ringing Near Zero-Crossing of $V_i$

Every time $V_i$ crossing the zero point toward a new phase, the proposed converter enters an idle condition. Its waveforms during idle and some period after that is shown in Fig. 10. The parasitic capacitance condition during(-) to (+) phase transition is shown in Fig. 11 with:

- $C_{S_n}$ is parasitic capacitance of $S_n$; $n=1,2,3,4$
- $C_{D_i}$ is parasitic capacitance of $D_i$; $i=1,2$
- $C_{B_j}$ is parasitic capacitance of the switch legs; $j=1,2,3$

Careful attention should be made on those parasitic capacitances. With condition as stated in Fig. 11, $C_{D2}$ will be discharged through $L_i$ and $V_i$ on the first PWM signal. Here, discharging process occurs under resonant condition of $L_i$ and all other parasitics capacitances.

It should be noted that at this moment, $V_i$ is still very small and is in phase to the charge stored inside $C_{D1}$. This creates current pulse and excites quite disturbing voltage and current oscillation as shown in Fig. 10.

The oscillation occurs in two different areas:

Fig. 8 Effect of the catch-diode type to $I_L$ waveform in a CRM-interleaved boost PFC.

![Graph showing effect of catch-diode type on $I_L$ waveform in CRM-interleaved boost PFC.]

Fig. 9 Efficiency of the CRM-interleaved boost PFC with fast reverse recovery diodes compared to one with slow reverse recovery diodes.

![Graph showing efficiency comparison of CRM-interleaved boost PFC with different reverse recovery diodes.]

Fig. 10 The proposed topology key-waveforms during phase transition.

![Waveforms showing key transitions during phase transition in the proposed topology.]
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Fig. 11 Parasitic capacitances in the proposed circuit during $V_i$ phase transition from - to +.

Parasitic capacitances in the proposed circuit during $V_i$ phase transition from - to +.

Fig. 12 Efficiency of the proposed topology compared to the CRM-interleaved PFC.

- $L_i$, $C_{Sn}$, and $C_{Di}$ generate oscillation referenced to neutral point,
- $L_i$ and $C_{Bj}$ generate oscillation referenced to earth.

The oscillating voltage and currents result in several problems like:
- The phase detector circuit generates wrong phase detection signal. This condition may result in catastrophic event.
- Oscillation occurs among $L_i$, $C_{Sn}$, and $C_{Di}$ increase differential-mode conduction noise.
- Oscillation between $L_i$ and $C_{Bj}$ increase common-mode conduction noise.

Therefore, voltage and current ringing near zero crossing point of $V_i$ should be addressed properly in order to achieve good performance of the proposed converter.

5. Experimental Result

Three converters have been built; a prototype of the proposed converter (proposed), a CRM-interleaved PFC with ultra-fast catch diodes (conv. 1), and a CRM-interleaved PFC with body-diode of the MOSFET act as the catch diodes (conv. 2).

Specifications of the converters can be seen in Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Proposed</th>
<th>Conv. 1</th>
<th>Conv. 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_o$</td>
<td>300 W</td>
<td>300 W</td>
<td>300 W</td>
</tr>
<tr>
<td>FET</td>
<td>SPP11N60</td>
<td>SPP11N60</td>
<td>SPP11N60</td>
</tr>
<tr>
<td>Diode</td>
<td>MA2DF60</td>
<td>MA2DF60</td>
<td>Body-diode</td>
</tr>
<tr>
<td>$L_i$</td>
<td>500 u</td>
<td>500 u</td>
<td>500 u</td>
</tr>
<tr>
<td>$C_o$</td>
<td>200 u</td>
<td>200 u</td>
<td>200 u</td>
</tr>
<tr>
<td>$V_o$</td>
<td>360 u</td>
<td>360 u</td>
<td>360 u</td>
</tr>
</tbody>
</table>

Efficiency comparison among those three converters can be seen in Fig. 12. As the catch-diode factor significantly affect the efficiency of the converter as shown in Fig. 9, fair efficiency comparison will be among the proposed converter to the CRM-interleaved boost PFC with MOSFET body diodes as the catch diode.

The efficiency figure shows that performance of the proposed converter is better than the CRM-interleaved PFC with MOSFET body-diode act as the catch diode. This confirm the theory stated that
the bridgeless topology should be able to improve efficiency of a PFC converter by eliminating one series element of semiconductor from the circuit\(^5\),\(^6\),\(^8\),\(^9\).

The harmonic content of the proposed converter can be seen in Fig. 13. It can be seen in the figure that the proposed converter generates quite significant amount of third harmonic. This is caused by apparent cusp distortion around input voltage zero crossing. However, this condition is still considered save for IEC31000-3-2 class D equipment.

Figure 14 describe about current condition inside \(i_{L1}\) and \(i_{i}\). It is clear that even though \(i_{L1}\) contains fast change current signal, it becomes smoother while combined with the \(i_{L2}\) and results for \(i_{i}\). This is the merit of an interleaved boost technique\(^2\),\(^3\).

6. Conclusion
A CRM bridgeless interleaved PFC has been presented. Its basic principle, control scheme, implementation problems, and experimental results have been shown thoroughly. It is evident that the new topology, at recent stage, be able to pass the IEC61000-3-2 class D standard while also performing reasonable efficiency even though some practical problems do exist. Further developments towards better results are still widely open and promising. This new topology is a good candidate towards low to middle power PFC target.

7. Future Work
It is important to improve further the proposed converter efficiency. IGBT can be a good candidate replacing traditional MOSFET in this area. This is because IGBT does not pose body diode problem as in MOSFET. However, it is still need some times until IGBT could be more suitable for high switching frequency application and gives lower on-time voltage character.

Input voltage and current glitch near zero-crossing should also be addressed properly. The glitch may give some penalties in complying the EMC standards.

It is also important to look deeper into the characterization of conducted and radiated EMI generation around this new topology.

References