Ultra-low-power signaling challenges for subthreshold global interconnects

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1. Introduction

Semiconductor devices are aggressively scaled in each technology node to obtain higher performance with maximum number of devices on chip. However, technology scaling significantly increases leakage power dissipation [1]. In recent years, increasing demand of portable devices and increased leakage power dissipation, thermal management, and self-heating of devices due to technology scaling makes power consumption a key design constraint in nanometer process technologies. Increased leakage power dissipation in nanometer regime can be tolerable for the highest performance application. However, it is the most challenging design issue for ultra low power (ULP) applications. Portable devices are bounded by ultra low power budget, which places pressing demand for ultra-low-power operation for longer battery life time for moderate performance applications. Many power efficient circuits are proposed using various power reduction techniques over the past few years [2,3]. Among all techniques, the most successful one is supply voltage ($V_{DD}$) scaling even below the threshold voltage ($V_{th}$) of device [4]. Recently, while designing low power systems importance is given to operate the device at minimum energy delay point (EDP) instead of minimum energy point (MEP). It is observed from Fig. 1 that minimum EDP of inverter with a fan out of four loading occurs at 0.4 $V_{DD}$ in the subthreshold region. Subthreshold operating region has great potential towards satisfying the ULP demand of portable systems having performance as a secondary design issue [4–6]. Thus, in future CMOS technologies, we can expect the domination of the subthreshold over superthreshold regime for ultra low power moderate throughput applications.

Variability and speed are the two important design challenges that are investigated in most of the previous work for subthreshold circuits [3,4]. Along with these two issues, there is a need to address the global interconnect resource performance under subthreshold conditions because global interconnects contribute significantly to both power and speed at the nanoscale. Though dimensional scaling has decreased transistor delay and power by orders of magnitude, interconnect performance has generally been negatively impacted by scaling [7]. Due to technology scaling even beyond Moore’s law, interconnect resistance and capacitance increase significantly, which can now directly impact the system performance. Global interconnect poses many design challenges due to increased chip size at every technology node with only a few potential solutions. Numerous researches have been carried out on global interconnect design in superthreshold region [7–9]. However, very few publication deals with interconnect design challenges under subthreshold conditions. Calhoun et al. [10] comprehensively addressed the challenging design issue of subthreshold FPGA and identified interconnects as a major design challenge. J. Kil et al. [11] explored gate voltage boosting technique to improve the subthreshold interconnect performance. However, there is a pressing need to explore the performance challenges for global interconnect resources under subthreshold conditions in the presence of process and temperature variations to achieve better global signaling performance.

Extremely high driver resistance under subthreshold conditions, increased device susceptibility to process parameters variations due to exponential relationship between subthreshold...
driving current and process parameters, and increased interconnect capacitance due to technology scaling have motivated us to investigate the performance of global interconnect under subthreshold conditions. Improving the delay performance will further extend the application area of subthreshold domain even to Field Programmable Gate Arrays (FPGAs).

The primary contributions of this paper are as follows:

1. This paper investigates the challenging design issues of subthreshold global interconnects using the conventional superthreshold approaches.
2. It proposes driver and interconnect optimization techniques for high speed subthreshold circuits. Also optimization of interconnect driver and interconnect parameters both under subthreshold and superthreshold conditions have been investigated.
3. Impact of $V_{th}$ and temperature variations on subthreshold interconnect performance has been investigated for different interconnect and device parameters.
4. Effect of crosstalk on subthreshold interconnect performance parameters like delay, power delay product (PDP), and RLC power has been explored.

The rest of the paper is organized as follows. Section 2 focuses on subthreshold operation of Si-MOSFET. Section 3 explores the conventional and proposed interconnect design techniques for subthreshold operating region. Section 4 investigates the effect of $V_{th}$ and temperature variations on delay, power dissipation and PDP of subthreshold interconnects. Section 5 examines the effect of crosstalk on subthreshold interconnects performance and Section 6 then concludes this paper.

2. Subthreshold operation of a MOSFET

Total power dissipation in digital circuits primarily consists of dynamic and static power dissipation. In well designed digital systems, the dynamic power dissipation is the dominant component in total power dissipation. Dynamic power dissipation of a gate can be expressed as follows [4]:

$$P_{dy} = \alpha C_{L} V_{DD}^{2}$$

(1)

where $\alpha$ is the switching activity, $f$ is the operating frequency, and $C_{L}$ is the load capacitance.

To keep power consumption within limit during technology scaling, $V_{DD}$ is scaled down, which degrades the circuit performance. To maintain better device performance, $V_{th}$ and oxide thickness of the device are also scaled down.

![Energy-delay curve for FO4 inverter.](image)

**Fig. 1.** Energy-delay curve for FO4 inverter.

This increases the leakage current components significantly. These leakage current components of Si-MOSFET device are shown in Fig. 2. Subthreshold leakage, direct tunneling gate leakage, gate induced drain leakage (GIDL), and reverse bias p–n junction leakage are the most important components in the nanometer region. Subthreshold leakage current between source and drain in MOSFET occurs when gate voltage is below $V_{th}$. It uses supply voltage less than the threshold voltage ($V_{DD} < V_{th}$). Subthreshold leakage dominates the other leakage components due to reduced $V_{th}$ and increases significantly as technology scales down [1,4]. As gate leakage is a strong function of $V_{DD}$, it is orders of magnitude less than superthreshold gate leakage due to low $V_{DD}$ in the subthreshold operating region [12] and the use of high-K material in advanced technology. Similarly, GIDL and p–n junction leakage can be negligible under subthreshold conditions [4]. Subthreshold drain current is expressed as follows [4]:

$$I_{D} = I_{0}e^{\left(V_{GS}-V_{th}-V_{th}^{n}V_{th}/V_{T}^{n}\right)}\left(1-e^{V_{TH}/V_{T}^{n}}\right)$$

(2)

where $I_{0}$ is a reference current proportional to ‘$W/L$’, which exponentially depends on $V_{th}$; ‘$n$’ is the subthreshold slope factor ($n=1+C_{G}/C_{Ox}$); $V_{T}$ is the thermal voltage; ‘$n$’ is DIBL coefficient. In subthreshold region, the propagation delay can be expressed as follows [4]:

$$T_{d} = \frac{KC_{L}V_{DD}}{I_{D}}$$

(3)

where $C_{L}$ is the output capacitance and ‘$K$’ is the fitting parameter [4].

A subthreshold MOS device operates at a very low current density level, which is very convenient for ULP applications. Moreover, devices in this regime exhibit maximum transconductance ($g_{m}$) to bias current ($I_{D}$) ratio, i.e., $g_{m}/I_{D}$, that leads to the maximization of power efficiency of the MOS circuit [6]. The next section explores the limitation of conventional interconnect techniques and proposed some new design strategies for high speed future subthreshold interconnects.

3. Performance analysis of subthreshold interconnects

To meet technology goals, the interconnect should also scale with technology. As technology scales down, the resistance of Cu wires increases, which leads to longer delay and electromigration problem for strong inversion operating region. However, in subthreshold region, electromigration is negligible due to lower current density ($\sim 0.5–1 \text{ mA} / \mu \text{m}$) [13] of drive current. Increased delay becomes more challenging in VLSI systems operating at low $V_{DD}$. The delay is even more pronounced in subthreshold circuits due to $V_{DD}$ lower than $V_{th}$.

The effect of driver resistance on interconnect delay can be illustrated with an RC delay model of interconnect line driven by a CMOS inverter and is given by [14]

$$\Gamma_{d} = R_{\text{ion}}(C_{\text{ion}}+C_{\text{load}}) + 0.4R_{W}C_{W}L^{2} + (R_{\text{dd}}C_{W}+R_{W}C_{\text{load}})l$$

(4)
where $R_{driv}$ is the driver resistance, $C_{driv}$ is the driver capacitance, $R_W$ and $C_W$ are interconnect resistance and capacitance, respectively, and $C_{load}$ is the load capacitance.

The driver resistance ($R_{driv}$) increases exponentially as $V_{DD}$ scales below $V_{th}$ and it is very high as compared to global interconnect resistance ($R_W$). However, the driver capacitance ($C_{driv}$) is very small as compared to global interconnect capacitance ($C_W$). Hence from Eq. (4), in subthreshold region global interconnect path delay is mainly dominated by $R_{driv}$ and $C_W$ contrary to superthreshold region in which it is mainly dominated by $R_W$ and $C_W$. The inductance effect can be negligible under subthreshold conditions due to lower operating frequency and higher driver resistance. The amount of literature on subthreshold interconnect design issues is very limited.

As IC technology scales down, interconnects are becoming the most limiting factor affecting integrated circuits functionality from speed, power dissipation and reliability perspectives. It is clear from Eq. (4) that increased interconnect capacitance at the global level and driver resistance plays an important role in determining subthreshold interconnection delay. Supply rails, clock signal transmission and complex interconnect architecture in future subthreshold FPGA need parallel long wires. Increased interconnect delay, variability and crosstalk may cause failure of subthreshold circuits. A significant amount of research work had already been carried out on global interconnect using different techniques for reducing the delay of global wires in superthreshold region including driver sizing, repeater insertion, interconnect width optimization, etc. [7,8,15,16]. Hence, it is important to investigate the effectiveness of previously proposed techniques along with some new optimization strategies for subthreshold conditions.

3.1. Conventional interconnects techniques

In subthreshold region, device delay increases exponentially as $V_{DD}$ scales down due to exponential behavior of subthreshold leakage current as shown in Fig. 1.

Global interconnects will further increase the total path delay due to higher capacitance thereby, causing circuit failure. Interconnect test benches used for exploring global interconnect design issues are shown in Fig. 3. Global interconnect of length 1–10 mm is considered for the simulation purpose [17]. The simulation is carried out using HSPICE at 32 nm technology node [18]. The equivalent RLC model of interconnect is used for measuring the delay, power and switching energy of Cu interconnects. The RLC parameters of Cu interconnect are extracted from PTM tool [18] with interconnect geometry as suggested in [19]. Test benches, shown in Fig. 3, are simulated for interconnect, driver and total path delay and PDP with fixed 50 fF load.

The most commonly used technique to reduce the path delay and PDP is to upsize the interconnect driver. To explore the delay and PDP, the test bench, shown in Fig. 3(a), is simulated for 1–10 mm interconnect length for different driver size. The total path delay in subthreshold and superthreshold operating regions significantly decrease with the increase in driver size. It is important to compare the effect of driver sizing on PDP for different interconnect lengths in subthreshold and superthreshold regions. Fig. 4 shows that the PDP of global interconnects for various interconnect lengths with different interconnect driver sizes in subthreshold and superthreshold operating regions. It is evident from Fig. 4 that as driver size increases from $16 \times$ to $32 \times$ minimum driver size, the PDP in subthreshold region decreases by 34% and of that in superthreshold region increases by 33%. In superthreshold region increase in PDP is due to 34.8% increase in power dissipation; however, because of less critical nature of driver capacitance and low swing signaling under subthreshold conditions power dissipation increases by only 5%, thereby improving PDP significantly. In case of superthreshold region, optimum PDP for 4 mm interconnect length can be obtained at $16 \times$ minimum size driver. Similarly, optimum driver sizes for minimum PDP can be obtained from Fig. 4 for different interconnect lengths.

It is also important to find out the interconnect length and driver size for which the interconnect delay dominates the driver delay under subthreshold conditions. We have plotted the driver delay and interconnect delay for various interconnect lengths and driver sizes in Fig. 5.
It can be observed from Fig. 5 that for driver size up to 16 × minimum driver size, the driver delay always dominates the interconnect delay. As driver size increases to 32 × minimum driver size, driver delay dominates the interconnect delay up to 6 mm interconnect length. From 6 mm interconnect length onwards, the interconnect delay starts dominating the driver delay. However in superthreshold region at 32 × minimum driver size and 400 μm interconnect length, the interconnect delay dominates the driver delay due to larger interconnect resistance. The above analysis clearly indicates that to reduce the total path delay and switching energy, larger size drivers are required for subthreshold application, which results in significant area penalty.

Tapered drivers are suggested in previous publications to reduce the delay and switching energy. This part of analyses examines the suitability of this technique under subthreshold conditions. Test setups 3(a) and 3(b) are simulated for 8 examinees the suitability of this technique under subthreshold application, which results in significant area penalty.

3.2. Proposed subthreshold interconnect techniques

This section presents device optimization for the interconnect drivers, interconnect parameter optimization along with the use of dynamic threshold MOSFET (DTMOS) to improve the performance of subthreshold interconnects. The next sub-section describes device optimization, which is followed by interconnect parameter optimization and then a sub-section on DTMOS.

3.2.1. Device optimization for subthreshold operation

Future subthreshold global interconnects for on-chip buses and clock distribution networks can significantly suffer from performance degradation due to increased driver resistance and interconnect capacitance. Conventional drivers designed for strong inversion region may not provide the optimum performance for subthreshold applications. In this part of analysis, we have investigated the effect of device optimization on the performance of subthreshold and superthreshold circuits. For device optimization purposes, a five stage inverter chain is considered. The PDP and delay are measured for the third inverter in the chain.

Superthreshold devices are normally optimized by considering the gate capacitance, gate leakage power dissipation, static power dissipation etc at nominal VDD. Also in superthreshold region, scaling of Vth is lower bounded by the amount of subthreshold leakage current. Such devices will give significant penalty in speed when operated under subthreshold conditions. The choice of Vth is a tradeoff between device speed and static leakage. For subthreshold region, lower static leakage due to scaled VDD even below Vth allows further reduction of Vth. From Eq. (2), increasing (VGS−Vth) by reducing Vth results in the shifting of device operating point towards moderate inversion region thereby, increasing the drive voltage. Fig. 8 shows the effect of Vth scaling on PDP performance in subthreshold and superthreshold regions. It is evident from Fig. 8 that reducing Vth from 0.49 V (technology defined) to 0.43 V (optimized) in subthreshold region reduces PDP by 15% and delay improves by 3.5 ×. However, upon scaling Vth in superthreshold region 4.5 × increase in power dissipation masks...
21% improvement in delay as shown in Fig. 9, which results in increase in PDP by 71%. As shown in Fig. 9, in subthreshold region, upon scaling $V_{th}$, the rate of change of delay is higher than that in superthreshold region. Hence, by using the optimum value of $V_{th}$, better performance in terms of delay and PDP can be achieved under subthreshold conditions.

The inverse subthreshold slope ($S$) of a short channel MOSFETs under subthreshold condition is an excellent measure of the gate control on the channel and can be expressed as follows [20]:

$$S = 2.3V_t \left[ 1 + \frac{3T_{OX}}{W_{dep}} \left[ 1 + \frac{11T_{OX}}{W_{dep}} e^{-\frac{V_{th}}{2\phi_S}} \right] \right] \tag{5}$$

where $W_{dep}$ is the depletion width, $L_{eff}$ is the effective channel length, $V_t$ is the thermal voltage and $T_{OX}$ is the oxide thickness. Smaller $S$ is preferred for better device performance. The delay and switching energy in terms of $S$ is expressed as follows [21]:

$$T_{delay} = C_{g'} L_{eff}$$

$$E_{dyne} = C_{ox} S^2 \tag{7}$$

where $C_{g'}$ is the load capacitance.

In technology scaling, $T_{OX}$ scales down slowly from 130 nm technology node to keep minimum gate leakage current in case of superthreshold devices. It deteriorates $S$ that causes lowering of $I_{ON}/I_{OFF}$ ratio thereby, degrading SNM. In subthreshold operating region due to lower $V_{th}$, reducing $T_{OX}$ will not significantly increase gate leakage current [4]. From Eqs. (5–7), device performance parameters can be improved by reducing $T_{OX}$ [12]. It provides an opportunity to explore the most suitable value of $T_{OX}$ for optimum value of subthreshold slope and gate capacitance. The effect of $T_{OX}$ scaling is explored for device parameters $S$ and $C_{ox}$ as shown in Fig. 10. It is evident from Fig. 10 that $S$ decreases by reducing $T_{OX}$ from 1.15 nm to 0.9 nm, which results in significant improvement of PDP in subthreshold region as shown in Fig. 11. Whereas from Fig. 12, it is observed that in case of superthreshold region decrease in $T_{OX}$ results in significant increase in gate leakage current and static power dissipation. This results in increase in PDP as shown in Fig. 11 upon $T_{OX}$ scaling.

It is important to investigate the joint impact of scaling $V_{th}$ and $T_{OX}$ on PDP and delay in both the operating regions. It is observed from Fig. 13 that reducing $T_{OX}$ and $V_{th}$ from 1.2 nm and 0.49 V to 0.9 nm and 0.43 V, respectively, increases PDP by 6.48 x in superthreshold and decreases by 1.41 x in subthreshold region.

The delay decreases by $9.55 \times$ and $1.61 \times$ in subthreshold and superthreshold regions, respectively.

The optimum values of $V_{th}$ and $T_{OX}$ are used to generate HSPICE model files for interconnect driver from a specific tool called “Nano CMOS” [18]. Fig. 14 compares the driver delay and total path delay for conventional and optimized interconnect driver. It is evident from Fig. 14 that the total path delay has been reduced by 50% and interconnect driver delay is reduced by 54% for 10 mm length. Thus, by using optimum device parameters, better interconnect
driver performance can be achieved without any area penalty over a wide range of interconnect lengths as shown in Fig. 14.

### 3.2.2. Interconnect parameters optimization

The interconnect thickness (‘T’) and height (‘H’) are typically kept constant in superthreshold region and width (‘W’) and spacing (‘S’) are commonly used by the designer for the optimization of global interconnects under subthreshold conditions [22]. This part of analysis explores different interconnect optimization strategies for subthreshold region and also examine their effectiveness in superthreshold region. It is clear from Section 3 that the total path delay also depends on global interconnect capacitance. Hence, it can be reduced by using more spacing between the wires than the minimum-space global interconnects provided by the technology. We have kept the width and height constant to explore the impact of interconnect spacing on subthreshold interconnects. Fig. 15 shows that by increasing spacing between interconnects, both the interconnect and the total path delay decrease.

In ITRS, an aspect ratio of ‘3’ is suggested for global interconnects. Large interconnect thickness and height are used in superthreshold region to minimize problems due to electromigration.

As electromigration in subthreshold region is negligible, smaller interconnect height can be used. Any decrease in interconnect capacitance with a moderate increase in resistance can improve the performance significantly because interconnect resistance is less critical for subthreshold interconnect.

In superthreshold operating region, reducing interconnect height by 33% increases the delay and PDP by 46% and 56%, respectively, due to increase in interconnect resistance whereas for subthreshold region, the delay and PDP reduce by 10% and 63%, respectively, due to decrease in capacitance for 2 mm interconnect length. This is because increase in resistance of the interconnect is not critical under subthreshold condition.

This technique will be more efficient along with device optimization technique to improve the performance of subthreshold global interconnects. To better understand the effect of device and interconnect optimization techniques on interconnect resource performance in subthreshold region we have plotted delay and PDP using the conventional method and the proposed one. Figs. 16 and 17 show the joint impact of interconnect driver and interconnect height and width optimization on delay and PDP under subthreshold conditions for fixed interconnect length. It has been observed from this part of analysis that subthreshold interconnect performance can be greatly improved by optimizing the device parameters and interconnect parameters simultaneously. On the contrary, the performances of superthreshold circuits degrade with device and interconnect parameters optimization. Hence,
proposed device and interconnect optimization strategies are useful only in subthreshold operating region.

### 3.2.3 Dynamic threshold MOS (DTMOS) technique

Another alternative way to achieve better interconnect driver performance is to use DTMOS logic. As gate is connected to substrate, $V_{th}$ of such transistors is dynamically changed with the input. However, it requires triple well process technology for the implementation purpose [5]. Fig. 18 shows the delay and PDP comparison for conv. MOS and DTMOS drivers. Fig. 18 shows that DTMOS driver has lower delay and switching energy for the same performance, DTMOS based driver implementation shows significant amount of area saving over driver upsizing technique even after accounting for the area overhead associated with DTMOS due to triple well process from [23]. The next section investigates the effect of $V_{th}$ and temperature variation on subthreshold interconnect performance.

### 4. Impact of process and temperature variations on subthreshold interconnects

It is well established that susceptibility to system and random process variations increases with the continuous scaling down of VLSI technology. Exponential dependency of subthreshold drive current on $V_{th}$ and temperature in subthreshold operating region makes process and temperature variations of great interest while designing robust ULP systems. Small variation in the device $V_{th}$ will translate into exponential variation in bias current and hence the device delay and power dissipation. It is clear from Eq. (1) that the increase in temperature increases the subthreshold leakage current. Hence, the change in temperature affects performance of subthreshold systems. It is, therefore, important to investigate the impact of $V_{th}$ and temperature variations on subthreshold interconnect driver for different driver size and interconnect lengths.

#### 4.1 Effect of threshold voltage variations

Amongst different variability sources, $V_{th}$ variation is extremely important. The process parameters like physical gate length ($L_g$), $T_{OX}$, and channel doping ($N_{ch}$) are having direct impact on $V_{th}$ [24]. In this part of analysis, we have considered the effect of $V_{th}$ variation on subthreshold interconnect performance. To investigate the effect of process variability on interconnect performance, we have performed sufficient Monte-Carlo simulations for different interconnect lengths and driver size using conventional (conv.) and optimized (opt.) interconnect drivers. The standard deviation of device $V_{th}$ in terms of these process parameters is given by [25]

\[
\sigma_{V_{th}} = 3.19 \times 10^{-6} T_{OX} \sqrt{N_{ch} - \frac{1}{W_{eff} L_{eff}}} 
\]

Assuming $V_{th}$ to be normally distributed and modeling $I_{sub}$ as a lognormal random variable, current variability has been modeled in [26] as follows:

\[
\frac{\sigma_{I_{sub}}}{\mu_{I_{sub}}} = \sqrt{e^{3\sigma_{V_{th}}/\sqrt{2\pi}T_{eff}^{1/2}} - 1}
\]

To explore the impact of process variation, we have considered 15% (3\(\sigma\)) variation in $V_{th}$ [27]. The effect of $V_{th}$ variation on delay and power dissipation is shown in Figs. 19–21. As shown in Fig. 19, using opt. device, the delay variability reduces significantly. This is due to the reduction in $V_{th}$, which moves the device operating point towards moderate inversion region in which subthreshold current is less sensitive to variations as compared to deep subthreshold region [5]. Also, it has been observed from Fig. 19 that increasing the transistor size reduces the effect of $V_{th}$ variations [28] by 3.6% and 30% on delay performance for conv. and opt. driver, respectively. This can be validated by exploring the transient response of interconnect drivers. The snapshot of
voltage transient response of interconnect driver driving 2 mm interconnect line under 15% $V_{th}$ variation is shown in Fig. 20. However, from Fig. 21 power variability due to $V_{th}$ variation significantly increases than conv. driver as width of opt. driver increases. It is also observed that, for $8 \times$ minimum driver size, optimum power variability is obtained for conv. interconnect drivers over a wide range of interconnect lengths. It can be inferred from Figs. 19 to 21 that the opt. device driver can reduce the delay variability at the cost of increased power variability. This is due to increased leakage and static power dissipation for long interconnects length.

4.2. Effect of temperature variation

Temperature dependant bias current in subthreshold region can be expressed as [29]

$$\frac{\partial I_{DS}}{\partial T} \approx I_{DS} \left( \frac{\partial^2}{\partial T^2} - \frac{(\partial V_{th}/\partial T)(\partial V_{th}/T)}{nV_{T}} \right)$$  (10)

![Fig. 20. Transient response comparison under $V_{th}$ variation (3σ = 15%) for $L = 2$ mm for conv. and opt. device.](image)

To examine the temperature effect on device performance over a wide range of $V_{DD}$, we have considered five stage inverter chain as a test bench and the delay is measured for the third inverter and is shown in Fig. 22. It is clear from Fig. 22 that as temperature increases, the delay decreases significantly in deep subthreshold region but starts increasing from near moderate inversion region. Also, it has been observed from Fig. 22 that as $V_{DD}$ decreases, the variation in delay increases significantly. Hence, it is necessary to operate the subthreshold device near to moderate inversion region to reduce the effect of temperature variation.

This part of analysis investigates the effect of temperature variation on subthreshold interconnects. Fig. 23 explores the effect of temperature variation on power dissipation and delay for different interconnect driver size using conv. and opt. drivers for 2 mm interconnect length. Increasing the temperature results in the reduction of interconnect delay for conv. driver whereas it increases for opt. driver. Increase in delay for opt. driver is due to reduced $V_{th}$, which moves the device operating point towards moderate inversion region. The current in such cases is no longer exponentially dependant on $V_{GS}$ and therefore less sensitive to temperature variation [5] as shown in Fig. 23. It has been observed that opt. driver is having higher power dissipation variation ($P_{av}$) than conv. interconnect driver due to increased leakage and static power dissipation upon reducing $V_{th}$ and $T_{OX}$ as from Fig. 12. Increasing driver size from $4 \times$ to $32 \times$ minimum.
driver sizes for opt. device driver reduces the effect of temperature variation from 30% to 18% upon increasing temperature from 25 °C to 175 °C. It is also observed that sizing does not have a significant impact on temperature variability using conv. interconnect driver. The next section studies the effect of crosstalk on the performance of subthreshold interconnects.

5. Effect of crosstalk on subthreshold interconnect performance

Crosstalk is the interference in a victim line signal transmission caused by switching activity on aggressor lines. It is one type of coupling mechanism between the disturbed interconnects line and the disturbing interconnects lines. The crosstalk effect has become a challenging design issue due to growing integration density with every technology node. Future subthreshold applications like subthreshold FPGA performance will be affected largely due to crosstalk. Rise and fall time may vary due to switching of adjacent lines and it may become a cause of subthreshold circuit failure. The crosstalk also causes voltage glitch due to the transition in one or more adjacent interconnects [13]. The effect of this unwanted noise interference depends on the value of the coupling capacitance ($C_c$), transition-time skew and the adjacent interconnect length. In order to keep crosstalk minimum, capacitance between two wires should be reduced [13]. This is possible by breaking a long line using intermediate buffers; however, in subthreshold operating region inserting repeaters increases the delay and PDP as shown in Fig. 7. Hence, this technique is not feasible under subthreshold conditions. Another approach of reducing the crosstalk is to use shielding wires, which also increases the capacitive load and therefore, the delay [13]. A more suitable approach to reduce the crosstalk effect is to increase the spacing between wires.

To explore crosstalk effect under subthreshold condition, a worst-case $4 \times$ minimum size driver from Fig. 4 and 10 mm long interconnect line is considered. The crosstalk affected interconnect line is termed as a victim line and lines that cause crosstalk on victim, we have simulated the test setup as shown in Fig. 24 for different signal direction on aggressor 1, aggressor 2, and victim lines.

The effect of crosstalk on subthreshold interconnect parameters is explored in Table 1. As shown in Table 1, if aggressor 1 and aggressor 2 are having simultaneous transitions in the same direction then the victim performance parameters are not affected by adjacent signals. However, opposite signal direction on aggressor 1 and aggressor 2 largely affects rise and fall time of the victim wire. It is clear from Table 1 that the capacitive crosstalk is strongly dependent on the signal direction of adjacent wires and it is having large impact on total path delay and PDP. To study the effect of spacing between two wires (pitch) on crosstalk, we have kept width constant and different wire spacing (pitch) is used to keep width/pitch ratio ($r$) as 1, 0.75, 0.5, and 0.35. Equivalent RLC parameters are used for simulation purposes. Fig. 25 shows the effect of capacitive crosstalk on rise and fall time of victim for opposite signal transition. It is evident from Fig. 25 that as pitch increases the difference between rise and fall time decreases.

To study the effect of crosstalk on transition less victim line, we have kept victim at low logic and low to high transition on both the aggressors is applied and corresponding results are plotted for different width and pitch ratio as shown in Fig. 26(a). It is clear that victim experiences rise glitch due to these transitions and is less for lower value of $r=$width/pitch. Fig. 26(b) shows that undershoot occurs for victim at low logic and high to low logic on aggressor lines and it is minimum for 0.35 width to pitch ratio. Fig. 27 shows the rise and fall time delay of victim wire for different values of ‘$r$’. It can be concluded from Fig. 25 to 27 that there is a need to put more efforts toward reducing the crosstalk effect so that subthreshold

![Fig. 24. Schematic of Cu equivalent circuit to model crosstalk between adjacent wires.](image)

![Fig. 25. Effect of wire spacing on rise and fall time delay.](image)

Table 1

<table>
<thead>
<tr>
<th>Aggressor transition</th>
<th>Victim transition</th>
<th>Rise time (ns)</th>
<th>Fall time (ns)</th>
<th>Delay (ns)</th>
<th>PDP (fJ)</th>
<th>RLC power (nW)</th>
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<tr>
<td>Without aggressors</td>
<td>Low to high</td>
<td>256.7</td>
<td>285.2</td>
<td>270.9</td>
<td>60.64</td>
<td>17.35</td>
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<td></td>
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<td>286.14</td>
<td>264.2</td>
<td>59.16</td>
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<tr>
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<tr>
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<td>387.9</td>
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circuits can retain better performance even for complex interconnect architecture like FPGA.

6. Conclusion

This paper has successfully carried out the design and analysis of subthreshold global interconnects. It also highlighted the differences in the optimization and design of interconnects under subthreshold and superthreshold conditions. It has been observed that the driver delay rather than the interconnect delay dominates under subthreshold conditions. Therefore, it can be concluded that intermediate repeater insertion technique is not suitable for subthreshold contrary to superthreshold regime. Hence, longer interconnect length must be considered while optimizing drivers for global interconnects. Moreover, the total path delay under subthreshold is determined by the driver resistance and the interconnect capacitance. Hence, the interconnect performance under subthreshold conditions can be significantly improved by reducing the driver resistance and the interconnect capacitance. Driver sizing is the key knob in enhancing the interconnect performance under subthreshold conditions. This work has, therefore, explored driver optimization techniques to improve interconnect speed and PDP. Moreover, DTMOS based drivers are also employed for better speed and energy performance. However, using DTMOS, power dissipation increases causing increase in switching energy. Hence an optimum supply voltage needs to be explored for DTMOS technique to achieve minimum possible switching energy. Interconnect width and thickness, designed for superthreshold region, need to be redesigned and optimized for subthreshold applications. Aspect ratio scaling, which is not possible in superthreshold domain due to electromigration problem, is feasible in subthreshold region due to lower current density. It is, therefore, important to explore new aspect ratios of interconnect to reduce the interconnect capacitance for improving the performance in terms of delay and energy. Since the capacitance and not the resistance of the interconnect determines delay under different subthreshold conditions, and hence it is essential to investigate the performance of a SWCNT as an interconnect because it has higher resistance but much lower capacitance than Cu. However, performance of SWCNT interconnects may vary at different operating point under subthreshold regime. In the end, variability analysis in this work shows that there is a need to reduce the impact of PVT variations on subthreshold interconnect performance so that logic bit retains its value even for long interconnect length up to few millimeters.

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