An advanced low power, high performance, strained channel 65nm technology

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I. ABSTRACT

An advanced low power, strained channel, dual poly CMOS 65nm technology with enhanced transistor performance is presented. At 1V and off current of 100nA/um, transistors have record currents of 1.21mA/um and 0.71mA/um for NMOS and PMOS respectively. This industry leading 65nm technology is currently in high volume manufacturing.

II. INTRODUCTION

Moore's Law requires continuous improvement in transistor performance and process technology with a two year development cycle. In this paper, we present improved performance for 35nm gate length transistors, further enhancing our industry leading 65nm technology [1].

The key features of our 65nm technology as described earlier [1] are summarized below. Using advanced 193nm lithography the technology design rules support a feature pitch of 220 nm, and a SRAM cell size of only 0.57 μm^2. The technology has 8 layer copper metallization with low K inter layer dielectric. Gate leakage concerns limit the silicon oxy-nitride gate dielectric thickness to 1.2nm, high transistor performance is achieved by using dual poly gates, NiSi and 35 nm gate lengths with enhanced uni-axial strain [2]. Figs. 1 and 2 show the cross-sectional TEM for the 35nm gate length N and P transistors respectively.

III. TRANSISTOR IMPROVEMENTS

To improve the transistor performance over [2], their short channel effects (SCE), series resistance (Rext) and mobility were all improved. For NMOS, SCE and Rext were improved by optimizing the thermal anneals and using advanced implants and co-implants; while to further improve the mobility we optimized second generation strain enhancement techniques. Similarly for PMOS SCE and Rext, we improved the source and drain regions, the tips and the halos, by optimizing anneals and using advanced implants, and enhanced the strain in the channel to get higher mobility using higher Ge fraction in stressor regions.

To improve the SCE without gate oxide scaling, the junction depths had to be scaled aggressively. With the optimized process and shallow junctions NMOS transistors down to gate lengths of 35nm have Vt roll off of less than 35mV (Fig. 3), with a drain bias of 1.0V the DIBL is only 150mV/V, while the sub-threshold slope is 105mV/decade (Fig.4). Fig. 5 shows the NMOS off current as a function of gate lengths, as seen, for 35nm gate length the off current is 100nA/um. Similarly for PMOS transistor down to gate lengths of 35nm, the Vt roll-off is less than 10mV (Fig. 6). Again with drain bias of 1V, the DIBL is 150mV/V, sub-threshold slope is less than 110mV/decade (Fig. 7) and finally the off current is only 100 nA/um (Fig. 8).

Transistor gate length scaling results in higher drive currents and this increases the relative importance of series resistance. Due to solid solubility and activation limits, shallow junctions invariably lead to an increase in sheet resistance. However, using co-implants and optimized anneals, transistors with improved series resistance and shallow junctions were fabricated. For a fixed source and drain overlap capacitance, optimized anneal and implant processes reduce the Rext by 35% for NMOS, and by 65% for PMOS.

IV. STRAIN ENHANCEMENT AND POLY PITCH

Uni-axial channel strain is an efficient way to enhance mobility by band repopulation and phonon suppression for electrons and due to band structure warping and carrier redistribution for holes. NMOS channel strain was optimized by improved thermo-mechanical design of spacers and stress inducing film, giving 20% mobility gain over [2] and 40% over unstrained silicon (Fig, 9). PMOS (Fig.10) uses higher Ge % fill and optimizes stressor trench shape for 30% mobility gain over [2] & nearly 100% over unstrained.

It is important to note that these results are quoted for transistor drawn at the minimum design rule poly pitch of 220nm. As seen in Fig. 11, higher gains can be quoted with wider poly pitch as more mechanical stress can be created in wider spaces. However, for the technology to fully harness transistor performance gain it is imperative to consider only the results with design rule minimum pitch, as is done here.

V. PERFORMANCE RESULTS

The 65nm technology has record high transistor saturation drive currents of 1.21 & 1.62 mA/µm for N and 0.71 & 0.91mA/µm for P at 1.0V & 1.2V respectively. With V_{DS} = 50mV the linear currents are 0.184 mA/µm for N & 0.105 mA/µm for PMOS. The Ion-Ioff, transistor I_{DS}-V_{DS} and sub-threshold characteristics of transistors with 35nm gate lengths are shown in Figs. 12 through 16. Fig. 17 shows the ring oscillators delays plotted as a function of the sum of transistor off currents, for leakage of 200nA/um the median value of stage delay is 4.25ps. Fig. 18 shows the technology trend for RO stage delay, we have shown 0.73x reduction in delay for each successive technology generation, this corresponds to 1.37x frequency increase per generation. The industry leading transistor performance presented here are on a mature 65nm technology, running with record high yields on multiple products in several high volume factories. Fig. 19 shows die photographs of the single core and dual core microprocessors currently in production.

VI. CONCLUSIONS

We report improved performance on 65nm technology for transistors with 35nm gate lengths. At 1V and 100nA/µm record drive currents of 1.21mA/µm and 0.71mA/µm for N and P respectively and ring oscillator delay of 4.25 ps are reported on a technology running in high volume manufacturing across multiple factories.

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VII. ACKNOWLEDGEMENTS

We would like thank our numerous colleagues in PTD, QRE and TCAD groups of Intel Corporation for their help, support and guidance.

VIII. REFERENCES

[1] P. Bai., IEDM Tech. Dig., p. 197-200, 2004

[2] K. Mistry, VLSI Symp Dig, p. 50-51, 2004

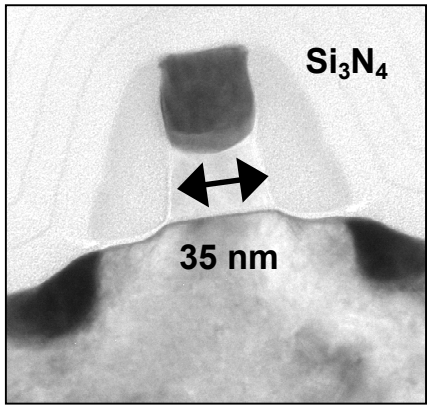


Fig. 1 X-TEM of 35nm gate NMOS.

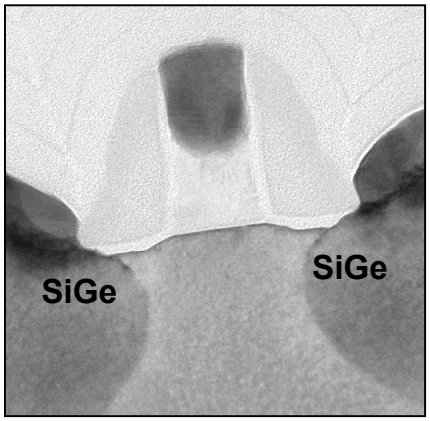


Fig. 2 X-TEM of 35nm gate PMOS.

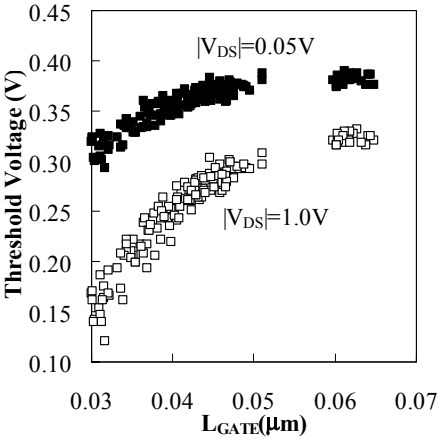


Fig. 3 NMOS threshold voltage as a function of gate length. Note the excellent Vt roll off and low DIBL for gate lengths down to 35nm.

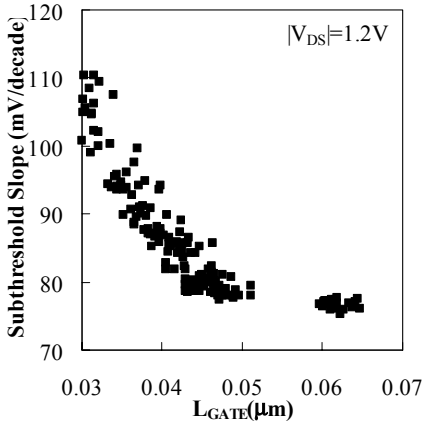


Fig. 4 NMOS sub-threshold slope as a function of gate length. Sub-threshold slopes, measured with drain biased at 1.2V, are 100 mV/decade down to gate lengths of 35nm.

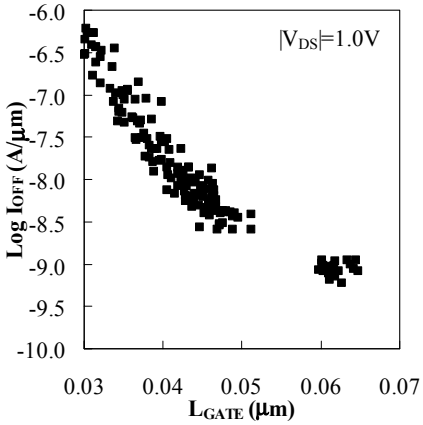


Fig. 5 NMOS off current as a function of gate length. For a gate length of 35nm, the off current is less than 100nA/um.

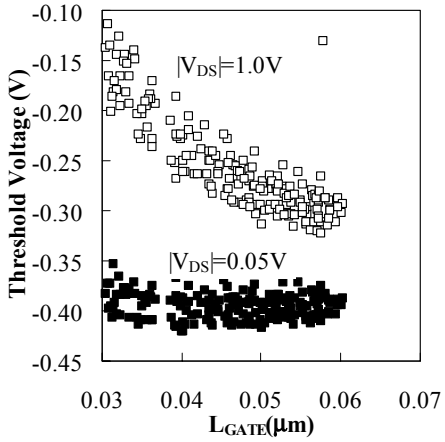


Fig. 6 PMOS threshold voltage as a function of gate length. Note the excellent Vt roll off and low DIBL for gate lengths down to 35nm.

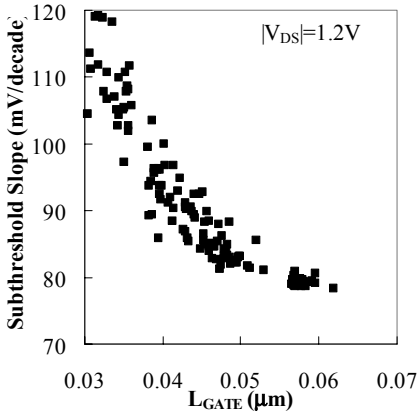


Fig. 7 PMOS sub-threshold slope as a function of gate length. Sub-threshold slopes, measured with drain biased at 1.2V, are less than 110 mV/decade down to gate lengths of 35nm.

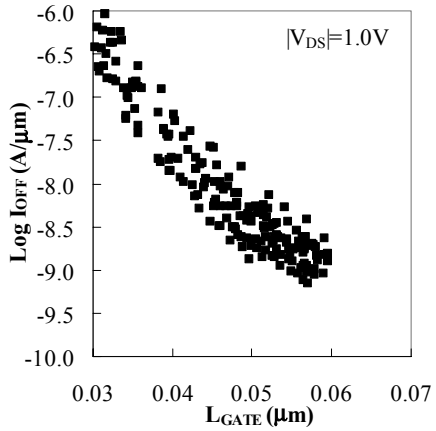


Fig. 8 PMOS off current as a function of gate length. For a gate length of 35nm, the off current is lesser than 100nA/um.

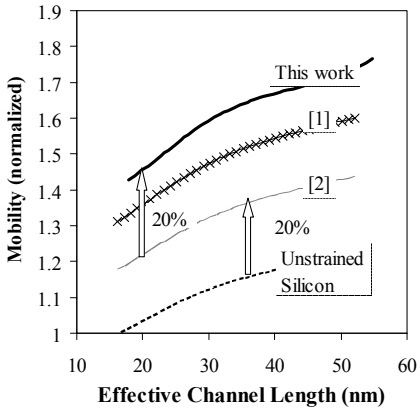


Fig. 9 NMOS Mobility as a function of gate length. Across the range the mobility increases by >20% for this work over 90nm technology [2].

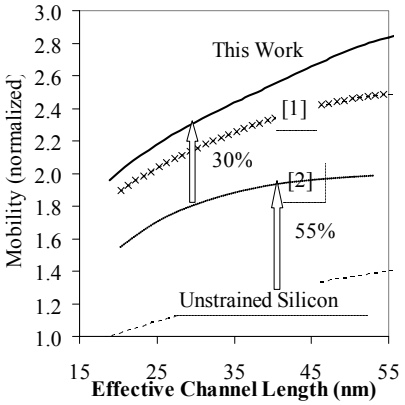


Fig. 10 PMOS mobility vs. gate length. Mobility increases by 30% for this work over 90nm technology [2], and is nearly double of that without stressor films.

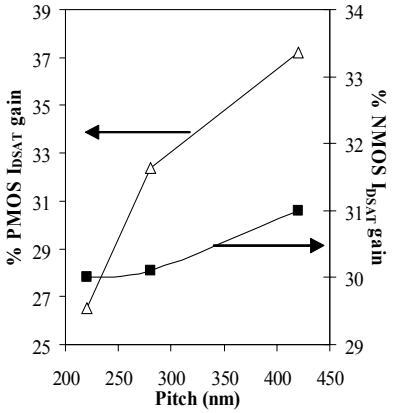


Fig. 11 Percentage gain in I_{DSAT} as a function of transistor poly pitch. The gain increases with wider pitch due to increased mechanical stress in these geometries. All results reported in this paper are at design rule pitch of 220nm

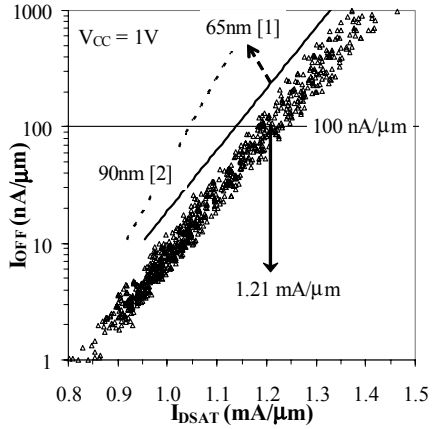


Fig. 12 NMOS I_{DSAT} vs Off current. For 100nA/µm off current the median Idsat is 1.21mA/µm. At 1.2V the median Idsat is 1.62 mA/µm.

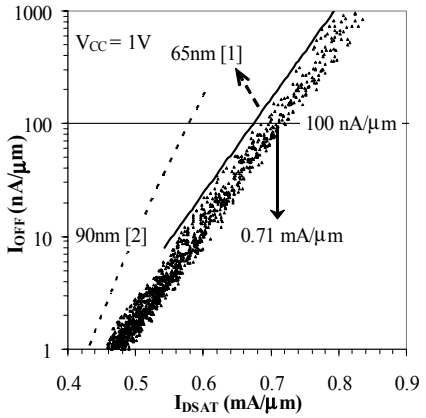


Fig. 13 PMOS I_{DSAT} vs Off current. For 100nA/µm the median Idsat is 0.71mA/µm. At 1.2V, the median Idsat is 0.91 mA/µm.

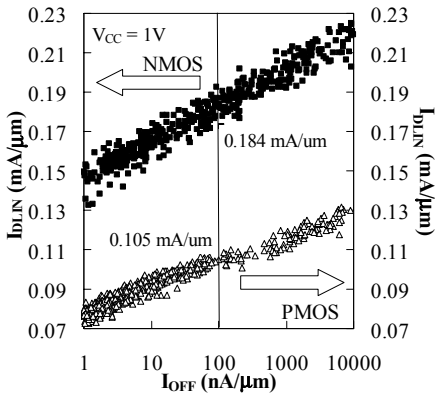


Fig. 14 Linear Current Vds=50mV vs Off current for both NMOS and PMOS. For 100nA/µm the median Idlin is 0.184 mA/µm for NMOS and 0.105 mA/µm for PMOS.

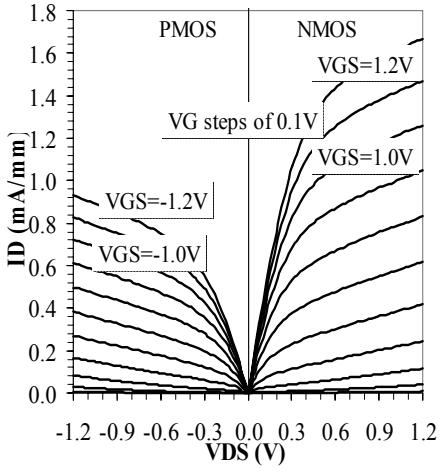


Fig. 15 I_{DS}-V_{DS} for 35nm gate lengths showing excellent transistor characteristics.

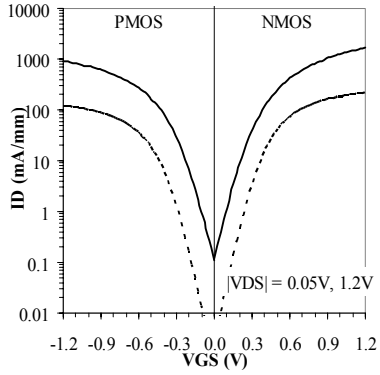


Fig. 16 Sub-threshold curves (I_{DS}-V_{GS}) for 35nm gate lengths with good gate control for both NMOS and PMOS transistors.

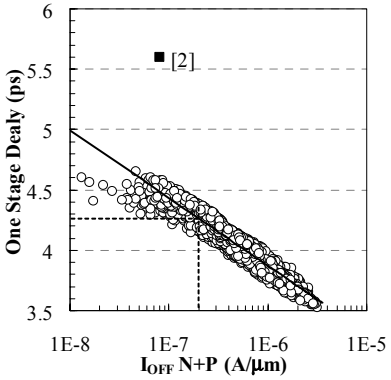


Fig. 17 Ring oscillator delay as a function of total transistor leakage current. Delay per stage is lesser than 4.25 ps for a total leakage of

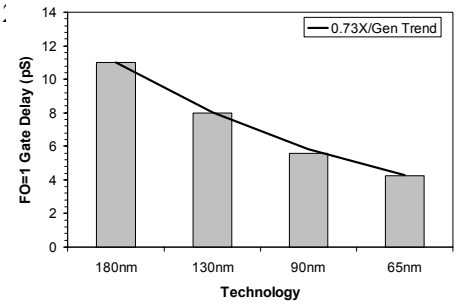
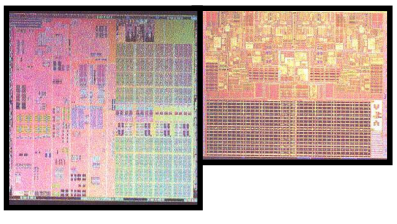


Fig. 18 Technology trend for stage delay showing 0.73x delay reduction per generation (1.37x frequency)



Single Core Dual Core

Fig. 19 Die photo of single core and dual-core microprocessors in high volume production today.