A FIVE LEVEL CASCADED MULTILEVEL INVERTER FED BRUSHLESS DC MOTOR
WITH PHASE SHIFTED CARRIER PWM TECHNIQUES

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ABSTRACT

In high power high voltage application BLDC motor are widely used because of high efficiency, simple construction, low cost less maintenance and high torque or high output power per unit volume. For driving the BLDC motor we required inverter. PWM inverter which gives good performance. In two level inverter there is a problem of harmonics distortion, lower electromagnetic interference, high DC link voltage, high dV/dt, heating of rotor shaft, voltage spikes across the motor terminals etc. The increase in the number of steps of voltage is the solution of the above problem. This can be possible using multilevel inverter. In this paper five level cascade H bridge inverter fed BLDC motor drive is proposed. The design of the inverter topology and phase shifted pulse width modulating technique are presented in this paper. Simulation is carried out using matlab / simulink, validating the steady state and dynamic performance of the drive.

KEYWORDS: Multilevel Inverter, Pulse Width Modulation (PWM), BLDC, Medium Voltage Ac Drives

INTRODUCTION

Because of powerful actuators in small sizes for industrial applications, BLDC motors gradually replace DC motors. Compared to same-output-rating DC motors, BLDC motors are less maintenance due to the lack of commutator and have a high-power density which is ideal for high torque-to-weight ratio applications [1]. Compared to induction machines, they have lower inertia allowing for faster dynamic response to reference commands, improved reliability and enhanced life, and are widely used for variable speed drive systems of the industrial applications [2]. It is known that adjustable-speed drives can be used for heating, ventilation, and air conditioning systems [3][4] to achieve great energy saving effects for partial loads by lowering motor speeds. Due to the above excellent characteristics, researchers take their efforts on the study of control strategies to improve the performance of BLDC motor systems. For instance, Park [5] used feed-forward compensator with disturbance torque observer to perform BLDC motor speed control and improved the servo stiffness.

For driving the BLDC motor we required inverter. In two level inverter there is a problem of harmonics distortion, lower electromagnetic interference, high DC link voltage, high dV/dt, heating of rotor shaft, voltage spikes across the motor terminals etc. The increase in the number of steps of voltage is the solution of the above problem. This can be possible using multilevel inverter.

Recently, developments in semiconductor technology and power electronics have lead improvements in power electronic systems. Hence, different circuit configurations namely multilevel inverters have became popular and considerable interest by researcher are given on them [1-2].Multilevel topologies provide a smart way of connecting switches in series, thus enabling the processing of voltages that are higher than the device rating. The industry need for medium voltage drives has initiated considerable research in this area, in which most applications include drives for,
compressors, pumps, conveyors, blowers and the like. In general, multilevel converters are efficient means of reducing harmonic distortion and \( \frac{dv}{dt} \) of the output voltages, which makes this technology important to utility interface and drives. The main reason for this attractiveness of multilevel inverters is that the output voltage waveforms can be generated at low switching frequencies with high efficiency and low distortion and large voltage between the series devices is easily shared.

There are a limited number of topologies that provide multilevel voltages and are suitable for medium voltage applications. The most well-known topologies are the neutral-point clamped (NPC), the flying capacitor (FC), and the cascaded H-bridge multilevel converters [6-8]. Other topologies such as the hybrid converters have been proposed as well, but they are not fully received for industrial applications [9] [10].

The NPC multilevel converter is a natural expansion of the three-level converter presented by Nabae. The multilevel NPC converter requires multiple clamping points to synthesize the different voltage levels across the output. The disadvantage of multiple clamping points is a limitation on the maximum voltage sharing across all the dc link capacitors [9]. Another drawback of the multilevel NPC converter is the need for series connection of the clamping diodes [11].

In case of floating capacitor Converter, by properly using the dc link and floating capacitor voltages, one can produce the required voltage levels across the output terminals. The redundant switching states can be used to achieve proper voltage control across the floating capacitors is an interesting property of the floating capacitor converter. In general, the energy stored in the floating capacitors is a limiting factor to increasing the number of voltage levels, which makes the five-level approach the most practical for industrial applications. An increased number of voltage levels may only be practical from the view point of floating capacitor requirements if the carrier frequency of the converter is increased. However, there are tradeoffs that should be observed between carrier frequency and switching losses in the converter.

In case of the cascaded H-bridge multilevel converter have the advantage of connecting single-phase inverters in series that are fed by independent dc voltage sources. Stair cased output voltage is produced by adding and/or subtracting the voltages of the single-phase modules. If active front-end rectifiers are used in the single-phase modules, the power flow may be bi-directional.

In this paper five level cascade H bridge topology is proposed. A general method of multilevel modulation phase shift PWM technique is utilized to drive the inverter and can be extended to any number of voltage levels. The simulation of the proposed topology is also presented.

**PROPOSED TOPOLOGY**

Figure 1 shows the proposed five level cascade H bridge inverter fed BLDC motor drive. Figure 2 shows single phase structure of a multilevel cascade H bridge inverter.

The N-level cascaded H-bridge, multilevel inverter comprises \( \frac{1}{2}(N-1) \) series connected single phase H-bridges per phase, for which each H-bridge has its own isolated dc source. Three output voltages are possible, ±Vs, and zero, giving a total number of states of \( \frac{3}{2}(N-1) \), where N is odd. Figure 5 shows one phase of a n-level cascaded H-bridge inverter.

The cascaded H-bridge multilevel inverter is based on multiple two level inverter outputs (each H-bridge), with the output of each phase shifted. Despite four diodes and switches, it achieves the greatest number of output voltage levels for the fewest switches.

Its main limitation lies in its need for isolated power sources for each level and for each phase, although for VA compensation, capacitors replace the dc supplies, and the necessary capacitor energy is only to replace losses due to inverter losses. Its modular structure of identical H-bridges is a positive feature.
The number of levels in the line-to-line voltage waveform will be \( k = 2N - 1 \).

While the number of levels in the line to load neutral of a star (wye) load will be \( p = 2k - 1 \).

The number of capacitors or isolated supplies required per phase is \( N_{\text{cap}} = \frac{1}{2}(N - 1) \).

The number of possible switch states is \( n_{\text{states}} = N_{\text{phases}} \).

The number of switches in each leg is \( S_n = 2(N - 1) \).

**Advantages**

- The number of possible output voltage levels is more than twice the number of dc sources (\( m = 2s + 1 \)).
- The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

**Disadvantages**

Separate dc sources are required for each of the H-bridges. This will limit its application to products that already have multiple SDCSs readily available.

**DESIGN OF PROPOSED NOVEL CASCADE H-BRIDGE INVERTER**

**Device Current**

The IGBT and DIODE currents can be obtained from the load current by multiplying with the corresponding duty cycles. Duty cycle, \( d = \frac{1}{2}(1 + H \sin(\omega t)) \) Where, \( m = \) modulation index \( H = +1 \) for IGBT, \(-1 \) for Diode.
\[ i_{ph} = \sqrt{2} I \sin(\omega t - \phi) \]

Where \( i_{ph} \) = RMS value of the load (output) current, \( \phi \) = Phase angle between load voltage and current.

Then the device current can be written as follows.

\[ I_{device} = \frac{\sqrt{2}}{2} I \sin(\omega t - \phi) \times (1 + H \, \text{rms current}) \]

The average value of the device current over a cycle is calculated as

\[ I_{avg} = \frac{1}{\pi} \int_{0}^{\pi} \frac{\sqrt{2}}{2} I \sin(\omega t - \phi) \times (1 + H \, \text{rms current}) dt \]

\[ = 2I \left[ \frac{1}{2 \pi} + \frac{H}{\pi^2} \cos \phi \right] \]

The device RMS current can be written as

\[ I_{rms} = \sqrt{\int_{0}^{\pi} \left( \frac{\sqrt{2}}{2} I \sin(\omega t - \phi) \right)^2 \times \left( 1 + H \, \text{rms current} \right) dt} \]

\[ = \sqrt{2} I \left[ \frac{1}{4 \pi} + \frac{H}{2 \pi^2} \cos \phi \right] \]

**IGBT Loss Calculation**

IGBT loss can be calculated by the sum of switching loss and conduction loss. Where conduction loss can be calculated by,

\[ P_{con}(IGBT) = V_{ceo} \times I_{avg}(jgb0) \times I_{rms}(jgb0) \times r_{ceo} \]

\[ I_{avg}(jgb0) = \sqrt{2} I \left[ \frac{1}{2 \pi} + \frac{H}{\pi^2} \cos \phi \right] \]

\[ I_{rms}(jgb0) = \sqrt{2} I \left[ \frac{1}{4 \pi} + \frac{H}{2 \pi^2} \cos \phi \right] \]

Values of \( V_{ceo} \) and \( r_{ceo} \) at any junction temperature can be obtained from the output characteristics (Ic vs. Vce) of the IGBT as shown in Fig. 3

![Figure 3: IGBT Output Characteristics](image)

The switching losses are the sum of all turn-on and turn-off energies at the switching events.
Assuming the linear dependence, switching energy

\[ E_{sw} = (a + b I + c I^2) \cdot \frac{V_{DC}}{V_{nom}} \]

Here \( V_{DC} \) is the actual DC-Link voltage and \( V_{nom} \) is the DC-Link Voltage at which \( E_{sw} \) is given. Switching losses are calculated by summing up the switching energies.

\[ P_{sw} = \frac{1}{\nu} \sum_{i} E_{sw}(i) \]

Here ‘\( n \)’ depends on the switching frequency.

\[ P_{sw} = \frac{1}{\nu} \sum_{i} (a + b I + c I^2) \]

\[ = \frac{1}{\nu} \left[ a + \frac{b I}{\nu} + \frac{c I^2}{4} \right] \]

After considering the DC-Link voltage variations switching losses of the IGBT can be written as follows.

\[ P_{\text{SW (IGBT)}} = E_{\text{sw}} \left[ \frac{a}{2} + \frac{b I}{\nu} + \frac{c I^2}{4} \right] \cdot \frac{V_{DC}}{V_{nom}} \]

So, the sum of conduction and switching losses gives the total losses.

\[ R_{\text{f (igbt)}} = P_{\text{es (igbt)}} + P_{\text{sw (igbt)}} \]

**Diode Loss Calculation**

The DIODE switching losses consists of its reverse recovery losses and the turn-on losses are negligible.

\[ E_{\text{es (diode)}} = a + b I + c I^2 \]

\[ P_{\text{sw (diode)}} = E_{\text{sw}} \left[ \frac{a}{2} + \frac{b I}{\nu} + \frac{c I^2}{4} \right] \cdot \frac{V_{DC}}{V_{nom}} \]

So, the sum of conduction and switching losses gives the total diode losses.

\[ P_{\text{f (diode)}} = P_{\text{es (diode)}} + P_{\text{sw (diode)}} \]

The total loss per one switch (IGBT+DIODE) is the sum of one IGBT and DIODE loss.

\[ R_{\text{f}} = P_{\text{f (igbt)}} + P_{\text{f (diode)}} \]

**Thermal Calculations**

The junction temperatures of the IGBT and DIODE are calculated based on the device power losses and thermal resistances. The thermal resistance equivalent circuit for a module is shown in Fig 4. In this design the thermal calculations are started with heat sink temperature as the reference temperature. So, the case temperature from the model can be written as follows.

\[ T_{c} = R_{f} \cdot R_{\text{es (igbt)}} + T_{h} \]
Here $R_{th(c-h)}$ = Thermal resistance between case and heat sink

$P_T =$ Total Power Loss (IGBT+DIODE)

IGBT junction temperature is the sum of the case temperature and temperature raise due to the power losses in the IGBT.

$$T_{j(IGBT)} = R_{th(c-h)} R_{th-j(IGBT)} + T_c$$

DIODE junction temperature is the sum of the case temperature and temperature raise due to the power losses in the DIODE.

$$T_{j(DIODE)} = R_{th(c-h)} R_{th-j(DIODE)} + T_c$$

The above calculations are done based on the average power losses computed over a cycle. So, the corresponding thermal calculation gives the average junction temperatures. In order to make the calculated values close to the actual values, transient temperature values are to be added to the average junction temperatures.

**DC-Capacitor Selection**

The required capacitance for each cell depends on the allowable ripple voltage and the load current. The rms ripple current flowing into the capacitor can be written as follows and the ripple current frequency is double the load current frequency (Novel cascade H-Bridge).

$$I_r = \frac{1}{V_d} \frac{1}{2} (\text{rms current}) \sin(2\omega t)$$

Since the value of ‘L’ is very small, the above equation can be written as below.
\[ I_T = -\frac{1}{V_{dc}} \frac{1}{2} (|U_{ac}| \times \phi \sin(\omega t)) \]

\[ I_T = -\frac{1}{V_{dc}} \frac{1}{2} \left| U_{ac} \right| \sin(\omega t) = -\frac{m}{2} \sin(\omega t) \]

Here ‘\( m \)’ is the modulation index.

Here \( I_T = C \frac{4\phi \omega \Delta V}{2} \sqrt{Z} \).

\[ \frac{m}{2} I \sqrt{Z} = C \frac{4\phi \omega \Delta V}{2} \sqrt{Z} I \]

PHASE SHIFTED CARRIER PWM (PSCPWM), TECHNIQUES FOR CHB INVERTER

Figure 6 shows the PSCPWM. In general, a multilevel inverter with \( m \) voltage levels requires \((m-1)\) triangular carriers. In the PSCPWM, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by \( \phi_{cr} = \frac{3600}{m-1} \).

**Figure 6: Phase Shifted Carrier PWM**

The modulating signal is usually a three-phase sinusoidal wave with adjustable amplitude and frequency. The gate signals are generated by comparing the modulating wave with the carrier waves. It means for five-level inverter, four triangular carriers are needed with a 90° phase displacement between any two adjacent carriers. In this case the phase displacement of \( V_{cr1} = 0^\circ \), \( V_{cr2} = 90^\circ \), \( V_{cr1}^- = 180^\circ \) and \( V_{cr2}^- = 270^\circ \).

SIMULATION RESULTS

**Phase Shifted Carrier PWM (PSCPWM) Five Level CHB MLI Fed BLDC Motor**

The proposed control strategy for the 5 level Cascaded H- Bridge (CHB) multilevel inverter fed BLDC motor with phase shifted PWM modulation technique has developed using Matlab/ Simulink and results are presented.

**Figure 7: Simulation Block of the Phase Shifted Carrier PWM (PSCPWM) 5- Level CHB MLI fed BLDC Motor**
Figure 7 shows the simulink block diagram of 5 level Cascaded H-Bridge (CHB) multilevel inverter fed BLDC motor with phase shifted PWM modulation technique. The behavior of the generated electromagnetic torque is also of vital importance. Fig.8 and Fig.9 show output speed and the generated torque of the 5-level CHB inverter fed BLDC motor.
The stator back-emf for each phase is shown in Fig.10. Fig.11 shows the five levels three phase output voltage of the CHB phase shifted PWM Inverter. FFT analyses of output voltage wave form is shown in Fig. 12 and for this case the THD value is 12.79%.

CONCLUSIONS

Permanent-magnet brushless dc motors is more widely used in high-performance applications because of their higher efficiency, higher torque in low-speed range, high power density, low maintenance and less noise than other motors. In two level inverter there is a problem of harmonics distortion, lower electromagnetic interference, high DC link voltage, high dV/dt, heating of rotor shaft, voltage spikes across the motor terminals etc. The increase in the number of steps of voltage i.e using of multilevel inverter is the solution of the above problem. In this paper, The design of the inverter topology and phase shift pulse width modulating technique are carried out for five level cascade H bridge inverter fed BLDC motor drive and the simulation results are presented for the performance of the motor. The results show that the dynamic performance of the motor is quite satisfactory.

REFERENCES


