Influence of GaN cap on robustness of AlGaN/GaN HEMTs

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Abstract— DC-Step-Stress-Tests of GaN HEMTs have been performed on wafers with and without GaN-cap. The tests consist of a step ramping of drain-source voltage $V_{DS}$ by 5V every two hours at off-state. The irreversible evolution of leakage current starting at a certain drain voltage has been taken as a criterion for the onset of device degradation. It has been stated that there is a stability limit for $V_{DS}$ depending on the epitaxial design. It has been found that wafers with GaN cap show much higher critical voltages as compared to non-capped epitaxial designs. Electroluminescence measurements have been performed to localize defects after DC-Step-Stress-Tests up to 80V for wafer without GaN cap and 120V for wafer with GaN cap.

I. INTRODUCTION

Reliability evaluation studies of AlGaN/GaN HFET devices are currently one of the most important undertakings to provide a rapid industrialisation of this technology. Long [1-3] and short term [4-5] life tests under DC operation conditions have been performed on AlGaN/GaN HEMTs to provide reliability data at the one side and to develop techniques to predict potential reliability problems within a short time frame. The latter aspect motivates us to develop a short-term robustness test based on DC-Step-Stress testing. The intention of this test is to provide a rapid technique to study the robustness as processed devices in order to provide a rapid feed-back to device development and processing.

So far, the main failure modes identified during aging of GaN HFETs result in irreversible changes of for example the drain current $I_{DS}$, the sub-threshold drain current $I_{DS,sub}$, the gate leakage current $I_{G}$, the pinch-off voltage $V_{p}$, the output power $P_{out}$ or the on-state resistance $R_{ON}$. In this paper, we focus on the change of the gate leakage current during on-wafer DC Step-Stress testing as an indicator of degradation. This test is considered as a robustness test which, in comparison to long term aging, gives results in quite a short time. However it has still to be proven, whether there is a direct correlation with long term tests. It has been found that a threshold drain voltage is existing beyond which device starts to degrade. It is defined as the drain voltage where the gate leakage current starts to increase irreversibly (refer to Fig. 2).

The onset of leakage current increase with time is considered as an indicator of a starting degradation in this case. Experimental data revealed that the threshold for degradation is higher if the Al concentration in AlGaN barrier is reduced and/or if a GaN cap design is present [6]. In this paper the performance of devices with and without GaN cap has been compared more intensively and correlated to electroluminescence (EL) measurements performed before, during and after DC-Step-Stress testing. Goal of the EL-measurements is to provide a possible localization of potentially defective device regions and to gain a better physical understanding of relevant degradation mechanisms [7-13].

Different physical mechanisms such as thermionic emission, tunnelling, surface or bulk hoping mechanisms and impact ionization hole currents may explain gate leakage current increase observed during stress testing. The first two mechanisms are related to the properties of the Schottky contact (gate) and its effective barrier on a given epitaxial layer sequence, the latter effects could explain gate leakage caused by surface or bulk defects.

II. EXPERIMENT

A. DC-Step-Stress test

In order to investigate the influence of a GaN cap, we have performed the DC-Step-Stress tests on 2x125μm GaN HEMTs fabricated on wafers without (A) and with (B) an additional GaN cap layer (Si-doped, 5nm, 7x10¹⁹/cm³). The gate length is 0.5μm, gate-to-drain spacing is 6μm and gate-to-source spacing is 1μm. Fig. 1 describes the epitaxial design with GaN cap where $x$ is the Aluminium barrier concentration (%) and $d$ is the barrier thickness. Wafer A and B have 23% and 24% of Al concentration respectively. Both structures have a barrier thickness of 25nm. The average electrical data of both device versions are shown in Table 1 where $I_{DSS}$ is the saturated current at a gate voltage of +1V, $G_{max}$ is the maximum
transconductance, $V_{th}$ is the threshold voltage, and $V_{br}$ the breakdown voltage.

The DC-Step-Stress tests were conducted by increasing the drain-source voltage $V_{DS}$ by 5 V every two hours. The devices were operated at off-state conditions at a gate voltage well below pinch-off ($V_{GS} = -7$ V). The critical voltage $V_{DS deg}$ for a starting degradation is defined as the voltage where the gate current starts to increase irreversibly during an individual step at a respective bias level (marked by an indicator in Fig. 2 and Fig. 3).

### Electroluminescence

Electroluminescence (EL) measurements are known as a useful tool to localize potentially defective regions in the device topology [8]. Electroluminescent emission has initially been studied in GaAs and InP based heterostructure field effect transistors (HFETs) in order to investigate hot electron induced breakdown [9], impact ionization [10] and the conduction-to-conduction band (intra-band) transition of electrons [11]. In AlGaN/GaN HFETs technology EL has also been claimed as a valuable tool to provide a deeper insight in electronic properties of devices. It has been pointed out that the EL is possibly due to the impact ionization in GaN channels [14], hot electron [8, 13] and intra-band transitions [14] EL emission has therefore been proposed as a way to probe the regions of high electric field in a device.

In this work, EL measurements have been performed at the Technical University Berlin using a Hamamatsu Photon Emission Microscope (Phemos 1000). The system is equipped with a liquid nitrogen cooled Si-CCD detector with spectral sensitivity in the visible and near infrared regime. The EL measurements were performed at $V_{DS} = 10$ V, $V_{GS} = -5$ V (off-state) and $V_{GS} = -1$ V (on-state).

Measurements of IV-characteristics and EL have been performed before (EL1), during and after device stressing (EL2, EL3) as indicated in Fig. 2 and Fig. 3. For wafer A, the epi design without GaN cap, EL2 and EL3 measurements were performed after stressing up to drain voltage $V_{DS}$ of 50 V and 80 V respectively. The EL2 and EL3 measurements of wafer B, epi design with GaN cap, were performed after stressing up to higher drain voltage $V_{DS}$ of 60 V and 120 V since both gate leakage $I_{GS}$ and subthreshold drain current $I_{DS}$ are much smaller than wafer A.

![Figure 1. Standard epitaxial design with GaN cap.](image1)

![Figure 2. A typical DC-Step-Stress test graph of wafer A (without GaN cap) at off-state bias conditions (gate voltage $V_{GS} = -7$ V). The red lines depict the drain voltage $V_{DS}$ over time. The blue and black lines describe the gate leakage current $I_G$ and drain current $I_{DS}$ respectively. According to our definition the degradation starts at $V_{DS} = 30$ V (see the magnification in the inset). EL measurements were performed before (EL1), during (stressing up to 50 V $\Rightarrow$ EL2) and after stress test up to 80 V (EL3).](image2)

![Figure 3. A typical DC-Step-Stress test graph of wafer B (with GaN cap) at off-state bias conditions (gate voltage $V_{GS} = -7$ V). The red lines depict the drain voltage $V_{DS}$ over time. The blue and black lines describe the gate leakage current $I_G$ and drain current $I_{DS}$ respectively. According to our definition the degradation starts at $V_{DS} = 30$ V (see the magnification in the inset). EL measurements were performed before (EL1), during (stressing up to 50 V $\Rightarrow$ EL2) and after stress test up to 80 V (EL3).](image3)

### Table 1. Selected Parameters of Wafers.

<table>
<thead>
<tr>
<th>GaN cap</th>
<th>$I_{DS}$ (mA/mm)</th>
<th>$g_m$ (mS/mm)</th>
<th>$V_{th}$ (V)</th>
<th>$V_{br} \pm \sigma$ (V)</th>
<th>$V_{DS deg}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1073 ± 68</td>
<td>240 ± 10</td>
<td>-3.35 ± 0.13</td>
<td>42 ± 3</td>
<td>20 – 30</td>
</tr>
<tr>
<td>B</td>
<td>901 ± 38</td>
<td>233 ± 10</td>
<td>-2.42 ± 0.23</td>
<td>105 ± 9</td>
<td>55 – 65</td>
</tr>
</tbody>
</table>

The DC-Step-Stress tests were conducted by increasing the drain-source voltage $V_{DS}$ by 5 V every two hours. The devices were operated at off-state conditions at a gate voltage well below pinch-off ($V_{GS} = -7$ V). The critical voltage $V_{DS deg}$ for a starting degradation is defined as the voltage where the gate current starts to increase irreversibly during an individual step at a respective bias level (marked by an indicator in Fig. 2 and Fig. 3).
III. RESULTS AND DISCUSSION

A. Step-Stress Test

Fig. 2 shows a typical gate leakage current during Step-Stress-Test for an epitaxial design without GaN cap (device A). Initially a recovery of the gate leakage current takes place after every increase of drain voltage. This might be due to the population of trap states in the vicinity of the gate. However, exceeding a certain threshold voltage, the gate leakage does not recover any more within one step period but starts to increase irreversibly. The onset of irreversible gate leakage degradation is marked in Figs. 2 and 3. We refer to it as the threshold of irreversibly. The onset of irreversible gate leakage degradation does not recover any more within one step period but starts to increase irreversibly. The onset of irreversible gate leakage degradation is marked in Figs. 2 and 3. We refer to it as the threshold of irreversibly. The onset of irreversible gate leakage degradation does not recover any more within one step period but starts to increase irreversibly.

The sub-threshold drain current of devices A starts to increase significantly if the drain voltage exceeds about 30V. This effect is more pronounced as the drain voltage increases further. We believe that this behaviour is related to the punch-through effect at higher voltage [15]. Any further step-wise increase of the drain voltage provokes a corresponding increase of the sub-threshold current. Within one step the drain current decreases exponentially. This could be an indication of trap charging at these conditions. The higher the drain voltage, the higher the sub-threshold drain leakage current. Electrons that are injected into the GaN buffer can then start to occupy trap levels there and thus reduce the available carrier density in the channel. The occupation of slow traps results in the observed exponential decay of the sub-threshold drain leakage current during one step period.

The IV-characteristics of both devices showed a slight knee walk-out after the first irreversible degradation of the gate leakage has been detected (see Figs. 4 and 5). More detailed investigations revealed that the knee walk-out and the reduction of the sub-threshold drain voltage is due to burn-in in the first few hours of device operation. Obviously the irreversible built-up of leakage current does not yet significantly degrade the DC-IV characteristics in addition to the burn-in. Of course dispersion measurements have to be carried out in order to study possible changes in the dynamic behaviour.

If device step stressing continues up to higher voltages a reversible knee walk-out has been detected. This is visualized especially in Fig. 5 for the capped device which has been stressed up to 120V. In this case a significant knee walk out was observed initially. However, keeping the device un-biased for a few hours the knee walk-out practically recovers to the value observed after first stressing (see green asterisks in Fig 5). This indicates that high voltage biasing resulted in reversible charging of trap states most probably in the buffer of the device. Similarly, the drain current for both devices decreases initially after higher voltage stressing and falls back more or less to the first stressed test values during non-biasing for a couple of hours (device A to values of stress up to 50V and device B to values of stress up to 60V).

In order to get some understanding in what might be the reason of this behaviour, simulations of the electrical field distribution in capped and non-capped structures have been performed. They show that capping shields the AlGaN layer in the vicinity of the gate from excessive electrical field (see Fig. 6). Since the electrical field in the AlGaN regions close to the GaN cap is more than a factor of two smaller as compared to a similar position in the non-capped AlGaN region, the field stressing of this area is significantly reduced. This finding could support a degradation model based on AlGaN relaxation in the high field regions due the inverse piezoelectric effect as first described by Joh et al. [5]. High values of the electrical field in the AlGaN layer could cause a local relaxation of the AlGaN and consequently provide a leakage path for electrons to the channel. Since the absolute values of the electrical field...
in the AlGaN are higher for non-capped devices our findings could probably be explained by this mechanism.

Joh et al. [5] in deed showed similar results based on step ramping tests of the gate-drain voltage $V_{GD}$ and pointed out that this kind of degradation may be due to additional tensile strain built-up at the drain side of the gate contact due to the inverse piezoelectric field. Critical voltages $V_{crit}$ of 25-30V for epitaxial designs comparable to the device without GaN cap had been described. They explained the increasing gate leakage by the onset of hopping conductivity along defects near the drain side gate edge which are created by a local relaxation of the AlGaN barrier layer in the high field regions (∼7MV/cm) close to the gate edge. Therefore the magnitude of the electric field in AlGaN layer is a decisive quantity.

**B. Electroluminescence**

EL measurements were carried before Step-Stressing and after electrical failure detection (irreversible gate leakage increase). Measurements taken at off-state and on-state conditions are compared to each other (see Figs. 7 and 8). EL measurements of non-stressed devices taken at off-state always show some bright spots which are more obvious for device B. Generally at off-state conditions the EL images show a more pronounced inhomogeneous behaviour as compared the on-state conditions. It is estimated that the bright spots result from localized inhomogeneities along the transistor which become dominant at off-state conditions. The spots could be due to micro roughness, defect clusters or also process imperfections. Those bright spots become more pronounced, show a tendency to coalesce and to increase in number after first and second stress. As indicated in Figs. 9 and 10 this is accompanied by an increase of the total EL-intensity in the sub-threshold region. It seems that this increase of sub-threshold EL-intensity is roughly correlated to the increasing sub-threshold drain current during stress testing.

The spotty behaviour of EL at off state has been observed by Chen et al. [12]. They showed that the bright spots can be related to point defects which may be associated with the existence of donor acceptor pairs. A dipole configuration of point defect acts as a potential well which can trap some electrons. Nevertheless, those bright spots are interesting to be further investigated by spectral distribution analysis as they could also inform some degradation/defect spots after stress which needs to be cross sectional examined by FIB and/or TEM analysis.

In contrast, at on-state conditions the EL-images show much more homogeneous properties (Figs. 7 and 8), the EL
We have developed on-wafer Step-Stress-Tests as a fast device robustness screening method. The method uses irreversible leakage current increase as an indicator to determine the critical voltage for device degradation in dependence on epitaxial layer designs for example. It has been found out that robustness significantly depends on epitaxial layer designs. For example epitaxial design with 23% Al in the barrier layer without GaN cap shows a threshold voltage for degradation of only 20-30V, whereas the same structures with doped GaN cap shows significantly higher threshold values of around 55-65V. After degradation the integral intensity of the EL-signal for devices biased at off state conditions always increases whereas the opposite is true for devices biased at on state conditions during EL measurements. Generally degraded devices show a larger number of individual EL spots at off-state conditions. These spots need to be further investigated for example by cross sectional FIB and/or TEM analysis in order to explain the appropriate degradation mechanism.

IV. CONCLUSION

We have developed on-wafer Step-Stress-Tests as a fast device robustness screening method. The method uses irreversible leakage current increase as an indicator to determine the critical voltage for device degradation in dependence on epitaxial layer designs for example. It has been found out that robustness significantly depends on epitaxial layer designs. For example epitaxial design with 23% Al in the barrier layer without GaN cap shows a threshold voltage for degradation of only 20-30V, whereas the same structures with doped GaN cap shows significantly higher threshold values of around 55-65V. After degradation the integral intensity of the EL-signal for devices biased at off state conditions always increases whereas the opposite is true for devices biased at on state conditions during EL measurements. Generally degraded devices show a larger number of individual EL spots at off-state conditions. These spots need to be further investigated for example by cross sectional FIB and/or TEM analysis in order to explain the appropriate degradation mechanism.

REFERENCES