A TOPOLOGY-BASED METHOD FOR IDENTIFYING FLIP-FLOP GRAPHS IN BJT CIRCUITS

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ABSTRACT

This paper presents a method focussed on finding embedded flip-flop graphs in the circuit topology. The method is based on performing a tearing of the graph of the dead network. It is implemented in a methodological way by applying a series of graph operations. The method is applied to networks containing BJTs, independent current and voltage sources, and positive linear resistors but it can be easily modified to cope with other kinds of active devices.

1. INTRODUCTION

The complete solution to the general dc problem of nonlinear circuits focusses on the next aspects [1]: determining whether or not the uniqueness of the dc solution is guaranteed, establishing an upper bond on the number of dc solutions, and as last step calculating all of them, as well as determining their conditions for stability.

In [2, 3], a topological method have been proposed in order to solve the problem of determining the uniqueness of the dc operating point of nonlinear resistive networks.

It is well-known that multiple dc operating points are due to the presence of a flip-flop alike structure embedded in the circuit [1, 4], as shown in figure 1.

![Figure 1: A flip-flop alike structure.](image)

As it is well known [5, 6], many algorithms dealing with graphs manipulations have a complete exponential complexity. The search for such a flip-flop alike structure is also a complete exponential problem. The tearing introduced herein allows us to achieve a dramatic reduction in the computation time.

2. FINDING THE FLIP-FLOPS

The aim of the method is to find a topological equivalent of the figure 1 in terms of the paths\(^1\) between transistor terminals as sketched in the figure 2. The topological equivalent is obtained via the dead graph\(^2\) of the circuit. Therefore, the existence of a flip-flop structure is coupled to the existence of the paths \(L_{C_iB_j}, L_{B_iC_j}\) and \(L_{E_iE_j}\).

![Figure 2: Path-equivalent of the feedback structure.](image)

2.1. Paths between terminals

However, not only do the paths sketched above result to be present for any transistor-pair, but also paths between the other terminals must be taken into account. In fact, all possible paths are directly related to the interconnection pattern of linear part of the circuit. The paths can be classified as follows:

\(^1\)A path is a subgraph in which all vertices have degree 2, except the first and the last vertices, that have degree 1.

\(^2\)A dead graph is the graph obtained by eliminating all independent sources, i.e. those branches of voltage sources (resp. current sources) are transformed into short circuits (resp. open circuits).

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**Path of a single transistor**

Two basic paths are joining involved for a single transistor, namely the collector-base path ($L_{Cj,Bi}$) and the base-emitter path ($L_{Bj,El}$).

![Figure 3: Set of paths between terminals.](image)

This concept is graphically depicted in figure 3, where each transistor junction shows assigned a circle representing the set of paths. A third path can be obtained as follows:

$$L_{Cj,Ei} = L_{Cj,Bi} \oplus L_{Bj,Ei}$$  \hspace{1cm} (1)

where the symbol $\oplus$ denotes the ring sum operation.

**Paths between two transistors**

It clearly results that for two transistors, the paths above must be considered twice (see figure 4). The next relations hold for the paths leaving from every terminal of the $i$-th transistor reaching the $j$-th transistor:

**Initial Node $C_i$**

- $L_{Cj,Ci} = L_{Cj,Ei} \oplus L_{Ej,Ci} = L_{Cj,Ei} \oplus L_{Ej,Ci}$
- $L_{Cj,Bi} = L_{Cj,Ei} \oplus L_{Ej,Bi} = L_{Cj,Ei} \oplus L_{Ej,Bi}$
- $L_{Cj,Ei} = L_{Cj,Ei} \oplus L_{Ej,Ei} = L_{Cj,Ei} \oplus L_{Cj,Ei}$

**Initial Node $B_i$**

- $L_{Bj,Ci} = L_{Bj,Ei} \oplus L_{Ej,Ci} = L_{Bj,Ei} \oplus L_{Ej,Ci}$
- $L_{Bj,Bi} = L_{Bj,Ei} \oplus L_{Ej,Bi} = L_{Bj,Ei} \oplus L_{Bj,Bi}$
- $L_{Bj,Ei} = L_{Bj,Ci} \oplus L_{Cj,Ei} = L_{Bj,Ci} \oplus L_{Cj,Ei}$

**Initial Node $E_i$**

- $L_{Ej,Ci} = L_{Ej,Ei} \oplus L_{Ej,Ci} = L_{Ej,Ei} \oplus L_{Ej,Ci}$
- $L_{Ej,Bi} = L_{Ej,Ci} \oplus L_{Cj,Bi} = L_{Ej,Ci} \oplus L_{Cj,Bi}$
- $L_{Ej,Ei} = L_{Ej,Bi} \oplus L_{Bj,Ei} = L_{Ej,Bi} \oplus L_{Bj,Ei}$

These paths denote in fact the interconnections between both transistors, that occur through the linear part of the network.

![Figure 4: Set of paths between $Q_i$ and $Q_j$.](image)

**3. PATHS MATRICES**

The paths above can be recast in a rectangular array, such as a matrix. The paths-matrix is a square matrix whose columns and rows are transistor nodes belonging to the dead graph. The $i$-th column and $i$-th row of the matrix are occupied by the same node.

The resulting matrix ($M_Q$) is used in order to identify the paths that indeed define the interconnection pattern of the linear part of the network. This concept is shown in the figure 5.

Because a triad of nodes is associated with a single transistor, viz. emitter, base, and collector nodes, the resulting dimension of this matrix is $3Q \times 3Q$, where $Q$ is the total number of transistors, as it is shown in the figure 5.

![Figure 5: The $M_Q$ matrix of paths.](image)

In the following, the matrix $M_Q$ is analyzed according with its structure.

Submatrices on the main diagonal

Every matrix on the main diagonal is associated with a single transistor, it has the following expression:

$$M_{i,i} = \begin{bmatrix}
\varnothing & L_{Cj,Bi} & L_{Cj,Ei} \\
L_{Bj,Ci} & \varnothing & L_{Bj,Ei} \\
L_{Ej,Ci} & L_{Ej,Bi} & \varnothing
\end{bmatrix}$$

where $L_{Cj,Bi}$ are the sets of paths between collector and base of the $i$-th transistor, $L_{Cj,Ei}$ are the sets of paths between...
collector and emitter of the \(i\)-th transistor, and \(L_{B,E}\) are the sets of paths between base and emitter of the \(i\)-th transistor. Besides, the entries on the main diagonal are empty sets, i.e. no self-loops are allowed to be connected at any transistor terminal. It clearly results that \(L_{C,B} = L_{B,C}, L_{C,E} = L_{E,C}\), and \(L_{B,E} = L_{E,B}\), because the graph of the circuit is considered to be an undirected graph.

Submatrices off the main diagonal

These matrices represent the sets of paths concerning a pair of transistors, namely transistor \(i\) and transistor \(j\), i.e.:

\[
M_{ij} = \begin{bmatrix}
L_{C_i,C_j} & L_{C_i,B_j} & L_{C_i,E_j} \\
L_{B_i,C_j} & L_{B_i,B_j} & L_{B_i,E_j} \\
L_{E_i,C_j} & L_{E_i,B_j} & L_{E_i,E_j}
\end{bmatrix}
\]

where \(L_{C_i,C_j}\) are the sets of paths between the \(i\)-th collector and \(j\)-th collector, \(L_{C_i,B_j}\) are the sets of paths between the \(i\)-th collector and \(j\)-th base, \(L_{C_i,E_j}\) are the sets of paths between the \(i\)-th collector and \(j\)-th emitter, \(L_{B_i,C_j}\) are the sets of paths between the \(i\)-th collector and \(j\)-th base, \(L_{B_i,B_j}\) are the sets of paths between the \(i\)-th collector and \(j\)-th emitter, \(L_{B_i,E_j}\) are the sets of paths between the \(i\)-th collector and \(j\)-th base, \(L_{B_i,E_j}\) are the sets of paths between the \(i\)-th collector and \(j\)-th emitter, \(L_{E_i,C_j}\) are the sets of paths between the \(i\)-th base and \(j\)-th base, \(L_{E_i,B_j}\) are the sets of paths between the \(i\)-th base and \(j\)-th base, \(L_{E_i,E_j}\) are the sets of paths between the \(i\)-th base and \(j\)-th base. Besides, the structure of \(M_Q\) yields \(M_{ij} = M_{ji}^T\).

In order to obtain a such structure such as given in the figure 1, it becomes necessary to search for the paths depicted on figure 2. This is given through the next result:

**Theorem 1** A flip-flop structure is found embedded in the circuit if the paths \(L_{C,B}, L_{B,C}, L_{E,E}\) fulfill:

\[
\begin{align*}
L_{C,B} \cap L_{B,C} &= \emptyset \\
L_{C,B} \cap L_{E,E} &= \emptyset \\
L_{B,C} \cap L_{E,E} &= \emptyset
\end{align*}
\]

The problem of finding the subgraph of the embedded flip-flop in the original graph can be easily solved by resorting to the paths connecting the terminals between transistor pairs.

**4. TEARING PROCEDURE**

In order to speed-up the search for the flip-flop structure, a tearing procedure has been devised. The tearing has as aim to separate the original graph into two subgraphs \(G_{L_1}\) and \(G_{L_2}\), and a hinge subgraph \(G_y\), which allow us to generate two subgraphs, namely:

\[
G_1 = G_{L_1} \cup G_y \quad \text{and} \quad G_2 = G_{L_2} \cup G_y.
\]

The hinge subgraph can have any of the following forms:

- A single subgraph, i.e. a single vertex or a single branch
- A composed subgraph \(G_y = G_y(E_y, V_y)\) where \(E_y\) is the set of branches and \(V_y\) is the set of vertices of \(G_y\), respectively. The figure 6, shows this concept.

![Figure 6: Tearing of cactus graphs.](image)

**5. OUTLINE OF THE ALGORITHM**

The algorithm can be recast in the next steps:

1. Obtain the dead graph.
2. Form the paths matrix.
3. Find the paths mentioned in the Theorem 1 that interconnects the first pair of transistors.
4. Verify that the Theorem 1 is fulfilled.
5. If the previous step is true then continue with the next step. In other case, take the next pair of transistors and return to the step 4.
6. Induce the subgraph that contains the flip-flop structure to \(G_1\).
7. Induce the subgraph remaining outside \(G_1\), i.e. \(G_2\).
8. Obtain the subgraph \(G_y\) with the intersection between \(G_1\) and \(G_2\).
9. Repeat the whole procedure (if possible) to \(G_2\).
6. EXAMPLE

The circuit shown in the figure 7 will be used to illustrate the method. The circuit is actually composed by two Schmitt-triggers interconnected by an amplifier stage. However, from its graph (figure 8), it is quite difficult to notice the existence of an embedded flip-flop subgraph.

![Figure 7: Test circuit.](image)

![Figure 8: Original graph.](image)

The application of the method allows us to obtain firstly the subgraph shown in the figure 9, i.e. transistors $Q_1$ and $Q_2$ form a flip-flop structure. In an ulterior step, the algorithm is applied to the remaining graph which yields a second flip-flop, namely, transistors $Q_3$ and $Q_4$ form a structure such as given in figure 1. This subgraph is shown in the figure 10.

The presence of two flip-flop alike structures allows us to assure that the uniqueness of the dc solution of the circuit is not guaranteed.

7. CONCLUSIONS

The present work allows us to find the embedded flip-flop subgraphs in the circuit. It resorts to concepts of graph theory in order to form a matrix containing the information on the topological paths within the circuit. The algorithm is used to assess the uniqueness of the dc solution for circuits with more than two transistors.

8. REFERENCES


