Abstract—The quantum definition based threshold voltage has been evaluated for triple-gate (TG) SOI FinFETs using self-consistent Schrödinger-Poisson solver. Although a new quantum definition of threshold voltage for multiple gate SOI MOSFETs has been provided in recent literature, in-depth analysis of quantization effects on threshold voltage calculation for highly scaled TG FinFETs is yet to be done. In this paper, the electrostatics of the device has been explored from a quantum mechanical point of view for variation in silicon film thickness in the sub 10nm regime. Also the self-consistent solver, which takes wave function penetration and other quantum mechanical (QM) effects into account, has been utilized here to establish the capacitance-voltage (C-V) characteristics and a modified approach has been proposed for threshold voltage calculation.

I. INTRODUCTION

Silicon-On-Insulator (SOI) and multiple gate devices like double gate FinFETs, tri-gate, pi-gate, omega-gate and gate-all-around (GAA) MOSFETs offer excellent electrostatic control required for 25nm gate lengths as foreseen by International Technology Roadmap for Semiconductors [1]. Among these multiple gate SOI MOSFETs (MugFETs), the tri-gate structure is being considered as a prospective alternative to single gate MOSFETs as it offers prolonged life of Si CMOS beyond the limits of classical scaling [2]. Calculation of threshold voltage, which is a fundamental parameter in device characterization and modeling [3], is an important step towards having an in depth understanding of the electrostatics and dynamic behavior of this novel device. A number of methods have been proposed towards the calculation of threshold voltage in MOS devices [4]-[8]. As device dimensions go below the sub 10nm region, which is called for by the ITRS, QM effects become pronounced [9]. Accurate calculation of threshold voltage in such nanoscale devices requires the consideration of QM effects. A quantum definition of threshold voltage has been proposed by Yun et al. that takes into account the quantum effects [10]. But detailed analysis of how this method of calculating threshold voltage can be applicable for a wide range of device family is not presented. The method proposed in [11] for the calculation of threshold voltage in double gate devices has been modified in [12] for multigate devices using a fitting parameter. There are scopes of modifications in the model proposed in [12] if the quantum mechanical definition of threshold voltage is taken into consideration.

II. SIMULATOR MODEL

In this paper, we calculate the quantum definition based threshold voltage of TG FinFETs for different silicon film widths. Self consistent simulation using coupled Schrödinger-Poisson solver has been carried out taking wave function penetration and other quantum mechanical (QM) effects into account. For the first time, the self-consistently calculated capacitance value has been utilized in the calculation of threshold voltage of TG FinFET. Also detailed analysis has been carried out to explore the correlation between threshold voltage and QM effects in nanoscale TG SOI FinFETs.
At threshold voltage, the curve shows a distinct transition point which signifies the start of inversion channel buildup at a high rate.

The charge calculation for this device geometry is based on self-consistent solution of coupled Poisson and Schrödinger equation [2]. In order to incorporate wave function penetration effects, open boundary condition is considered at Si/SiO$_2$ interface. At the end of convergence of the self-consistent solver, the total electron concentration per unit width ($N$) is obtained using

$$N = \int \int_{A_{si}} n(x, y) \, dx \, dy \quad (cm^{-1})$$  \hspace{1cm} (2)

Differentiating $N$ with respect to ($V_{gb}$) gives the capacitance which is divided by gate length to obtain the gate capacitance per unit area.

In the particular case of Multigate MOSFETs, a relationship between physical device parameters and threshold voltage is given by [12]:

$$V_{th} = \Phi_{ms} + n \frac{kT}{q} \ln \left( \frac{2C_{ox}kT}{q^2ni_{si}} \right) + \frac{\hbar^2 \pi^2}{2m_{ds} W_{si}^2}$$  \hspace{1cm} (3)

This can be simplified to,

$$V_{th} = \Phi_{ms} + \Phi_{inv} + E_{G1}$$  \hspace{1cm} (4)

Here, $\Phi_{ms}$ is the metal to semiconductor work function difference, which is equal to $-0.8eV$ in our simulations. The second term, denoted by $\Phi_{inv}$, accounts for the voltage needed to build up inversion carrier concentration at the threshold. It is a classical term which varies inversely with silicon film thickness ($t_{si}$). The fitting parameter ($n$) varies depending on the device geometry. The modification in the equation comes from the substitution of the fixed oxide capacitance ($C_{ox}$) by the inversion capacitance ($C_{inv}$) obtained using self-consistent analysis.

The third term of the equation, $E_{G1}$ is the lowest subband energy above conduction band minima. It is a quantum mechanical term which varies depending on the splitting of the conduction band energy level into subbands. The value of $E_{G1}$ in TG FinFETs is twice the value obtained for Double gate FinFETs [10]. This modification is valid according to the equation for calculating $V_{th}$ given in literature [11].

In our study, we calculated the threshold voltage of TG FinFETs having different fin widths using the method in literature [10] and afterwards obtained the values of the fitting parameter of Eq. (3). TG FinFETs with square silicon films

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**Fig. 2.** Electron concentration profile at $V_{gb} = V_{th}$ for four different geometries.
having doping density of $5 \times 10^{17} \text{cm}^{-3}$ have been considered. The gate oxide thickness and gate length have been kept fixed at 1nm and 15nm respectively. The work function of the gate metal used is 3.25eV. The contribution of the classical and quantum mechanical terms on threshold voltage has been studied with the variation of silicon film thickness.

III. SIMULATION RESULTS

Silicon film thickness or fin width, which has a profound impact on the threshold voltage of MuGFETs, is one of the most important process parameters of TG FinFET [10] and [12]. In our simulations, $t_{si}$ in the range of 2 nm to 15 nm has been considered. In Fig. 2a, 2b, 2c and 2d the charge profiles of the devices are shown at $V_{gb} = V_{th}$. It has been reported earlier that multiple gate structures show non planar silicon/gate oxide interface with corners [13]. The corner charge accumulation influences the device parameters like threshold voltage and sub threshold slope. It can be observed from the charge profiles that when film dimension is reduced from 15 nm to 6 nm, the ratio of peak electron concentration near the corners to the minimum concentration near the center of the fin, as well as $n_{peak}$ to $n_{average}$ ratio increases. This is because of the increased confinement at the corners and sidewalls of the film when device dimensions are reduced. When device dimension is further reduced, as it is the case of the TG having $t_{si}$ of 2 nm, the inversion layers are no longer localized at the surfaces but can be found at the center of the film giving rise to volume inversion (Fig. 2a). This phenomenon has a significant effect on the threshold voltage for device dimensions in the subnanometer regime.

From the band diagrams shown in Fig. 3, it is obvious that potential wells narrow down with decreased device dimensions. This in effect results the increased quantum confinement of electrons and also causes the increase in splitting of energy levels into subbands. Quantum mechanical effects resulting from this increased quantum confinement has a pronounced effect on $V_{th}$. Based on the quantum definition of $V_{th}$ [10], $\frac{n_{peak}}{n_{average}}$ ratio vs. gate voltage ($V_{gb}$) variation curves are used to extract these threshold voltages (Fig. 4). It is obvious from the curves that the threshold voltage point has a significant effect on the charge profile of the devices. The threshold voltages extracted from Fig. 4 have been used to demonstrate the dependence of $V_{th}$ on $t_{si}$ (Fig. 5). As expected, the threshold voltage increases considerably with the decrease of silicon film width indicating the requirement of extra amount of charge for inversion channel buildup in low-dimension devices.

In Fig. 6, the C-V characteristics of the simulated devices indicate that the rate of charge buildup is enhanced by the increase of fin width. The value of the inversion capacitances can be extracted from this figure for different gate voltages. The use of this self-consistently obtained capacitive values certainly gives better approximate than the use of fixed oxide capacitance in (3). In [11], Eq. (3) has been proposed to calculate threshold voltage of Double gate FinFETs with fitting parameter $n$ equal to unity. In this equation, the term $\Phi_{inv}$ containing $n$ is a measurement of the inversion charge needed to reach threshold point for a device. Extracting the threshold voltage for different fin widths of TG FinFETs using the method described earlier, the values of $n$ are obtained with respect to fin width (Fig. 7).
An effect of scaling in silicon film thickness on TG FinFETs can be observed from Fig. 8. In this figure, the variation of $V_{th}$, $\Phi_{inv}$ and $E_{G1}$ are shown with respect to film thickness. As the devices are scaled down from $15\text{nm}$ to $6\text{nm}$, the value of $n$ as well as $\Phi_{inv}$ increases accordingly which results in increase of $V_{th}$. Moreover, as scaling continues from $6\text{nm}$ to $2\text{nm}$, the contribution of $\Phi_{inv}$ on $V_{th}$ changes drastically. In this region, the value of $n$ as well as $\Phi_{inv}$ drops sharply indicating the prominent effect of quantum mechanical term $E_{G1}$ on $V_{th}$. Certainly threshold voltage in this level of scaling shows strong dependence on quantum mechanical effects. This profound impact of quantum confinement in low dimensional devices has been demonstrated earlier in this paper. Thus calculation of threshold voltage of TG FinFETs using the novel approach in literature [10] manifests the quantum mechanical effects comprehensively.

**IV. CONCLUSION**

Detailed analysis has been carried out to examine the significance of QM effects in the calculation of threshold voltage of nanoscale TG devices. An important modification is the substitution of the conventionally used gate oxide capacitance by the self-consistently computed inversion capacitance, which results in a more accurate assessment of threshold voltage. Simulation results demonstrate that increased QM effects with continued device scaling would necessitate increased voltage for the onset of inversion channel buildup. Proper estimation of this voltage i.e. the threshold voltage, demands for comprehensive incorporation of QM effects, which has been the focus of our study in this literature.
REFERENCES


