VLSI Design and Implementation of Low Power MAC Unit with Block Enabling Technique

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Abstract— In the majority of digital signal processing (DSP) applications the critical operations are the multiplication and accumulation. Real-time signal processing requires high speed And high throughput Multiplier-Accumulator (MAC) unit that consumes low power, which is always a key to achieve a high performance digital signal processing system. The purpose of this work is, design and implementation of a low power MAC unit with block enabling technique to save power. Firstly, a 1-bit MAC unit is designed, with appropriate geometries that give optimized power, area and delay. The delay in the pipeline stages in the MAC unit is estimated based on which a control unit is designed to control the data flow between the MAC blocks for low power. Similarly, the N-bit MAC unit is designed and controlled for low power using a control logic that enables the pipelined stages at appropriate time. The adder cell designed has advantage of high operational speed, small transistor count and low power. The MAC is implemented on a 0.18um CMOS technology using CADENCE tool. This paper also investigates on various architectures of multipliers and adders also on the various techniques to reduce power consumption which are suitable for implementation of high throughput signal processing and at the same time to achieve low power consumption. The whole MAC chip is operated at 125 MHz using 1.8 V power supply. The power is reduced by 11.28% using the block enabling technique compared to the normal design.

Keywords— **Low Power, MAC, clock gating, block enable, multiplier.**

1. Introduction

Digital Signal Processing (DSP) is used in a wide range of applications such as speech and audio coding, image processing and video, pattern recognition, sonar and so on. In real time Very Large Scale Integration (VLSI) implementation of the DSP instruction, the system requires hardware architecture which can process input signals. Most of the DSP computation involves the use of multiply and accumulate operations and therefore Multiplier Accumulator (MAC) unit is very important in DSP applications. In the last few years, the main consideration of MAC design is to enhance its speed. This is because , speed and throughput rate is always the concern of digital signal processing system. But for the epoch of personal communication, low power design also becomes another main design consideration. This is because, battery energy available for these portable products limits the power consumption of the system. Therefore, the main motivation of this work is to investigate various pipelined multiplier/accumulator architectures and circuit design techniques which are suitable for implementing high throughput signal processing algorithms and at the same time achieve low power consumption. A conventional MAC unit consists of (fast multiplier) multiplier and an accumulator that contains the sum of the previous consecutive products. The function of the MAC unit is given by the following equation:

$$F = \Sigma A_i B_i$$

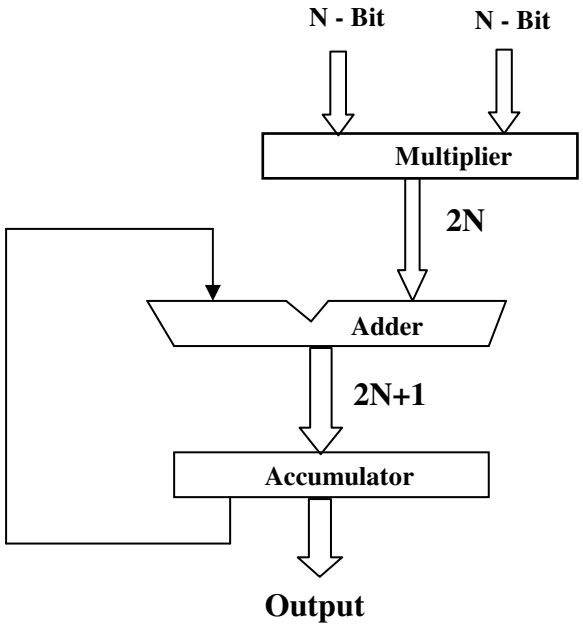

Fig 1: Basic structure of MAC

The main goal of a DSP processor design is to enhance the speed of the MAC unit, and at the same time limit the power consumption In a pipelined MAC circuit, the delay of pipeline stage is the delay of a 1-bit full adder (Jou, Chen, Yang and Su, 1995) .Estimating this delay will assist in identifying the overall delay of the pipelined MAC. In this work, 1-bit full adder is designed. Area, power and delay are calculated for the full adder, based on which the pipelined MAC unit is designed for low power.

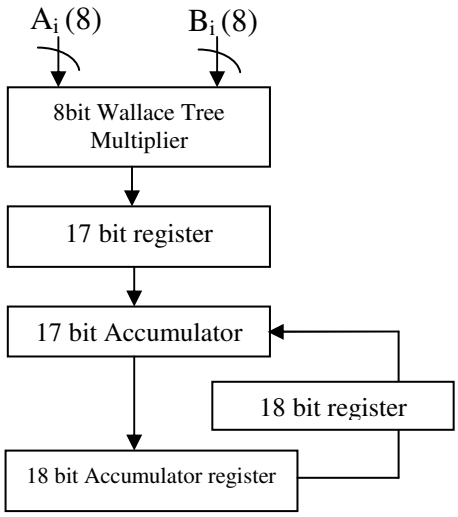

Fig 2: MAC architecture

2. Multiplier and Accumulator Unit

MAC is composed of an adder, multiplier and an accumulator. Usually adders implemented are Carry-Select or Carry-Save adders, as speed is of utmost importance in DSP (Chandrakasan, Sheng &Brodersen, 1992 and Weste & Harris, 3rd Ed). One implementation of the multiplier could be as a parallel array multiplier. The inputs for the MAC are to be fetched from memory location and fed to the multiplier block of the MAC, which will perform multiplication and give the result to adder which will accumulate the result and then will store the result into a memory location. This entire process is to be achieved in a single clock cycle (Weste & Harris, 3rd Ed). Figure 2 is the architecture of the MAC unit which had been designed in this work. The design consists of one 17 bit register, one 8-bit Wallace tree multiplier, 17-bit accumulator using ripple carry and two18-bit accumulator registers. To multiply the values of A and B, Wallace tree multiplier is used instead of conventional multiplier because Wallace tree multiplier can increase the MAC unit design speed. Ripple Carry Adder (RCA) is used as an accumulator in this design. Apparently, together with the utilization of Wallace tree multiplier approach, carry save adder in the final stage of the Wallace tree multiplier and Ripple Carry adder as the accumulator, this MAC unit design is not only reducing the standby power consumption but also can enhance the MAC unit speed so as to gain better system performance. The operation of the designed MAC unit is as in Equation 2.1. The product of Ai X Bi is always fed back into the 17-bit Ripple Carry accumulator and then added again with the next product Ai x Bi. This MAC unit is capable of multiplying and adding with previous product consecutively up to as many as eight times.

Operation: Output = Σ Ai Bi

In this paper, the design of 8x8 multiplier unit is carried out that can perform accumulation on 17 bit number. This MAC unit has 18 bit output and its operation is to add repeatedly the multiplication results. The total design area is also being inspected by observing the total count of transistors. Power delay product is calculated by multiplying the power consumption result with the time delay.

2.1 Wallace tree Multiplier

The design analysis starts with the analysis of elementary algorithm for multiplication by Wallace tree multiplier. Figure 6 shows the algorithm for 8 x 8 bits multiplication performed by Wallace tree multiplier. There are five stages to go through, to complete the multiplication process (Weste & Harris, 3rd Ed). Each stage used half adders and full adders that are denoted by the red circle for the 1bit half adder and the blue circle for the 1 bit full adder. Firstly, we had to reduce the partial products using the

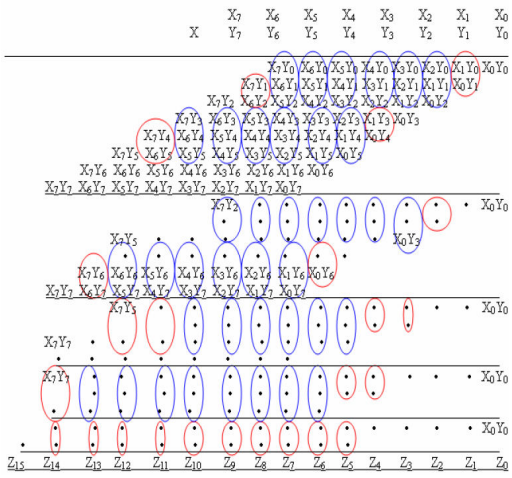

Fig 3: Algorithm for 8 bits x 8 bits Wallace tree multiplier (Harun, 2007)

half adders and full adders that are combined to build a carry save adder (CSA) until there were just two rows of partial products left. Next, we add remaining two rows by using a fast carry propagate adder. In this project, CSA (carry save adder) using ripple carry adder is used to get the final product. Secondly, the schematic of the conventional 8 bits x 8bits high speed Wallace tree multiplier is designed by referring to the algorithm.

2.2 Ways of Reducing Power Consumption

There are many ways to reduce power consumption of a MAC unit. Some of the methods that we will employ in our design are listed below.

2.2.1. Logic Styles:

Dynamic and static logic, for example, have different speed/power tradeoffs.

2.2.2. Transistor Sizing:

Adjusting the size of each gate or transistor can reduce the power consumption.

2.2.3. Reduced Supply Voltage:

Power consumption (P) of a CMOS based MAC unit is related to the supply voltage (V), switching frequency (*f*), and CMOS gate capacitance (C). The relationship can be stated as:

$$P \alpha C * f * V^2$$

The above relationship shows that reducing the supply voltage can reduce power consumption. However, the switching frequency is directly proportional to the supply voltage as well; that is:

$$V \alpha f$$

Therefore, while lowering supply voltage will reduce power consumption, it will also result in lower switching frequency, and thus slower MAC unit speed. A trade off must be made in the form of speed in order to reduce power usage.

2.2.4. Full Custom Design:

Full custom design will help to reduce the number of logic gates in the implementation of the necessary functionality of the MAC unit. Since each logic gate requires power to operate, lower gate count means fewer switching and thus lower power need.

2.2.5. Using Low Power CMOS Design:

There are three existing low power CMOS [6] design techniques in current technology namely Variable Threshold CMOS (VTCMOS), Super Cut-off CMOS (SCCMOS) and Multiple Threshold CMOS (MTCMOS).

2.2.6. Clock Gating or Block Enabling:

Clock gating is a method where certain parts of the MAC unit are prevented from receiving the clock signal. If a part of the processor is not needed for a given operation, then the clock signal to that part can be blocked. Switching requires large power. In the absence of the clock signal switching will not take place and gating the clock will lower the needed power.

2.3 Block Enabling Technique

In any MAC unit, data flows from the input register to the output register through multiple stages such as, multiplier stage, adder stage and the accumulator stage as shown in figure 4. Within the multiplier stage, further we find that there are multiple stages of addition. During each operation of multiplication and addition, the blocks in the pipeline may not be required to be on or enabled until the actual data gets in from the previous stage. In block enabling technique, we find the delay of each stage. Every block gets enabled only after the expected delay. For the entire duration until the inputs are available, the successive blocks are disabled, thus saving power. In the next section, we design a 1-bit MAC unit with pipeline structure and find the power consumption.

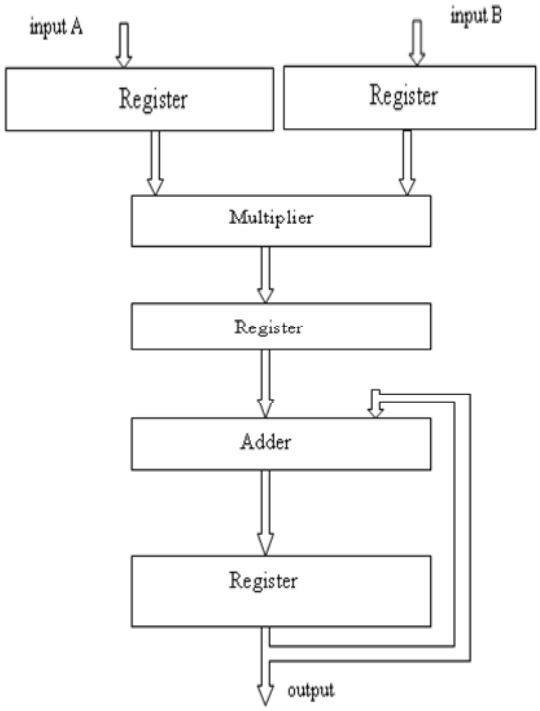

Fig 4: General Block Diagram of a Pipeline MAC with block enabling Technique cs - control signal

2.4 Pipelined block enabled logic

Figure 5 shows a three stage pipelined MAC with block enable logic. In this logic, depending upon the delay of individual blocks, the control logic enables the clock, power and logic pins of the block, thus saving power. Figure 6 shows the block schematic of the 1 bit full adder circuit with enable. Each of the blocks in the MAC unit has an enable signal to save power.

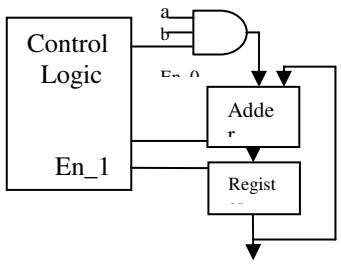

Fig 5: MAC with control logic

We find that the basic building blocks for any MAC unit are Multiplier, Adder and Register. Multiplier and adder blocks require full adders, and registers require flip-flops or latches. The objective of this work is to find the total area, power and delay of the MAC unit that forms the critical part of any DSP application. At the micro level, the power, delay and area for the basic blocks are calculated based on the experimental setup.Based on the results obtained, the reasons for power and delay are identified at the micro level and remedies are taken to minimize this power. Further this power reduction technique is extended at the macro level. In our design, it is the MAC architecture. Section 3 discusses these results.

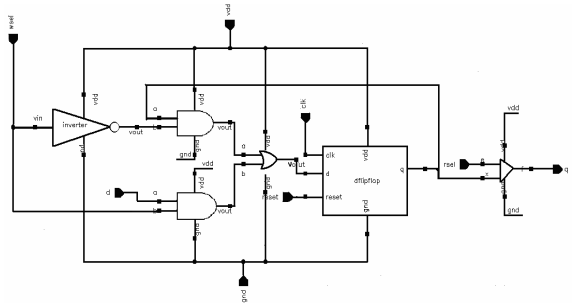

Fig 6: 1 bit Register cell

Comparison of Wallace MAC with and without Block Enabling Technique							
Architecture	**Cells**	**Leakage Power**	**Dynamic Power**	**Total Power**	**Area**	**Internal Power**	**Net Power**
Normal mode (Without BET)	**162**	**4739**	**25150**	**29890**	**1600**	**21065**	**4084**
Low Power mode(With BET)	**165**	**4585**	**22313**	**26898**	**1544**	**18277**	**4585**
% of Dynamic Power Savings of Wallace MAC with Block enabling Technique over Wallace MAC without Block Enabling Technique = 11.28 %							

3. Results

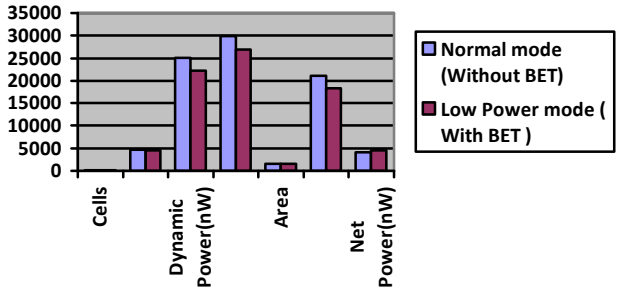

Fig. 6: Generated bar-graph indicating power consumption details of the design in two modes (normal and low power modes)

Control logic built, controls the multiplier logic to work only when cs_1 is high and at that time the accumulator consumes no power. Similarly in the next cycle, when the output from multiplier block is available for the next state, cs_2 is made high and that enables only the accumulator to consume power. Hence power consumption is reduced. Percentage of Dynamic Power Savings of Wallace MAC with Block enabling Technique over Wallace MAC without Block Enabling Technique is 11.28 %.

4. Conclusion

In the previous chapter, the results of both Wallace-MAC and Wallace-MAC with block enabling technique are tabulated and by observing the table following conclusions can be derived.

1. Design and Implementation of low power MAC using the Cadence tool is achieved.
2. The power factor is reduced by 11.28% using Block Enabling Technique.
3. Block Enabling proves to be one of the efficient technique to reduce power, hence one can implement this to various logic circuits to reduce power.

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