ADC Histogram Test by Triangular Small-Waves

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Abstract – A histogram-based method for quasi-static test of analog-to-digital converters has been proposed for standardization aims. The test exploits the use of small-amplitude triangular waves. Different signal offset values are used to fully stimulate the converter input range. The reduced amplitude and slope of the input triangular wave with respect to the converter range and slew rate, respectively, lead to quasi-static test conditions. The test allows (i) linearity constraints of function generators to be relaxed, and (ii) experimental burden to be reduced. In this paper, after a brief recalling of the test procedure, analytical relations for designing an efficient test are provided. Numerical and experimental results of a comparative analysis with the IEEE 1057/94 standard static test highlight its better performance.

Keywords – ADC testing, static test, histogram method.

I. INTRODUCTION

In the traditional static test of analog to digital converters (ADCs), the code transition levels are determined according to a step-wise algorithm [1]. In successive steps, the DC input test signal is progressively increased. For each step, a suitable amount of samples is acquired according to the required statistical significance on the transition level measurement. By considering that for each transition level, about 5 input voltage changes are required, and that, for each of them, a significant waiting time is required for the calibrator to settle, the test duration becomes prohibitive for high-resolution ADCs. In this case, the problems increase with the number of bits and with the accuracy required for the results.

One solution to decrease the test duration is to reduce the number of applied voltage changes. In [2] a method that uses a variable step size calculated by using an extrapolated convergence factor method was proposed. The basic idea was to try guessing the position of the next code transition level from the results of the previous data records. However the test duration was not reduced as significantly as desired. In this paper a new approach that reduces dramatically the test duration is proposed.

In Section II, after a brief recalling of the basic idea underlying the proposed method, the procedure of the proposed test is illustrated. In Section III, analytical relations for designing an efficient test are provided. In Section IV, numerical simulations for characterizing the efficiency of the test are reported.

Finally, in section V, experimental results aimed at comparing the proposed techniques with the IEEE 1057/94 standard static test are presented.

II. THE PROPOSED TEST

The basic idea of the proposed test is the use of small amplitude triangular waves with increasing DC offset levels as stimulus signal for a histogram-based quasi-static test of ADCs [3,4]. The converter range is scanned by progressively increasing the offset level (C) step by step systematically (Fig.1). Small amplitude and slope in comparison to the converter range and slew rate, respectively, lead to quasi-static test conditions.

The histogram procedure [4-7] is adopted in order to reduce the sample number and the test time in comparison to the standard static test. The total number of samples to be acquired for the same desired tolerance and confidence levels is much lower with the histogram method in relation to the traditional static test, as will be shown in this paper. As a matter of fact, the number of changes of the DC input offset generator is reduced by several orders of magnitude. Consequently, the total waiting time for the calibrator settling will decrease accordingly. For instance, if 50 codes at a time are stimulated by the small-amplitude wave, the waiting time will be reduced by about 250 times.

The standard histogram test exploits a sinusoidal stimulus signal since it is easier to generate with sufficiently low distortion than a triangular one [1,7]. This is due to the present state of the art in function generators. However, conceptually, to characterize an ADC, a linear stimulus signal should be...
used for achieving uniform stimulus condition over the range [9,10]. In the proposed test, the constraint on the linearity of the triangular generator is relaxed by using a signal of amplitude much lower than the fullscale. In order to stimulate all the ADC input range, the acquisition of the samples is repeated, in several steps, with the same small-amplitude triangular wave but with different offset values.

The procedure of the proposed test is reported in Fig. 2. In each of the $N_s$ steps, the ADC acquires $M$ records of $R$ samples [5]. The sampling frequency $f_s$ and the small-wave frequency $f$ are selected according to the standard histogram test procedure [1]. The data acquisition is repeated $N_s$ times for progressively increased values of the offset $C_j$. With the samples acquired in each step a cumulative histogram $CH_j[k]$ is computed. The value for the $k$-th class of the cumulative histogram is obtained by counting the number of samples whose output code is equal to or less than the code $k$. The transition levels for each step are computed from the cumulative histogram [5,11]. After all the steps, $N_s$ different transition voltage arrays are obtained. These have to be combined into a single one. However, the need for overdrive [3,5], as well as the inaccuracy of the stimulus signal, give rise to some transition levels with two values computed. The one far from the step limit is considered for final computation since the triangular wave is more distorted near the peaks owing to the discontinuity of the derivative [3].

### III. PROCEDURE DESIGN

In designing the test, the user has to define the values of its main parameters: (i) the amplitude $A$ of the small wave, (ii) the offset $C_j$ in the $j$-th step, (iii) the number of samples $M$ in each record, and (iv) the frequency $f$ of the small wave. In the following, analytical relations for designing the procedure parameters are provided.

#### A. Small-Wave Amplitude ($A$)

The small wave amplitude $A$ must be sufficiently small to relax the linearity constrains of the triangular signal generator. The non linearity, $NL$, of a triangular wave can be defined as the ratio of the maximum difference between actual and ideal waves, and its ideal amplitude. This $NL$ causes an error on the measured transition voltages. Once the user defines a maximum value $B_i$ for this error, a boundary for the amplitude in the case of an $n_b$-bit ADC can be defined:

$$ A \leq \frac{B_i}{NL \cdot (2^n - 1)} = A_{\text{max}} $$

(1)

where $V = T[2^n - 1] - T[1]$ is the ADC reduced fullscale voltage.

Overdrive is needed to increase accuracy and to guarantee that all codes are stimulated. By starting from the overdrive required for the traditional sinusoidal histogram test, the overdrive necessary for the proposed test is derived [5]:

$$ V_{OD} = \sigma_n \cdot \left[ \sqrt{2 \pi} - 4 \ln \left( \frac{\sqrt{2 \pi} \cdot Q}{\sigma_n} \right) \right] - \sqrt{2 \pi} $$

(2)

where $B_i$ is expressed in LSB, $\sigma_n$ is the standard deviation of the input-equivalent noise, and $Q$ the ideal code bin width.

The amplitude of the small wave is equal to half of the range stimulated in each step ($\Delta s$) plus the amount of overdrive $V_{OD}$. Thus, the maximum value $\Delta s_{\text{max}}$ is

$$ \Delta s_{\text{max}} = 2(A_{\text{max}} - V_{OD}) $$

(3)

For equal steps, the number of step $N_s$ results

$$ N_s = \left\lfloor \frac{V}{\Delta s_{\text{max}}} \right\rfloor $$

(4)

where $[x]$ denotes the integer part of $x$. Consequently, the exact range to be stimulated in each step is
\[
\Delta t = \frac{V}{N_f} \quad (5)
\]

and the small wave amplitude results
\[
A = \frac{\Delta s}{2} + V_{oo} \quad (6)
\]

B. Offset (Cj)
The offset \(C_j\) to apply in the \(j\)-th step is the middle point of the stimulated range:
\[
C_j = T[1] + \frac{\Delta s}{2} + j \cdot \Delta s, \quad j = 0, 1, \ldots, N_s - 1 \quad (7)
\]

where \(T[1]\) is the lowest transition level.

C. Number of Samples (M)
The maximum number of samples in each record \(M\) depends on the input frequency \(f\), the sampling frequency \(f_s\), and their accuracies \(\varepsilon_f\) and \(\varepsilon_{f_s}\). The following expression sets a boundary for the relative error \(\varepsilon_{f_s}\) of the ratio between these two frequencies \([12]\):
\[
\frac{\varepsilon_{f_s}}{2D \cdot M} \quad (8)
\]

where \(D\) is the acquired number of signal periods. From (8), by substituting the explicit expression of \(\varepsilon_{f_s}\), the maximum number of samples \(M_{\text{max}}\) is derived:
\[
M \leq \left\lfloor \frac{1}{2} \cdot \frac{f_s}{f} \cdot \frac{\varepsilon_f}{1 - \varepsilon_f} \right\rfloor = M_{\text{max}} \quad (9)
\]

Furthermore, the uncertainty on the transition levels arises because the number of occurrences in the cumulative histogram is a random variable. This is due to three factors: additive noise \(\sigma_n\), phase noise \(\sigma_{\phi}\), and random phase difference between the stimulus signal and the sampling clock. This last is generally negligible compared with the other two, provided that (9) is verified. For a given uncertainty \(B_u\), an expression to determine the minimum number of samples per step was derived on the basis of previous work on the traditional histogram method \([5, 13]\), but considering a triangular stimulus and its small amplitude:
\[
M_{\text{min}} = \left(\frac{K_u}{B_u} \cdot 2A \cdot \frac{\sqrt{\pi} \sigma_n + \sigma_{\phi}}{4A} \right)^2 \quad (10)
\]

where \(K_u\) is the confidence level of the transition levels in case of the maximum limit \(B_u\) allowed for their uncertainty.

The number of samples per step is
\[
M_s = R \cdot M \quad (11)
\]

where \(R\) is the number of records determined as
\[
R \geq \left\lceil \frac{M_{\text{min}}}{M_{\text{max}}} \right\rceil \quad (12)
\]

where \(\lceil x \rceil\) denotes rounding up to the next integer.

Thus, the number of samples per record results:
\[
M \geq \left\lceil \frac{M_{\text{min}}}{R} \right\rceil \quad (13)
\]

IV. EFFICIENCY ANALYSIS

In this section, the efficiency of the proposed test is analyzed in terms of time duration \(t_T\) and it is compared to the one of the standard static test. In particular, the influences of (i) the number of bits \(n_b\), (ii) the input-equivalent noise standard deviation \(\sigma_n\), (iii) the phase noise standard deviation \(\sigma_{\phi}\), and (iv) the required uncertainty \(B_u\) are analyzed. With this aim, at first the expressions of the \(t_T\) are derived for both the tests, and then the analysis conditions are defined.

The duration of the proposed test depends on the step number \(N_s\) and on the time taken by each step:
\[
t_T = N_s \cdot \left[ T_s + \left( T_c + \frac{1}{f_s} \right) \cdot R \cdot M \right] \quad (14)
\]

where \(T_s\) is the generator settling time, and \(T_c\) the communication time.

The duration of the standard static test depends on the ADC number of transition levels \((2^{n_b} - 1)\), the number of used input voltages \(N_T\) by each transition level determination, and the time necessary for the acquisition:
\[
t_T = N_T \cdot (2^{n_b} - 1) \cdot \left[ T_s + \left( T_c + \frac{1}{f_s} \right) \cdot M \right] \quad (15)
\]

The analysis was carried out in the following conditions: (i) a reduced fullscale voltage \(V\) of 1V; (ii) an accuracy \(B_i\) of 0.001LSB on the measured transition levels; (iii) a small-wave frequency \(f\) of 10Hz; (iv) a sampling frequency \(f_s\) of
10MS/s, (v) accuracies $\varepsilon_f$ and $\varepsilon_{fs}$ of $\pm 25$ppm; (vi) a communication time $T_c$ of 100 $\mu$s per sample, (vii) a settling time $T_s$ of 0.1s; (viii) number of input levels for the determination of each transition level $N_T$ equal to 5, as required in average by the standard static test [1]; and (viii) finally a sample number $M = (3.66 \cdot \sigma_n / Q \cdot B_s)^2$, derived from [1] for a confidence level equal to $3\sigma$.

A. Number of Bits

For this analysis, the standard deviation of the input-equivalent noise and the phase noise were set to 1LSB and $721 \cdot 10^{-\pi}$ rad respectively, and a required uncertainty $B_u$ of $\pm 0.1$LSB was used. In Fig. 3, the durations of the two tests are compared at varying the number of bits. The semilogarithmic scale highlights their quasi-exponential trend. In particular, the duration of the standard static test doubles with each added bit according to (15), and is prohibitive for high-resolution converters ($n_b \geq 16$). The duration of the proposed test is generally 10 times lower than the standard test one. For converters with 12 or more bits, it doubles with the increase of each bit, but is practically independent from the number of steps used. Furthermore, in Fig.3, also the decreasing impact of the step number on the proposed test duration is highlighted by reporting the extreme cases of 1 and 100 steps.

B. Input-equivalent Noise

This analysis was carried out on a 12-bit ADC with a phase-noise standard deviation of $2\pi \cdot 10^{-7}$ rad, and a required uncertainty of $\pm 0.1$LSB. In Fig. 4, the durations of the proposed and the standard test are compared at varying the input-equivalent noise standard deviation $\sigma_n$. The duration of the static test depends on the square of the noise standard deviation, for the required number of samples.

In the case of the proposed test, the dependence is almost linear according to (10). Also in this case, the increasing impact of the step number on the proposed test duration is highlighted in Fig.4, by reporting the extreme cases of 1 and 100 steps.
C. Phase Noise

The analysis of the phase noise $\sigma_\phi$ influence on the test duration was carried out for a 12-bit ADC, with 2mV input-equivalent noise standard deviation, and a required uncertainty of $\pm 0.1$ LSB. Of course, the duration of the standard test is independent on the phase noise. For the above conditions of analysis, this duration is equal to 1.33 hours. The duration trend of the proposed with the phase-noise standard deviation is represented in Fig.5. The dependence is linear and again the impact of the step number on the proposed test duration can be highlighted.

D. Required Uncertainty

The analysis of the influence of the required uncertainty $B_u$ for the transition levels on the test duration was carried out for a 12-bit ADC, with 2mV input-equivalent noise standard deviation, and phase noise with $2\pi \cdot 10^{-7}$ rad of standard deviation. In Fig.6, the durations of the two tests are compared at varying the required uncertainty. In particular, for both the tests the duration decreases according to the required accuracy, but it is always much lower for the proposed test.

V. EXPERIMENTAL RESULTS

An experimental analysis was carried out on two different digitizer architectures: a VXI waveform analyzer (Tektronix VX4240), and a PC data acquisition board (Keithley DAS1601). The Tektronix VX4240 is based on a Burr-Brown 12-bit ADC mod.603JH. It was tested in the $\pm 2$V range, single-ended mode, with a sampling frequency of 10Msample/s. In this range, the LSB is equal to 976.8 $\mu$V. The communication time $T_c$ between the waveform analyzer and the PC is 150 $\mu$s. The Keithley DAS 1601 is based on a 12-bit successive approximation ADC from Burr-Brown (ADS774). It was tested in the $\pm 1$V range at its maximum sampling frequency of 100kS/s. In this range, the LSB is equal to 488 $\mu$V, while $T_c$ is 1 $\mu$s.

<table>
<thead>
<tr>
<th>Table I</th>
<th>Calibrator</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model</td>
<td>Fluke 5700A</td>
</tr>
<tr>
<td>Range</td>
<td>2.2 V</td>
</tr>
<tr>
<td>Uncertainty</td>
<td>8ppm+1.2mV</td>
</tr>
<tr>
<td>Settling time ($T_s$)</td>
<td>1 s</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table II</th>
<th>Function Generator</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model</td>
<td>Wavetek 9100</td>
</tr>
<tr>
<td>Frequency</td>
<td>998.0 Hz</td>
</tr>
<tr>
<td>Frequency accuracy</td>
<td>25 ppm</td>
</tr>
<tr>
<td>Frequency resolution</td>
<td>4 digits</td>
</tr>
<tr>
<td>Amplitude accuracy</td>
<td>0.15% of output +400$\mu$V</td>
</tr>
<tr>
<td>Triangular Wave nonlinearity</td>
<td>0.085%</td>
</tr>
</tbody>
</table>

A comparative analysis of the proposed test with the standard one was carried out also in experimental conditions in order to: (i) validate the proposed test by verifying its accuracy in estimating the INL, and (ii) verify its efficiency.

Table I shows the specifications of the calibrator used to generate both the input DC voltage for the standard test and the offset voltage for the proposed test. Table II shows the specifications of the small triangular wave generator.

The examples reported in the following were performed in the experimental conditions of Tables III and IV, for the standard and the proposed test, respectively.

A. Validation

Figs. 7 and 8 show the differences of the results obtained for the INL ($\Delta$INL) by using the proposed and the standard static test for the VX4240 and the DAS1601 respectively. It can be seen that when the test is performed with a high number of steps, as in the conditions of Fig.8, the differences in relation to the results of the standardized procedure are negligible. In Fig.7 a small influence on the results of the nonlinearity of the generator due to the small number of steps according to (10), can still be observed as it was shown in [3,4].

<table>
<thead>
<tr>
<th>Table III</th>
<th>Standard Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M$</td>
<td>VX4240</td>
</tr>
<tr>
<td>Input-equivalent noise</td>
<td>2LSB</td>
</tr>
<tr>
<td>Uncertainty</td>
<td>0.25 LSB</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table IV</th>
<th>Proposed Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M$</td>
<td>VX4240</td>
</tr>
<tr>
<td>$R$</td>
<td>50,099</td>
</tr>
<tr>
<td>$N_s$</td>
<td>10</td>
</tr>
<tr>
<td>$A$</td>
<td>220 mV</td>
</tr>
<tr>
<td>$f$</td>
<td>998.0 Hz</td>
</tr>
<tr>
<td>Uncertainty</td>
<td>0.13 LSB</td>
</tr>
</tbody>
</table>
B. Efficiency Comparison

Tables V and VI show the huge reduction on the number of acquired samples and on the duration of the proposed test, respectively, in comparison with the standard test.

<table>
<thead>
<tr>
<th></th>
<th>Standard Test</th>
<th>Proposed Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>VX4240</td>
<td>20,966,400</td>
<td>5,009,900</td>
</tr>
<tr>
<td>DAS1601</td>
<td>83,865,600</td>
<td>23,999,760</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Standard Test</th>
<th>Proposed Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>VX4240</td>
<td>7 hours</td>
<td>11 minutes</td>
</tr>
<tr>
<td>DAS1601</td>
<td>6 hours</td>
<td>5 minutes</td>
</tr>
</tbody>
</table>

VI. CONCLUSIONS

In this paper, a quasi-static test based on a histogram algorithm was presented. The small ADC range swept by the test signal, together with a reduced slope, gives rise to quasi-static test conditions. It reduces dramatically the duration of the test in comparison to the standard static test and it allows the use of inexpensive function generators. The linearity constraint of the generator is relaxed by exploiting triangular test signals ranging only a small fraction of the ADC fullscale. Relations for designing the proposed test parameters were provided for standardization purposes.

Numerical and experimental simulation results for characterizing the efficiency of the proposed test and for comparing it with the standard test, were presented. They show that the new technique can perform the test in a small time fraction of the standard one, for the same accuracy level.

ACKNOWLEDGMENT

This work was sponsored by the Portuguese research project PCTI/ESE/32698/1999, entitled “New Measurement Methods in Analog to Digital Converters Testing”, whose support the authors gratefully acknowledge.

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