Proceedings of the 15th
IEEE International Conference on Nanotechnology
July 27-30, 2015, Rome, Italy

Ultra-high Density Out-of-plane Strain Sensor 3D Architecture based on Sub-20 nm PMOS FinFET

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***Abstract*— Future wearable electronics require not only flexibility but also preservation of the perks associated with today's high-performance, traditional silicon electronics. In this work we demonstrate a state-of-the-art fin-shaped field-effect transistor (FinFET)-based, out-of-plane strain sensor on flexible silicon through transforming the bulk device in a transfer-less process. The device preserves the functionality and high performance associated with its bulk, inflexible state. Furthermore, gate leakage current shows sufficient dependence on the value of the applied out-of-plane strain that enables permits use of the flexible device as a switching device as well as a strain sensor.**

Keywords—FinFET; sensor; flexible; electronics; silicon

I. INTRODUCTION

With the emergence of the Internet of Things (IoT) we expect to see a flexible version of state-of-the-art electronics deployed on curvilinear surfaces in wearable format [1–7]. Various methods and techniques have already been proposed for achieving flexible electronic systems.

There are three mainstream approaches towards making flexible electronics. The first approach is building an all-polymer based electronic system that capitalizes on the inherent flexibility of polymers [8–11]. The most critical challenge with this approach is the relatively low performance of polymeric material compared to the performance of traditional state-of-the-art silicon electronics. The second mainstream approach adds a transfer step in which silicon-based high-performance electronics are built using various microfabrication techniques and then transferred to a polymeric substrate for flexible support. This is an important milestone toward high-performance, flexible electronic systems [12–15]. But the complexity associated with the transfer step, the low yield and low integration density, continue to pose critical challenges that must be met. The third approach uses a fundamental relation of inverse proportionality by relating a material's thickness (t) to its flexibility or flexural modulus ($\varepsilon_{Flexural}$) (1) to transform the traditional high-performance electronics on bulk inflexible silicon into flexible ones through a transfer-less process by reducing the silicon substrate's thickness using soft-back etch deep reactive ion etch (DRIE) chamber [16–19].

$$\varepsilon_{Flexural} \propto 1/t^3 \quad (1)$$

In this work we capitalize on the third approach to transform state-of-the-art high-κ hafnium silicate fin-shaped field-effect transistors (FinFETs) on silicon into a flexible version. Moreover, we harness the device's added flexing ability to use its functionality as an out-of-plane strain sensor.

II. FABRICATION OF PMOS HFSIO FINFETS

A. Traditional Device Fabrication

To build traditional state-of-the-art FinFETs, silicon-on-insulator (SOI) monitor grade wafers were used with gate first approach. The fins were patterned using deep ultra-violet lithography to achieve sub-20 nm features followed by anisotropic reactive ion vertical etch of silicon. The gate stack is then formed by successive deposition of 4 nm hafnium silicate (HfSiO) gate dielectric and 10 nm of TiN gate metal. Ion implantation of source and drain was then carried out followed by NiSi salicidation and Al sputtering for ohmic contacts; activation anneal of dopants was carried out at 1000°C for 10 seconds. The device has a 250 nm channel length. A summary of the main fabrication steps is depicted in Fig. 1.

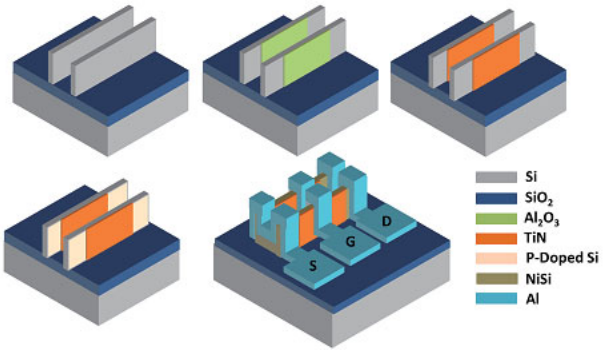


Fig. 1 Fabrication process of PMOS FinFETs with 2 fins.

B. *Transofrmation into a Flexible Device*

Fig. 2 shows the transformation steps of the fabricated devices. First, the fabricated devices are protected using ECI 327 positive-tone photoresist and then flipped upside down on a carrier wafer for the thinning etch. Using DRIE soft-back etch, the die is transformed from 500 µm thick inflexible substrate into a 50 µm flexible fabric that bear the fabricated devices.

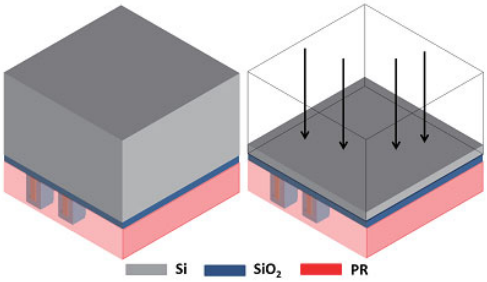
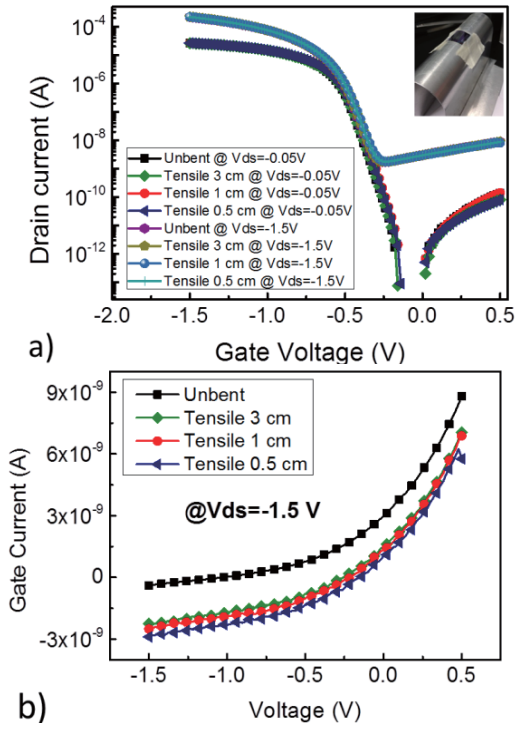


Fig. 2 Transforming the bulk devices into flexible ones.

III. Results and Discussion

Fig. 3a shows the transfer characteristics of the 250 nm PMOS FinFET; the inset shows the physical testing setup for applying out-of-plane tensile stress using custom-designed, steel curved structures. Although the drain currents show no sensitivity to out-of-plane strain, we have observed sensitive gate leakage following a specific pattern as out-of-plane strain increases (Fig. 3b and 3c). This means that gate leakage can be monitored and sensed for strain measurements while, at the same time, the functionality of the FinFET as a switching gating structure remains intact.

Fig. 4 shows the sensing properties of the PMOS FinFET as a strain sensor. The measurement points are fitted linearly for an accurate estimation of the sensitivity of the device to out-of-plane stress, and the results are summarized in Table I.



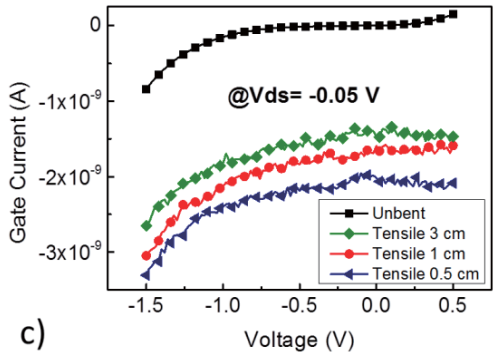


Fig. 3: (a) Transfer characteristics of PMOS FinFET, (b) Gate current in saturation, and (c) Linear regime.

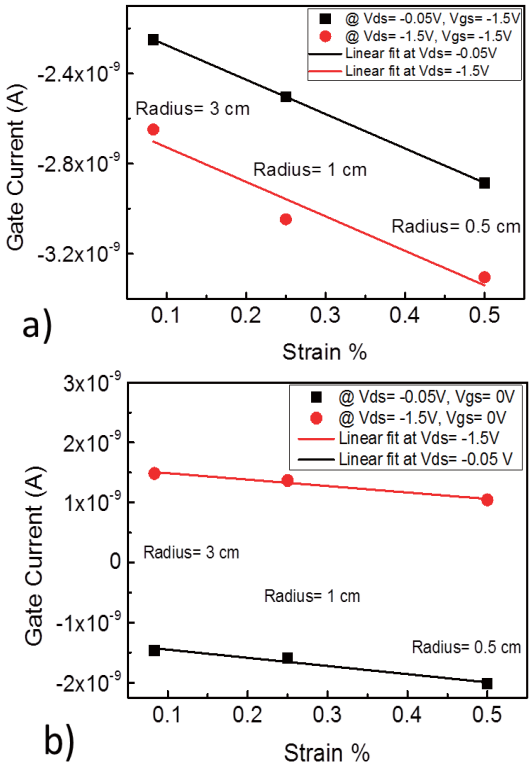


Fig. 4: Linear relation between sense gate current and bending radius (out-of-plane strain %) when the transistor is (a) "ON" (V_{gs}=-1.5V) and (b) "OFF" (V_{gs}=0V).

Table I: Sensitivity of the PMOS FinFET strain sensor under different operation conditions.

Sensing Regime	Sensitivity (nA/1% strain)
$V_{ds}=V_{gs}=-1.5$ V	1.53
$V_{ds}=V_{gs}\sim 0$V	1.36
$V_{ds}\sim 0$V, $V_{gs}=-1.5$V	1.53
$V_{ds}=-1.5$V, $V_{gs}=0$V	1.07

These results show that the bent PMOS FinFET can be used as an out-of-plane strain sensor by sensing the gate current at all operation conditions without affecting the functionality of the device because the drain current is not

affected. For digital applications, the transistor acts as a simple switch that has a signal applied to its terminals that is either a "0" or a "'1." The "0" corresponds to ground reference, and "1" corresponds to the supply voltage V_{dd}. Fixing the source voltage as a reference, there are only four possible combinations of applied signals for the two terminals (gate and drain): "11" corresponds to V_{gs} (voltage between gate and source terminals) = V_{ds} (voltage between the drain and source terminals) = V_{dd} (-1.5 V, in our case) "00" corresponds to V_{gs}= V_{ds} = 0 V; "01" corresponds to V_{ds} = 0 and V_{gs} = V_{dd}; and "10" corresponds to V_{ds} = V_{dd} and V_{gs}= 0. Under all these possible regimes of functionality for the PMOS as a switch, an external sensing analogue circuit can be connected to the gate terminal to sense the leakage current and deduce the strain information (the bending radius value) based on the current value because, in all cases, the sensitivity of the device as a sensor lies between 1.07 and 1.53 nA per 1 % change in strain.

The gauge factor (GF) is define as the slope of the normalized sensed current (I/I(0)) *vs.* strain plot (ε) (2) [20].

$$[\Delta I(\varepsilon)/I(0)]/\Delta\varepsilon \quad (2)$$

where I(0) is defined as the current through the gate at similar V_{gs} and V_{ds} while the transistor is unbent. Fig. 5 shows the gauge factor for the different states of operation of the FinFET. The pattern depicted shows that when the transistor's gate is in "00", the gauge factor is highest indicating maximum sensitivity to out-of-plane stress. This is because the transistor has very low gate leakage (pA range) in the unbent state, when V_{ds} is 0.05 V and V_{gs} is 0 V; whereas, when bending occurs the gate leakage current increases by three orders of magnitude. The slight increase of gauge factor from "01" to "10" and "11" is attributed to the contention between Vgs and V_{ds} is controlling how much leakage current is collected through the gate terminal. Higher gauge factors mean that changes in mechanical strain will result in higher electrical signal change.

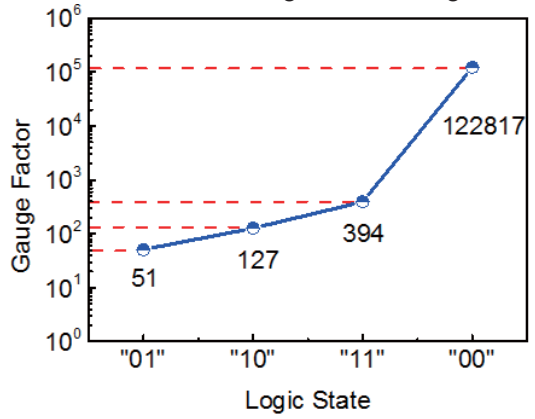


Fig. 5 Gauge factor vs. strain plot for the four possible states of the sensor FinFET; the inset shows the "00" state on a semi-log scale.

IV. Conclusion

We have demonstrated a state-of-the-art 3D FinFET PMOS transistor that preserves functionality in its flexible state after being transformed in a transfer-less soft-back etch process from rigid bulk into a thin flexible state. The sensing ability of the device is quantified and calibrated relating gate leakage current to the applied out-of-plane strain. These results present an important milestone toward achieving ultra-high-density CMOS sensor networks for wearable and other flexible electronics-enabled applications.

Acknowledgment

The authors acknowledge KAUST OCRF Grant CRG-1-2012-HUS-008.

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