Emphasis of Modulated Techniques for Cascaded Multilevel Inverters fed drive using FPGA

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Abstract-Pulse width modulated (PWM) techniques of a voltage source inverter need a reference signal and carrier signal to generate the required modulating signals for the desired output. Modifications in Modulating techniques can be considered in two ways, namely Modified reference and Modified carrier. The existing multilevel carrier-based pulse width modulation strategies have no special provisions to offer quality output, besides lower order harmonics are introduced in the spectrum, especially at low switching frequencies. This paper proposes a novel multilevel PWM strategy to counter the advantages of low frequency switching and reduced total harmonic distortion (THD). This paper also presents the most relevant control and modulation methods by a new reference/carryer based PWM scheme for Cascaded Multilevel Inverter and comparing the performance of the proposed scheme with that of the existing control schemes. A prototype is developed for a single-phase 5-level cascaded inverter fed drive using VHDL programming with FPGA.

Index Terms- Multilevel concept, Field Programmable Gate Array(FPGA), Cascaded Multi level inverters, Multi Level carrier signals, Pulse width modulation, Total Harmonic Distortion.

I. INTRODUCTION

Multilevel power conversion technology is a very rapidly growing area of power electronics with good potential for further development. The most attractive application of this technology is in the medium-to-high-voltage range, motor drives, power distribution, and power conditioning applications. In recent years, industry demands power in the megawatt level. Controlled ac drives in the megawatt range are usually connected to medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels [4].

Multilevel inverter structures have been developed to overcome shortcomings in solid-state switching device ratings so they can be applied to higher voltage systems. The multilevel voltage source inverters [10] unique structure allows them to reach high voltages with low harmonics without the use of transformers. The general function of the multilevel inverter is to synthesize a desired ac voltage from several levels of dc voltages as shown in Fig. 1.

II. FIELD PROGRAMMABLE GATE ARRAY (FPGA)

A field-programmable gate array is a semiconductor device containing programmable logic components called "logic blocks", and programmable interconnects. Logic blocks can be programmed to perform the function of basic logic gates such as AND, and XOR, or more complex combinational functions such as decoders or simple mathematical functions. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

A hierarchy of programmable interconnects allows logic blocks to be interconnected as needed by the system designer, somewhat like a one-chip programmable breadboard. Logic blocks and interconnects can be programmed by the customer or designer, after the FPGA is manufactured, to implement any logical function—hence the name "field-programmable". The architecture of field programmable gate array is illustrated in Fig. 2, similar to that of a mask programmable gate array (MPGA), consisting of an array of logic blocks that can be programmably interconnected to realize different designs. The major difference between FPGA's and MPGA's is that an MPGA is programmed using integrating circuit fabrication to form metal connections, while an FPGA is programmed via electrically programmable switches much the same as traditional PLD's. FPGA's can achieve much higher levels of integration than PLD's, however, due to their more complex routing architectures and logic implementations. PLD routing architectures are very simple but highly inefficient cross-bar like structures in which every output is directly connectable to every input through one switch. FPGA routing architectures provide a more efficient MPGA-like routing where each connection typically passes through several switches. In a PDL, logic is implemented

![Fig. 1 Multilevel concept for (a) two level (b) three level and (c) 5-level](image-url)
using predominantly two-level AND-OR logic with wide input AND gates. In an FPGA logic is implemented using multiple levels of lower fan-in gates, which is often much more compact than two-level implementations.

Fig. 2 FPGA Architecture

An FPGA logic block can be as simple as transistor or as complex as a microprocessor. It is typically capable of implementing many different combinational and sequential logic functions. Current commercial FPGA’s employ logic blocks which are based on one or more of the following:

- Transistor pairs.
- Basic small gates such as two-input NAND’s or exclusive-OR’s.
- Multiplexers.
- Look-up tables (LUT’s).
- Wide-fan-in AND-OR structures.

Table 1. Load voltage with corresponding conducting switches

<table>
<thead>
<tr>
<th>Conducting switches</th>
<th>Load voltage (Vab)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1, S2</td>
<td>+Vdc</td>
</tr>
<tr>
<td>S3, S4</td>
<td>-Vdc</td>
</tr>
<tr>
<td>S1, S4 or S3, S2</td>
<td>0</td>
</tr>
</tbody>
</table>

The advantages and disadvantages of cascaded H-bridge inverter is as follows:

Advantages:
1. The series structure allows a scalable, modularized circuit layout and packaging since each bridge has the same structure.
2. Requires the least number of components considering there are no extra clamping diodes or voltage balancing capacitors.
3. Switching redundancy for inner voltage levels are possible because the phase voltage output is the sum of each bridges output.
4. Potential of electric shock is reduced due to the separate d.c sources.

Disadvantages:
1. Limited to certain applications where separate d.c sources are available.

III. CASCADED FIVE LEVEL INVERTER

The cascade H-bridge inverter is a cascade of H-bridges, or H-bridges in a series configuration. A single H-bridge inverter is shown in Fig. 3 and the cascade of H-bridge inverter for five-level inverter is shown in Fig. 4. A N level Cascaded H bridge inverter consists of series connected (N-1)/2 number of cells in each phase. Each cell consists of single phase H bridge inverter with separate d.c source. There are four active devices in each cell and can produce three levels 0, Vdc/2 and –Vdc/2. Higher voltage levels can be obtained by connecting these cell in cascade and the phase voltage can be the sum of voltages of individual cells, \( v_{an} = v_1 + v_2 + v_3 + \ldots + v_N \). For a three phase system, the output of these cascaded inverters can be connected either in Y or \( \Delta \) configuration.

![Fig. 3 Configuration of single-phase H-bridge inverter](image)

![Fig. 4 Configuration of three-phase Cascaded Five Level Inverter (C 5LI)](image)

IV. PROPOSED MODULATED TECHNIQUE

In the SPWM scheme for two-level inverters, each reference phase voltage is compared with the triangular carrier and the individual pole voltages are generated, independent of each other [6]. To obtain the maximum possible peak amplitude of the fundamental phase voltage, in linear modulation, a
common mode voltage, \( V_{\text{offset}} \), is added to the reference phase voltages [9, 1], where the magnitude of \( V_{\text{offset}} \) is given by

\[
V_{\text{offset}} = -\frac{(V_{\text{max}} + V_{\text{min}})}{2}
\]  

In (1), \( V_{\text{max}} \) is the maximum magnitude of the three sampled reference phase voltages, while \( V_{\text{min}} \) is the minimum magnitude of the three sampled reference phase voltages, in a sampling interval. The addition of the common mode voltage, \( V_{\text{offset}} \), results in the active inverter switching vectors being centered in a sampling interval, making the SPWM technique equivalent to the modified reference PWM technique [9]. Equation (1) is based on the fact that, in a sampling interval, the reference phase which has lowest magnitude (termed the min-phase) crosses the triangular carrier first, and causes the first transition in the inverter switching state. While the reference phase, which has the maximum magnitude (termed the max-phase), crosses the carrier last and causes the last switching transition in the inverter switching states in a two-level modified reference PWM scheme [9, 2]. Thus the switching periods of the active vectors can be determined from the max-phase and min-phase sampled reference phase voltage amplitudes in a two-level inverter scheme [3]. The SPWM technique, for multilevel inverters, involves comparing the reference phase voltage signals with a number of symmetrical level-shifted carrier waves for PWM generation [5]. It has been shown that for an \( n \)-level inverter, \( n-1 \) level-shifted carrier waves are required for comparison with the sinusoidal references [5]. In this paper, a simple technique to determine the offset voltage (to be added to the reference phase voltage for PWM generation for the entire modulation range) is presented, based only on the sampled amplitudes of the reference phase voltages. The idea behind the proposed scheme is to determine the sampled reference phase, from the three sampled reference phases, which crosses the triangular first (first-cross) and the reference phase which crosses the triangular carrier last (third-cross). Once the first-cross phase and third-cross phase are identified, the principles of offset calculation of equation (1), for the two-level inverter, can easily be adapted for the multilevel modified reference PWM generation scheme. The proposed modified reference PWM technique presents a simple way to determine the time instants at which the three reference phases cross the triangular carriers. Fig. 5 and Fig. 6 illustrate about the Modified reference and modified carrier modulation techniques with multi carriers for a three phase configuration.

V. SIMULATION RESULTS

The circuit diagram of 5-level Cascaded H-bridge (CHB) inverter is shown in Fig. 7. The circuit consists of two H-bridges of \( V_{dc1}=V_{dc}=V_{dc} \) connected in Cascaded position and eight switches connected in the form of bridge which can be controlled by the gate signals generated by the control circuit. The five levels of the circuit are viz... +\( \frac{V_{dc}}{2} \), \( 0 \), \( -\frac{V_{dc}}{4} \) and \( -\frac{V_{dc}}{4} \).

A SIM of 0.5 H.P, 1425 rpm, 4.5 A is used as the motor load for single phase CHB topology. It consists of two individual DC sources of 15 V each and eight no’s of IGBTs used as switches connected in the form of two H-bridges. The firing pulses for the IGBTs are generated using the proposed modulating technique i.e. Offset voltage injected reference with U-type carrier (OVPWM) also termed as Modified SVPWM.

![Fig. 7 single phase 5-level Cascaded H-bridge inverter fed SIM](image)
For the level \( \frac{V_{dc}}{2} \), the switches to be made ON are \( S_1, S_2, S_3 \) and \( S_4 \), and the current path is \( V_{dc}(+ve) \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow V_{dc}(-ve) \).

For the level \( \frac{V_{dc}}{2} \), the switches to be made ON are \( S_2, S_3, S_4 \) and \( S_1 \), and the current path is \( V_{dc}(-ve) \rightarrow S_2 \rightarrow S_3 \rightarrow S_4 \rightarrow V_{dc}(+ve) \).

For the level \( -\frac{V_{dc}}{2} \), the switches to be made ON are \( S_2, S_3, S_4 \) and \( S_1 \), and the current path is \( V_{dc}(+ve) \rightarrow S_2 \rightarrow S_3 \rightarrow S_4 \rightarrow V_{dc}(-ve) \).

The switching sequence of the inverter is shown in Table 2.

<table>
<thead>
<tr>
<th>Voltage Levels</th>
<th>( S_1 )</th>
<th>( S_1' )</th>
<th>( S_2 )</th>
<th>( S_2' )</th>
<th>( S_3 )</th>
<th>( S_3' )</th>
<th>( S_4 )</th>
<th>( S_4' )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>(+\frac{V_{dc}}{4})</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>(+\frac{V_{dc}}{2})</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>(+\frac{V_{dc}}{4})</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
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<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>(-\frac{V_{dc}}{4})</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>(-\frac{V_{dc}}{2})</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>(-\frac{V_{dc}}{4})</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
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<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

By switching on the corresponding switches in the circuit as per the given sequence, the output is as shown in Fig 8 (a) to (d) for resistive load of 373 W and Single phase induction motor respectively. The resistive load chosen as 373 W, which is equal to 0.5 H i.e. 0.5 X 746 W.

Fig 8 (c) & (d) Output current FFT of 5-Level CHB Inverter with resistive load (373 W) & SIM on no load

Fig 8 (a) & (b) Output voltage FFT of 5-Level CHB Inverter with resistive load (373 W) & SIM on no load

It is observed that the output current is more sensitive to load variations. For resistive load, voltage and current are in phase. For non-linear load like induction motor, current THD is more around 40% and voltage parameters remains same either for linear load or non-linear load.

### VI. Hardware Description

Based on the information brought forward from the earlier sections, it is decided that a Cascaded 5-level three phase topology of the OVPWM with U-type carrier PD modulating technique has given less harmonic reduction, when fed to a three phase induction motor. In this section, an attempt is made to develop a prototype of single phase Cascaded five level topology. By using Xilinx -- FPGA Spartan 3E board, the firing pulses are generated for the IGBTs in the topology, with the help of the equivalent VHDL code written and embedded in FPGA in the environment of ISE 12.0. The entire structure output is fed to a single phase induction motor (SIM), the input voltage and current harmonic spectrum is obtained with the help of YOKOGOWA precision power Analyzer WT1800.

The proposed modulating signals are generated by writing the VHDL code and embedded in Xilinx FPGA Controller board by using ISE 12.1 software. The screen shots are obtained from the simulation of VHDL code using Modelsim 6.0 software.

![Fig 9 Triggering pulses for 8 IGBTs using OVPWM](image_url)

Triggering pulses are represented in Fig 9 for the two H-bridges (i.e. eight IGBTs). The respective PWM pulses are
generated with the help of offset voltage injected in sinusoidal reference signals as shown in Fig 10; these reference signals are compared with the level shifted four U-type carrier signals shown in Fig 11.

Fig. 10 Modified Reference Signals used in OVPWM

Fig. 11 Level shifted U-type PD carrier signals used in OVPWM

VII. Experimental Description

i) INPUT -AC SOURCES
Two Transformers of 230V/110V –0-110V for two individual sources of two H-bridges
Two Transformers of 230V/12V, 8V for two H-bridges, to supply $V_{cc}$ for various ICs used as optocouplers, comparators etc.

- Bridge rectifier (MB 356)
  - Voltage rating - 600V
  - Current rating – 35A

ii) CAPACITORS AS DC SOURCES
Two sets of Capacitors for two H-bridges 2200 μF/450 V parallel with 330 μF / 450 V

iii) FSBB20CH60F (IGBT MODULE)
- UL Certified No. E209204 (SPM27-CA package).
- 600V-20A 3-phase IGBT Inverter Bridge including control ICs
  for gate driving and Protection

iv) FPGA (XILINX SPARTAN 3E)
To generate the firing pulses of proposed modulating technique in
ISE 12.1 with the help of VHDL programming

v) OTHER ICs FOR ISOLATION
To provide isolation from Low voltage side i.e. FPGA side and High Voltage side i.e. H-bridge Inverter side

- OPTOCOUPLERS (4506)
The relevant figures of voltage and current are shown in Fig. 14 and 15. The resultant voltage and current are presented in Fig. 16.

![Fig. 15: Output voltage and current of the prototype](image)

![Fig. 16: Numerical description from Power Analyzer YOKOGAWA WT1800](image)

### Experimental Results

**Topology:** Single phase Cascaded 5-level H-bridge Inverter

**Input Voltage (rms):** 230V (two individual dc sources of 162.5 V)

**Switching Frequency:** 10 KHz

**Nature of output:** m-levels i.e. 5-levels

**Load:** Single phase induction motor of capacitor start type (0.5 HP, 230 V, 4.5 A, 1425 rpm, 50 Hz) on No-Load

<table>
<thead>
<tr>
<th>M</th>
<th>Speed</th>
<th>Output Voltage</th>
<th>Output Current</th>
<th>Remarks</th>
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<tbody>
<tr>
<td>0.9</td>
<td>1492</td>
<td>207.3</td>
<td>22.45</td>
<td>3.2</td>
</tr>
<tr>
<td>0.8</td>
<td>1486</td>
<td>192.3</td>
<td>21.58</td>
<td>3.2</td>
</tr>
<tr>
<td>0.7</td>
<td>1482</td>
<td>158.7</td>
<td>20.67</td>
<td>3.2</td>
</tr>
<tr>
<td>0.6</td>
<td>1482</td>
<td>135.1</td>
<td>20.84</td>
<td>3.9</td>
</tr>
</tbody>
</table>

**Table 3: Experimental results of a prototype with SIM on No-Load**

<table>
<thead>
<tr>
<th>M</th>
<th>Speed</th>
<th>Output Voltage</th>
<th>Output Current</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.9</td>
<td>1490</td>
<td>220.42</td>
<td>21.3</td>
<td>3.19</td>
</tr>
<tr>
<td>0.8</td>
<td>1400</td>
<td>211</td>
<td>22</td>
<td>4.01</td>
</tr>
<tr>
<td>0.9</td>
<td>1450</td>
<td>230</td>
<td>21.20</td>
<td>4.25</td>
</tr>
<tr>
<td>0.9</td>
<td>1438</td>
<td>205</td>
<td>21.4</td>
<td>4.60</td>
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<tr>
<td>0.8</td>
<td>1490</td>
<td>196.33</td>
<td>22.02</td>
<td>2.64</td>
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<tr>
<td>0.8</td>
<td>1400</td>
<td>177</td>
<td>21</td>
<td>3.6</td>
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<tr>
<td>0.8</td>
<td>1370</td>
<td>170</td>
<td>22</td>
<td>4.0</td>
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<td>0.8</td>
<td>1422</td>
<td>193</td>
<td>21.5</td>
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<tr>
<td>0.8</td>
<td>1416</td>
<td>188.07</td>
<td>22.63</td>
<td>4.60</td>
</tr>
</tbody>
</table>

**Table 4: Experimental results of a prototype with SIM on Load**

By considering the economical aspects, a prototype for single phase cascaded topology is developed instead of three phase topology. Without altering its modulating technique proposed, the output of the Cascaded Multilevel inverter is fed to a Single phase induction motor. The results which justify with experimental implementation are also presented.

**VIII. CONCLUSION**

The single phase CHB multilevel inverter fed SIM is implemented with the OV PWM with U-type PD carrier modulating technique and the performance based parameters are tabulated. From the simulation results of SIM on load, it is also concluded that the machine runs beyond the rated current of 4.5 A for sometime till the overheating of the windings and melting of fuse after reaching its melting point because of temperature raise beyond the rated current. So, it is concluded that 4.5 A is the safety limit of the drawing current for safer operation and smooth running. Rated conditions of the machine also depend on the mechanical structure and power factor of the machine. It is known that small rated machines have very poor power factor. Hence it is decided that for hardware implementation a single phase induction motor of 230 V, 4.5 A, and 1425 rpm can be preferable, which gives a rated torque of 2.5 N.m. The result analysis is elaborated in tables 3 & 4.

Based on the single phase configuration experimental results, it can also be concluded that Three phase Cascaded Multilevel inverter fed three phase induction motor with proposed modulation technique i.e. Offset Voltage injected in
reference PWM with U-type carrier can give least THD in output voltage with nine levels, which is least amongst all the modified reference modulation techniques and Modified Carrier Modulating techniques.

IX. REFERENCES


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