A New Space Vector Modulation Scheme for Multilevel Inverters Which Directly Vector Quantize the Reference Space Vector

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Abstract—A new space-vector-based sigma delta modulation scheme for any general N-level voltage source inverter is proposed in this paper, which directly quantizes the reference space vector. The proposed scheme uses the sigma delta modulation with the quantizer implemented by the proposed space vector quantizer. A new scheme is proposed for directly quantizing the reference space vector to the multilevel inverter switching vectors without mapping it into two-level inverter vector space. Voronoi regions of the multilevel inverter vector space in the proposed space vector quantizer are defined as a parallelogram with the inverter switching vectors as its vertices. The property of the integer values of the inverter switching vectors in 60◦ coordinates is utilized for the direct vector quantization of the instantaneous reference voltage space vector. The proposed scheme is implemented for five-level inverters realized by an open-end-winding induction motor fed with two three-level inverters from either side having symmetrical dc-link voltages, and results are presented.

Index Terms—Digital modulation, harmonics, sigma delta modulator, space vector, vector quantization.

I. INTRODUCTION

MULTILEVEL inverters are extensively used for medium-voltage high-power industrial drive applications and grid-connected inverters for renewable energies. Voltage operation above classic semiconductor ratings, lower common mode voltages, near sinusoidal outputs, reduced voltage derivatives \(\frac{dv}{dt}\), voltages with reduced harmonic content, and increased efficiency are the main characteristics that have made multilevel inverters more popular [1]–[5].

The recent development of multilevel inverters has led to the introduction of many new simpler and flexible modulation schemes [3]–[6]. The modulation and control strategies in multilevel inverters can be broadly classified into voltage-level-based algorithm and space-vector-based algorithm. The space vector modulation schemes have wider linear modulation range, lower baseband harmonics, and convenience for digital implementation [3]–[5]. Compared with conventional orthogonal coordinate systems, the representation of the space vector in 60◦ coordinate systems reduces the computational complexity by eliminating fractional arithmetic [7]–[9]. The selection of the inverter switching vector and the calculation of the duration of these vectors in multilevel inverters can be simplified if the reference space vector is first mapped to the two-level inverter plane [10], [11]. In addition to the desired fundamental component, converters employing conventional deterministic modulation schemes have a power spectrum concentrated around the switching frequency and its harmonics, resulting in radiation of the electromagnetic interference and acoustic noise [12]. To spread the harmonic energy over a large frequency range, principles of random modulation have been widely applied to two-level inverters and also in three-level inverters [12]–[15].

Delta modulation and sigma delta modulation which uses the oversampling technique rather than Nyquist rate sampling of the reference input signal are also used in adjustable-speed drives for modifying the spectral characteristics [16]–[28]. Delta modulation found practical application for the control of resonant dc-link inverters in which the switches are commutated only when the dc bus resonates back to zero [16], [17]. Different sigma delta modulator based two-level three-phase inverter control schemes can be classified as a scalar sigma delta modulator [18], [19], a space vector modulation with a scalar sigma delta modulator [20], [21], a hexagonal sigma delta modulator [22]–[25], and a vector-quantized space-vector-based sigma delta modulator [26]–[28].

In adjustable-speed drives, the analog control signal is modulated and amplified by the voltage source inverter which is then demodulated by the high impedance offered by the inductance of the motor. Hence, in motor drive application, the inverter acts as a transmitter, and the motor acts as the demodulator analogous to the communication system with modulation [18]. The voltage source inverter has a discrete state output like digital systems, and it tries to approximate the input signal, which is a set of three-phase analog signals, by switching inverter discrete states at a high frequency. Therefore, the inverter’s behavior is similar to an oversampling analog-to-digital converter [22], [23]. Hence, the induction motor drive system can be considered as a communication system with digital modulation. This understanding prompts us to explore the possibility of adopting the techniques used in the context of digital communication systems to control multilevel inverters.

In digital communication, sigma delta modulators are used to achieve a higher resolution with a lesser number of bits by
spreading the quantization noise out of the signal bandwidth [29], [30]. The switching frequency in the sigma delta converters varies randomly, resulting in spreading of the output power spectrum. This will eliminate the concentration of energy at switching frequency harmonics which are present in the fixed frequency switching [29], [30]. By Shannon’s rate-distortion theory, a better result can always be achieved by coding vectors instead of scalars. For efficient quantization in digital communication and data compression, instead of processing the N different bits separately, as a scalar quantity, they can be treated as a single vector quantity with a magnitude and phase value for better result [31], [32]. This principle of vector quantization has been used in space-vector-based sigma delta modulation for multilevel voltage source inverters after mapping the reference space vector into the two-level space vector plane [27], [28].

This paper proposes a space vector modulation scheme which directly vector quantizes the reference space vector of the multilevel voltage source inverters in the sigma delta modulator without mapping. The property of the integer values of the inverter switching voltage space vectors in $60^\circ$ coordinate systems is utilized for vector quantization of the instantaneous reference space vector directly. The proposed scheme is implemented for five-level inverters realized by an open-end-winding induction motor fed with two three-level inverters from either side having symmetrical dc-link voltages, and results are presented.

II. PRINCIPLES OF THE PROPOSED SCHEME

Figs. 1 and 2 show the block diagram and flowchart of the proposed space vector modulation scheme with direct vector quantization. The scheme uses two sigma delta modulators for each resolved component of the instantaneous reference voltage space vector $\mathbf{V}_{\text{Ref}}(V_m, V_n)$ in $60^\circ$ coordinates. Each sigma delta modulator consists of a difference node, a discrete time integrator, and a space vector quantizer. The input to the integrator is the difference between the input signal $\mathbf{V}_{\text{Ref}}$ and the quantized output value $\mathbf{V}_{\text{S}}(V_{Sm}, V_{Sn})$. This error is summed up in the integrator to produce the integrated error vector $\mathbf{V}_E(V_{Em}, V_{En})$. The integrated error vector ($\mathbf{V}_E$) is random in nature and can be mapped into the multilevel inverter voltage space vector. These integrated error vectors ($\mathbf{V}_E$) can be quantized to the nearest inverter switching vectors by the principle of vector quantization. In the proposed space vector quantizer, the coordinates of the four inverter voltage space vectors forming the vertices of the parallelogram enclosing the integrated error vector ($\mathbf{V}_E$) in $60^\circ$ coordinates are determined. Out of these four inverter voltage space vectors, the inverter voltage vector nearest to the integrated error vector $\mathbf{V}_E$ is selected as the switching vector. The inverter switching vectors obtained in $60^\circ$ coordinates from the space vector quantizer are converted into the corresponding multilevel inverter switching states. The scheme is described in detail in the following sections.

A. Switching Vectors of Five-Level Inverters in $60^\circ$ Coordinate Systems

The three-phase reference signal is transformed into the $60^\circ$ coordinate system using the following relationship:

$$
\begin{bmatrix}
V_m \\
V_n
\end{bmatrix} =
\begin{bmatrix}
1 & -1 & 0 \\
0 & 1 & -1
\end{bmatrix}
\begin{bmatrix}
V_a \\
V_b \\
V_c
\end{bmatrix}
$$

where $[V_m, V_n]^T$ are the coordinate values of $V_{\text{Ref}}$ in the $60^\circ$ coordinate system and $[V_a, V_b, V_c]^T$ are the coordinate values of the reference space vector $\mathbf{V}_{\text{Ref}}$ in three-phase systems. Fig. 3 shows the switching vectors of the five-level inverter in the $60^\circ$ coordinate system. The switching vectors of the inverter in the $60^\circ$ coordinate system have only integer values, whereas it has fractional values in the Cartesian coordinate system. The representation of the space vector in the $60^\circ$ coordinate system
Fig. 3. Switching vectors of the five-level inverter in the 60° coordinate system.

reduces the computational complexity by eliminating fractional arithmetic [7]–[9]. The multilevel inverter space vector diagram can be divided into different parallelograms (Fig. 3).

Fig. 4. Vectors of the five-level inverter in 60° coordinate in sector 1 and the reference space vector.

B. Proposed Space Vector Quantizer

In the proposed scheme, the principle of vector quantization is used to implement the quantizer in the sigma delta modulator. A vector quantizer maps \( k \)-dimensional random vectors in the vector space \( R^k \) into a finite set of vectors \( Y = \{ y_i : i = 1, 2, \ldots, N \} \). Each vector \( y_i \) is called a code vector or a codeword, and the set of all of the codewords is called a codebook. Associated with each codeword \( y_i \) is a nearest neighbor region called Voronoi region, and it is defined in [31] and [32] as

\[
V_i = \{ x \in R^k : ||x - y_i|| \leq ||x - y_j||, \text{ for all } j \neq i \} .
\]

For the vector quantization, the vector space is divided into nonoverlapping Voronoi regions, and each code vector will be the centroid of the particular Voronoi region. All of the random vectors in a particular region are rounded to a single code vector in each Voronoi region [31], [32]. The integrated error space vector \((V_{E})\) of the proposed sigma delta modulator is random in nature, and these can be mapped into the multilevel inverter voltage vector space. These integrated error space vectors \((V_{E})\) can be quantized to the nearest inverter switching vectors by the principle of vector quantization.

C. Determination of Switching States

The inverter switching vector obtained from the space vector quantizer in 60° coordinates has to be mapped to switching states of the multilevel inverter in the \( abc \) frame. Fig. 5 shows the switching states of the five-level inverter without the redundant states in the \( abc \) frame. It can be noted that, in sectors 1 and 2, phase C values are zero. Similarly, phase A values are zero in sectors 3 and 4, and in sectors 5 and 6, phase B values are zero. The switching states are transformed to 60° coordinates by \( V_m = V_a - V_b \) and \( V_n = V_b - V_c \). Utilizing the occurrence of zero level in each phase in different sectors, reverse transformation of the 60° coordinates of the inverter voltage vector to the corresponding switching states is possible.
In sectors 1 and 2, phase C value $V_c = 0$ results in $V_b = V_n$ and $V_a = V_m + V_n$. As $V_a = 0$ in sectors 3 and 4, $V_b = -V_m$, and $V_c = -V_m - V_n$. Similarly, in sectors 5 and 6, $V_b = 0$; hence, $V_a = V_m$, and $V_c = -V_n$. This conversion of switching vectors in 60° coordinates into switching states in the $abc$ frame is shown in Table I.

This proposed scheme works efficiently with higher level inverters as the inverter voltage vectors are located more closely in higher level inverters, resulting in a lesser quantization step size in the space vector quantizer. With lesser quantization step size, the integrated error space vector ($V_E$) follows the reference space vector $V_{Ref}$ more closely. The proposed space vector modulation scheme with direct vector quantization in this paper has lesser computational overhead compared to the schemes proposed in [26]–[28]. This is due to the fact that, in this scheme, the reference space vector is directly quantized in the sigma delta modulator without mapping and the Voronoi regions directly obtained from the 60° coordinate of the error space vector. The coordinates of the four inverter switching vectors enclosing the error vector are obtained by finding the integer values of the error vector.

![Fig. 6. Trajectory of the integrated error vector and the reference space vector.](image)

Fig. 6 shows the trajectory of the integrated error space vector and the reference space vector. The selection of the inverter switching vector in the proposed scheme will be always nearest to the integrated error vector in the sigma delta modulator which closely follows the input reference space vector. The coordinates of the four inverter voltage space vectors encircling the integrated error vector ($V_E$) forming the vertices of parallelogram are determined as explained in the preceding section. Out of these four inverter voltage space vectors enclosing the tip of the integrated error space vector, the inverter voltage vector nearest to $V_E$ is selected as the switching vector in each sampling period by calculating the Euclidian distances of these vectors from $V_E$. Unlike the SVPWM scheme, only one inverter voltage space vector is switched in each sampling period in the proposed scheme.

### TABLE I

<table>
<thead>
<tr>
<th>Sector</th>
<th>Switching States</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 and 2</td>
<td>$V_a = V_m + V_n$</td>
</tr>
<tr>
<td>3 and 4</td>
<td>$0$</td>
</tr>
<tr>
<td>5 and 6</td>
<td>$V_m$</td>
</tr>
</tbody>
</table>

![Fig. 7. Five-level inverter realized by an open-end-winding induction motor fed with two three-level inverters from either side having symmetrical dc-link voltages.](image)

![Fig. 8. Integrated error space vector ($V_E$) and space vector quantizer output ($V_S$) from the DAC output of the dSPACE DS 1104 RTI platform for the proposed space vector modulation scheme with direct vector quantization. Trace 1: integrated error space vector ($V_E$) signal in the $M$-axis—$V_{Em}$. Trace 2: space vector quantizer output ($V_S$) signal in the $M$-axis—$V_{Sm}$. Trace 3: integrated error space vector ($V_E$) signal in the $N$-axis—$V_{En}$. Trace 4: space vector quantizer output ($V_S$) signal in the $N$-axis—$V_{Sn}$. Scale: Y-axis: 5 V/div; X-axis: 10 ms/div.](image)

**III. EXPERIMENTAL SETUP AND RESULTS**

**A. Power Circuit**

The proposed scheme can be used in any multilevel inverter configuration. In the present work, the proposed scheme is implemented for the five-level inverter realized by an open-end-winding induction motor fed with two three-level inverters from either side having symmetrical dc-link voltages, as shown in Fig. 7 [33], [34]. Each three-level inverter configuration in the setup is realized by cascading two two-level inverters. It is used to drive a 2-hp three-phase induction motor with $V/f$ control for different modulation indexes covering different speed ranges. The proposed scheme is implemented using dSPACE DS 1104 RTI at a constant sampling frequency of 20 kHz.

**B. Results and Discussion**

Fig. 8 shows the signals corresponding to the integrated error vector $V_E$ and space vector quantizer output vector ($V_S$) obtained experimentally from the dSPACE DS 1104 RTI.
traces \((\text{vector resolved in the level inverter-A})\). Similarly, the last three traces correspond to \(N\)-\([5V/\text{div}];\) direct vector quantization. The first and third traces platform for the proposed space vector modulation scheme with \(3\) and \(4\) (i.e., effective pole voltage of cascaded three-level inverter-B). Fourth and fifth traces: switching signals for inverters \(1\) and \(2\). Third trace: sum of traces \(1\) and \(2\) (i.e., effective pole voltage of cascaded three-level inverter-A). Sixth trace: sum of traces \(3\) and \(4\) (i.e., effective pole voltage of cascaded \((\text{three switching voltage levels. The difference between these two traces})\) \((V_{S2O} - V_{AO})\) is the effective pole voltage of the five-level inverter realized in the open-end-winding induction motor which is shown as trace \(3\). This has five switching voltage levels. Even though sampling was done at a constant frequency of \(20\) kHz, the switching frequency in the proposed scheme is not constant since the proposed scheme is basically a pulse density modulation scheme \([26]\). The number of pulses in a given time window is proportional to the average value of the input reference signal. Individual pulsewidths are quantized to multiples of the modulator clock period. The average number of switching in the proposed scheme is lesser than that of the SVPWM scheme since pole voltage \((V_{AO})\) clamped toward \(V_{DC}\) most of the clock cycles during the positive peak period and zero during the negative peak period of the fundamental reference sinusoidal signal. The pole voltage switches rapidly between \(V_{DC}\) and zero during the zero crossover of the fundamental sinusoidal signal so that the average pole voltage will be zero.

![Fig. 9. Switching signals for three phases from the DAC output of the dSPACE DS 1104 RTI platform for the proposed space vector modulation scheme with direct vector quantization. Scale: \(Y\)-axis: \(5\) V/div; \(X\)-axis: \(10\) ms/div.](image)

![Fig. 10. Switching signals for individual two-level inverters for the proposed scheme in five-level mode of operation. First and second traces: switching signals for inverters \(1\) and \(2\). Third trace: sum of traces \(1\) and \(2\) (i.e., effective pole voltage of cascaded inverter-A). Fourth and fifth traces: switching signals for inverters \(3\) and \(4\). Sixth trace: sum of traces \(3\) and \(4\) (i.e., effective pole voltage of cascaded three-level inverter-B). Scale: \(Y\)-axis: \(5\) V/div; \(X\)-axis: \(10\) ms/div.](image)

![Fig. 11. Experimental waveforms of the proposed scheme in five-level mode of operation. First trace: pole voltage of three-level inverter-A \((V_{A2O}); Y\)-axis: \(250\) V/div. Second trace: pole voltage of three-level inverter-B \((V_{AO}); Y\)-axis: \(250\) V/div. Third trace: effective pole voltage of the five-level inverter \((V_{A2O} - V_{AO}); 200\) V/div. Fourth trace: motor phase voltage \((V_{A2A4}); Y\)-axis: \(100\) V/div. Fifth trace: motor phase current \((I_A); Y\)-axis: \(2.5\) A/div; \(X\)-axis: \(10\) ms/div.](image)
Fig. 12. Waveforms of the proposed scheme in four-level mode of operation. First trace: pole voltage of cascaded inverter-A \( (V_{A2O}) \); Y-axis: 50 V/div. Second trace: pole voltage of cascaded inverter-B \( (V_{A4O}') \); Y-axis: 100 V/div. Third trace: effective pole voltage \( (V_{A2O} - V_{A4O}') \); Y-axis: 100 V/div. Fourth trace: motor phase voltage \( (V_{A2A4}) \); Y-axis: 50 V/div; X-axis: 10 ms/div.

Fig. 12 shows the experimental waveforms of the proposed scheme in four-level mode of operation. The first two traces are the pole voltages of the two three-level inverters \( (V_{A2O} \text{ and } V_{A4O}') \). The pole voltages of three-level inverter-A have two switching voltage levels, and three-level inverter-B has three switching voltage levels. The difference between these two traces \( (V_{A2O} - V_{A4O}') \) is the effective pole voltage which has four switching voltage levels (third trace). Motor phase voltage \( (V_{A2A4}) \) is shown as the last trace.

The spectra of the proposed scheme and the SVPWM scheme are shown in Fig. 13. The harmonic spreading effect of the switching noise can be observed in the spectrum of the proposed scheme since the switching frequency in the sigma delta modulator varies randomly. The harmonic spikes are 25–15 dB less in the proposed scheme at audio frequency compared to the SVPWM scheme.

Fig. 14 shows the comparison of the total harmonic distortion (THD) characteristics of the proposed scheme, SVPWM scheme, random PWM scheme, and scalar sigma delta modulation scheme. THD characteristics are evaluated experimentally with different modulation indexes for the phase voltage in the four schemes. It shows that the THD of the proposed scheme is much lesser than the THDs of the SVPWM scheme and scalar sigma delta modulation scheme for all modulation indexes since the harmonic spectrum is spread without any large concentrations at discrete frequencies in the proposed scheme compared to the other two schemes. The THD of the proposed scheme is comparable with that of the random SVPWM scheme, and it is slightly higher than that of the random SVPWM scheme at higher modulation indexes as the average switching frequency reduces in the proposed scheme at higher modulation indexes.

The performance of the proposed scheme is compared with the performances of different pulsewidth modulation schemes. To compare the switching losses in different schemes, the switching frequency \( (f_{sw}) \) is normalized with respect to the carrier frequency \( (f_c) \) to suppress the effect of sampling frequency. The normalized switching frequency is defined as \( v = f_{sw} / f_c \). The other parameters used to evaluate the performances of the schemes are switching frequency distortion product (SFDP) and switching loss factor (SLF) [19], [24], [25]. SFDP is defined as the product of the normalized switching frequency \( (v) \) and the harmonic distortion \( d_{harm} = \sqrt{P_{harm}} \), where \( P_{harm} \) is the power of harmonics. SLF is used to compare the switching losses in different switching schemes in the inverter, which is defined as \( SLF = \Delta P_{sw} / m_f \), where \( \Delta P_{sw} \) is the switching loss per fundamental period and \( m_f \) is the ratio of the carrier frequency and fundamental frequency [24].

Fig. 15 shows the comparison of the normalized switching frequencies of the proposed scheme with space vector PWM...
switching frequency, SFDP, and SLF. The modulation indexes (Fig. 17). The performance of the proposed scheme is better than the performances of the SVPWM and PWM schemes, except at middle ranges of modulation indexes, resulting in lesser efficiency at these ranges. SLF is lesser for the proposed scheme compared to the SVPWM scheme. SFDP is higher for the proposed scheme at middle ranges (and higher) modulation indexes.

Fig. 15. Comparison of normalized switching frequencies of the proposed scheme with space vector PWM and sine triangle PWM at different modulation indexes.

Fig. 16. SFDP versus modulation index of the proposed vector SDM, SVPWM, and SPWM.

Fig. 17. Plot of SLF versus modulation index for the proposed vector sigma delta modulator, SVPWM, and SPWM.

IV. Conclusion

The proposed scheme integrates the digital signal processing techniques of space vector modulation, sigma delta modulation, and vector quantization. This results in faster implementation with small memory space using low-cost general-purpose DSP or FPGA. The proposed scheme works more efficiently with higher level inverters as the inverter voltage vectors are located more closely, resulting in lesser quantization step size in the space vector quantizer. The proposed scheme is implemented for the five-level inverter-fed open-end-winding induction motor, and results have been presented. The performance of the proposed scheme has been compared with the performances of the PWM schemes at different speed ranges. The number of switching in the proposed space vector modulation scheme with direct vector quantization is lesser than the SVPWM scheme since it is a pulse density modulation scheme. The spectrum of the proposed space vector modulation scheme with direct vector quantization spreads uniformly without any concentration of switching noise. The harmonic spikes are 25–15 dB less in the proposed scheme at audio frequency compared to the SVPWM scheme. The performance of the proposed scheme is better than the performances of the SVPWM and PWM schemes at the rated operating speed of the motor in terms of THD, normalized switching frequency, SFDP, and SLF.

REFERENCES


