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Abstract—The multi-level inverter is widely used in high-power and high-voltage applications. Multi-level inverters use a large number of switches for high power conversion, resulting in increased system’s fault probability. To ensure stable operation of the system, several fault diagnosis methods have been carried out by researchers. In this article, a fault diagnostic system in a multi-level inverter using wavelet modulus maxima is developed. The working situation of the power devices of a five-level diode-clamped multi-level inverter drive system under an open-circuit fault is analyzed through MATLAB (The MathWorks, Natick, Massachusetts, USA) simulation. The wavelet modulus maxima of output phase voltages are used to detect faulty phase (leg), and wavelet modulus maxima of DC bus currents are used to detect fault type and fault switch. Wavelet analysis is used for feature extraction, which can be used as input to the expert system to develop a fault identifier. The open-circuit fault on the five-level diode-clamped multi-level inverter of power devices is carried out experimentally. The experimental prototype is developed to validate the fault analysis with simulation results.

1. INTRODUCTION

High power converters have found widespread applications in industry [1, 2]. The converter topologies for high-power (in MW) motor drives are classified as indirect methods using a cyclo-converter and direct methods using voltage source inverters (VSIs) and current source inverters (CSIs). The high-power VSI fed drives have undergone significant development in comparison to CSI topologies [3] with improved overall performance. VSIs in the form of multi-level inverters (MLIs) are more popular in the market due to their high power capability with low output harmonics and low commutation losses, reduced $dv/dt$, reduced common mode voltages, and converter modularity [4, 5]. Multi-level topology uses pulse-width modulation (PWM) converters and fast switching medium power devices for high-voltage, high-power applications [6]. The diode-clamped MLI (DCMLI) is the most attractive topology, as it has high converter efficiency and low switching frequency and is also economical [7, 8].
The reliability of MLI systems used in high-power drive applications is important. As the MLI has large number of switches, the probability of faults (open or short circuit of switch) increases. Faults should be detected as soon as possible to avoid vital damage. The various fault modes of a VSI system for an induction motor were investigated in [9]. The conventional protection systems are passive devices, such as fuses, overload relays, and circuit breakers, to protect inverter systems and induction motors. Power sources from the MLI system are disconnected by the protection devices whenever a fault occurs, interrupting the process and causing heavy economic losses.

To maintain continuous operation of an MLI system, knowledge of fault behavior, fault prediction, and fault diagnosis are necessary. The diagnosis solutions found in the literature has been divided into two main groups: (1) switch measurement and (2) output waveform analysis. The variations in monitored output waveforms are observed under an open switch fault from that of normal condition (see Figures 12 and 13 below). The variation in the waveform could visually be distinguished but is difficult to rate as an important characteristic, and it needs a high correlation coefficient for classifying the fault. The variation in waveform can be due to the occurrence of a fault or due to system parameter variations, such as increases or decreases of load, voltage fluctuations, etc. The fault identifier based on waveform analysis may mal-operate for system parameter variation, as it can non-distinguish between system
parameter variations or fault. A survey on fault operation in MLIs was presented in [10], where the spectral analysis was reported to be faster than waveform analysis. The fault gives rise to a transient condition, which is marked by the presence of harmonic variations; thus, feature extraction using a signal transformation technique with suitable diagnostic parameters called signatures is obtained from the monitored waveform(s) in the frequency domain. The most commonly used signal processing tools include discrete Fourier transform (DFT), short-time Fourier transform (STFT), and wavelet transform (WT). A fault diagnostic system for MLIs using fast Fourier transform (FFT) for feature extraction and neural networks (NNs) for classification was explained in [11], but the classification performance decreases when the operating point is different from the training set. Also, more training data are needed for a wide range of operation. The prediction of switch faults in the brushless excitation system of synchronous generators by second and fifth harmonic components as diagnostic indices using DFT was proposed in [12]. DFT provides accurate information of frequency components, but the time information of the transients in the signal is totally lost [13]. STFT provides a compromise between time and frequency resolution when the signals are decomposed, but the size of window is not adaptive. These drawbacks can be overcome by WT, as it provides non-uniform division of the frequency domain; i.e., WT uses short windows at high frequencies and long windows at low frequencies. This helps to analyze effectively the signal in both frequency and time domains.

Fault tolerance is an important area considering the reduction of downtime in industrial processes. The performance of inverter is improved by a fault tolerant scheme [14], where gate control signals are modified according to failure modes when some of the power devices fail. The fault is detected by a built-in de-saturated detector commercial gate drive chip using voltage sensing. A fault tolerant control framework for a periodic switched non-linear system was proposed in [15], where an adaptive model free sliding-mode observer was developed for fault detection. For discrete faults, the adaptive model requires more than ten cycles for identification. The fault-tolerant features of conventional neutral point clamped (NPC) MLIs were discussed in [16, 17]. Fault diagnosis and neutral point voltage control during a fault condition in a three-level DCMLI using Park’s vector was proposed in [18]. In [19], the fault-tolerance of four-level flying-capacitor MLI, which can maintain full converter operation even under a single-switch fault per phase conditions, is realized; however, due to the complex design,
cost, and size concern of the fault tolerant system, it can be an impractical solution for most MLIs.

Condition monitoring and automatic fault diagnosis are mostly based on theory analysis, such as artificial intelligence (AI) based techniques, NNs, expert systems, etc. The features for fault classification extracted from the proposed diagnosis system can be used to train expert systems (artificial neural networks [ANNs] or fuzzy logic) to develop a fault identifier. A fault diagnostic system for rotary machines based on fuzzy NNs was developed in [20]. With the use of principal component analysis (PCA) for feature extraction process, the NN input size can be reduced [21], but six cycles are required to clear a short switch fault and nine cycles for an open switch fault. Histogram analysis is used for feature extraction to obtain input for NNs [22]. Using this algorithm, various possible faults can be detected accurately, but a fault is detected and removed after six cycles. The fault diagnostic and protection technique for interior permanent magnet (IPM) motor drives using WT was reported in [23] to be less complicated and faster as the trip signal is initiated within two cycles of fault occurrence. Wavelet analysis finds a wide range of applications in electrical engineering fields, such as de-noising in signal processing, fast transient analysis (e.g., inrush/faults in a transformer) [24], fault identification and diagnostics in electrical machine or drives [25], permanent magnet (PM) brushless DC motors [26], and power electronic problems (e.g., harmonic analysis), etc.

The use of wavelet analysis for fault diagnosis for power electronics is not much reported in the literature. The literature reports the use of the wavelet modulus maxima (WMM) technique mainly for fault detection and fault location on transmission lines. This article proposes a novel technique based

**FIGURE 5.** WMM analysis of phase voltages under switch $S_{x2}$ opened.

**FIGURE 6.** WMM analysis of phase voltages under switch $S_{x3}$ opened.
on the application of wavelet analysis (WMM) for switch fault detection (open fault) of DCMLIs. In this article, the wavelet maxima of the first scale high-frequency details of fault phase voltages and DC bus currents show distinctive features between fault and normal conditions. A five-level DCMLI model feeding an induction motor is developed in MATLAB (The MathWorks, Natick, Massachusetts, USA). The phase voltages and DC bus currents under normal and faulty (open-circuit fault of a switching device) operations are obtained, which are used as an input to wavelet analysis for feature extraction. WT is first applied to decompose the signals into a series of wavelet components, each of which is a time-domain signal that covers specific frequency band. The maxima of the wavelet components are calculated to provide signatures for fault detection. The results show that the wavelet techniques lead to a new way for the switch fault identification and protection of DCMLIs. The proposed method based on wavelet analysis is faster, as a particular set of building blocks, called wavelets. Equations (1) and (2) illustrate the difference between FT and WT: small symbols.

\[
\hat{f}(\omega) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\infty} f(t) e^{-i\omega t} dt, \quad (1)
\]

\[
Wf(a, b) = \int_{-\infty}^{\infty} f(t) \bar{\psi}_{a,b}(t) dt. \quad (2)
\]

TABLE 2. Feature for fault detection

<table>
<thead>
<tr>
<th>Signal</th>
<th>Simulated analysis</th>
<th>Hardware analysis</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Normal</td>
<td>Normal</td>
</tr>
<tr>
<td></td>
<td>( S_{s_2} ) opened</td>
<td>( S_{s_2} ) opened</td>
</tr>
<tr>
<td>Phase A</td>
<td>WMM = 121</td>
<td>WMM \approx 0</td>
</tr>
<tr>
<td>Phase B</td>
<td>WMM = 121</td>
<td>WMM = 121</td>
</tr>
<tr>
<td>Phase C</td>
<td>WMM = 121</td>
<td>WMM \approx 0</td>
</tr>
<tr>
<td>DC bus current ( I_{d_0} )</td>
<td>WMM \approx 0.3</td>
<td>WMM \approx 0.3</td>
</tr>
<tr>
<td>DC bus current ( I_{d_1} )</td>
<td>WMM \approx 0.3</td>
<td>WMM \approx 0.3</td>
</tr>
<tr>
<td>DC bus current ( I_{d_0} )</td>
<td>WMM \approx 0.3</td>
<td>WMM \approx 0.3</td>
</tr>
<tr>
<td>DC bus current ( I_{d_1} )</td>
<td>WMM \approx 0.3</td>
<td>WMM \approx 0.3</td>
</tr>
<tr>
<td>DC bus current ( I_{d_2} )</td>
<td>WMM \approx 0.3</td>
<td>WMM \approx 0.3</td>
</tr>
</tbody>
</table>

MLIs use a large number of switching devices, which affect the circuit operation significantly. Switching device failure is often a cause of circuit dysfunction. Many factors lead to failure of switching power devices, and the disabled device can be either short circuited or open circulated depending on different causes and device types. This article aims at a single switch open-circuit fault in an MLI. If a power supply or element in the self-drive circuit of each switch is invalid, it causes an abnormal trigger pulse to the corresponding switch. The switch cannot work normally, and the fault is defined as a losing drive pulse (LDP) fault. LDP and open circuit faults have similar fault features in output waveforms.

The relationship between output voltage \( V_{o0} \) and switching states (shown in Table 1) indicates one switching state for a corresponding output voltage. Non-conduction (open) of switching devices causes loss of some switching states and the corresponding desired voltage levels. Similarly, when clamping diodes open, the clamping ability and some switching states are lost, with the possibility of damaging the switching devices due to voltage across the switch exceeding the rating of device. Thus, the device open failure fatally impacts the circuit operation.

The identification of signature patterns under faults obtained from WT has proven to be more reliable compared to Fourier transform [27]. WT is a technique to represent signals in time-frequency domains simultaneously with different set of building blocks, called wavelets. Equations (1) and (2) illustrate the difference between FT and WT [27, 28]:

\[
\hat{f}(\omega) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\infty} f(t) e^{-i\omega t} dt, \quad (1)
\]

\[
Wf(a, b) = \int_{-\infty}^{\infty} f(t) \bar{\psi}_{a,b}(t) dt. \quad (2)
\]

2. SWITCH FAULTS ANALYSIS IN INVERTER

Several studies have reported on multi-level topology for variable-speed motor drive applications. A three-phase five-level DCMLI [1], shown in Figure 1, is used in the research work for driving the induction motor. Table 1 shows the output voltage levels possible for one phase of the inverter, with DC-link voltage \( V_o \) as a reference. State condition 1 is considered as the switch being on and 0 for off switch. For a five-level inverter, a set of four switches are on at any given time.
In Eq. (2), $\psi_{a,b}(t)$ denotes continuous wavelets or a function that is a translated (shifted with time) and dilated (scaled or changed frequency) version of mother wavelet $\psi(t)$, as shown in Eq. (3):

$$
\psi_{a,b}(t) = \frac{1}{\sqrt{a}} \psi \left( \frac{t - b}{a} \right), \quad a, b \in \mathbb{R} \text{ and } a \neq 0.
$$

(3)

The continuous signals are sampled into a series of discrete sequences using WT. In dyadic discrete WT (DWT), $a$ is the dilation parameter of wavelet function $\psi_{a,b}(t)$ and is $2^j$, where $j$ is decomposition level; $b$ is shifting parameter given by $k2^j$, where $j, k \in \mathbb{Z}$; and $\mathbb{Z}$ is the set of positive integers. Signals are decomposed into two parts, approximations ($c_n$) and details ($d_n$) on each scale, and the next resolution decomposition is an iterative process.

The multi-resolution property is suitable for analyzing transient signals and has fast calculation algorithms that are based on a filter bank. For better time location and information, the ‘a’ trous structure without a down-sampling block after the high-pass filters is shown in Figure 2, where $H_0$ and $H_1$ are low-pass filter and high-pass filter, respectively. The output of high-pass filters are the WT of the original signal.

3. WMM

WT transfers a signal into the time-scale (frequency) domain with multi-resolution property used for analyzing transient signals. Wavelet analysis can also be useful for detection of edges and discontinuities in the signals using WMM. The absolute local maximum values of the WT of the signal are called WMM. The edge of a signal can be represented by WMM, if the basic wavelet is the first derivative of a smooth function. The polarity of the maxima shows a changed direction of the edge, and the value represents the change intensity of the edge. The WMM must satisfy the following relation $|W_{\text{max}}x(t)| \leq k a^\alpha$, where $W_{\text{max}}x(t)$ is WMM of signal $x(t)$, $k$ is a constant, $a$ is scale, and $\alpha$ is Lipschitz exponent. This relation means that the modulus maxima of an edge ($\alpha = 0$ or $\alpha > 0$) on the scales remain unchanged or increase with increase in scale.

4. EXPERIMENTAL SETUP AND RESULTS

A three-phase, five-level DCMLI, shown in Figure 1, feeding a 3-HP, four-pole, induction motor for a line voltage of 400 V is simulated in MATLAB Simulink. Figure 3 shows multi-level carrier-based sinusoidal PWM (SPWM) of 1-KHz switching frequency and the output voltages sampled at 5-KHz serves as input for discrete wavelet analysis. The five-level inverter is simulated for various conditions as normal (without fault) and switch opened. The signals used for wavelet analysis are phase voltages and DC bus currents.

Figure 4 shows WMM analysis of phase voltages under healthy condition. Figures 5 and 6 show WMM analysis of phase voltages when a switch of phase $A$ ($S_{a2}$) and phase $C$ ($S_{c3}$), respectively, are opened at 2.5 sec. The features from WMM analysis of phase $A$ voltage under $S_{a2}$ open switch fault seen in Figure 5 are different from the features of healthy condition of Figure 4. Similarly, for $S_{c3}$ open switch fault (Figure 6), the WMM analysis of phase $C$ voltage has variation, indicating that phase $C$ is affected by the fault. Thus, if any of the phases are affected by a fault (opening of switch), the WMM of phase voltage of the faulty phase shows variation. WMM analysis of phase voltages gives identification of the phase affected by the fault.

Figure 7 shows WMM analysis of DC bus currents under normal condition, whereas Figures 8 and 9 show WMM analysis of the DC bus currents when a switch of phase $A$ ($S_{a2}$) and phase $C$ ($S_{c3}$), respectively, are opened at 2.5 sec. The repeated features in every cycle, i.e., threshold or Maxima pattern, under switch fault condition are compared with healthy conditions. It is observed that if a switch is opened, the maxima of the DC bus current of affected links reduce and are negligible for a larger period of time as compared to the normal case. In comparison, if switch $S_{a2}$ is shorted, the WMM analysis of DC bus currents of affected links shows an increase, as shown in Figure 10. Thus, the fault type can be analyzed from DC bus currents.

To some extent, it is possible to identify the affected switch from WMM analysis of the DC bus current. If WMM features of the DC current of upper links ($I_{dc2}$ and $I_{dc1}$) show reduction, then upper switches $S_{a1}$, $S_{a2}$, $S_{c3}$, and $S_{a4}$ ($x$ indicates phase $a/b/c$) are affected and vice versa; i.e., if WMM of the DC current of lower links ($I_{dc2}$ and $I_{dc1}$) show reduction, then lower switches $S_{a1}$, $S_{a2}$, $S_{c3}$, and $S_{a4}$ are affected. If $S_{a1}$ is opened, then WMM of $I_{dc1}$ only reduces to zero; if $S_{c3}$, $S_{a3}$, and $S_{a4}$ are opened, then WMM of $I_{dc2}$ and $I_{dc1}$ varies; if $S_{a4}$ is opened, then WMM of $I_{dc2}$ only reduces to zero; if $S_{a1}$, $S_{a2}$, and $S_{c3}$ are opened, then WMM of $I_{dc2}$ and $I_{dc1}$ varies.

The feature extraction obtained using WMM is tabulated in Table 2.

To verify the validity of the proposed topology, a five-level DCMLI laboratory prototype using MOSFET, shown in Figure 11, has been developed. To control the inverter system and generate the SPWM pulses, a digital signal processor (TMS320F2812 DSP, Texas Instruments Incorporated, Dallas, Texas, USA) was used. Phase $A$ voltage under switch $S_{a2}$ open condition from the experimental setup is shown in
FIGURE 7. WMM analysis of DC bus currents under no fault.

FIGURE 8. WMM analysis of DC bus currents under switch $S_{2}$ opened.
FIGURE 9. WMM analysis of DC bus currents under switch $S_{x'y'}$ opened.

FIGURE 10. WMM analysis of DC bus currents under switch $S_{x'2}$ shorted.
FIGURE 11. Experimental setup of MLI feeding induction motor.

Figure 12, which is similar to the phase voltage obtained by simulation, shown in Figure 3, only for a no-fault condition. Also, DC bus currents under switch $S_{a2}$ open condition from the experimental setup is shown in Figure 13. The signals from the experimental setup are stored and used as inputs for wavelet analysis. Figure 14(a) shows the effect of opening of the switch on phase voltage for $S_{a2}$ switch open fault, and Figure 14(b) is its WMM analysis. Figures 14(c) to 14(g) are the WMM analysis of DC bus currents. Thus, the results in Table 2 have been validated experimentally. A similar technique of fault detection and classification can be applied for any switch fault.
5. CONCLUSION

The article aims at a single-switch open-circuit fault in an MLI. A technique of wavelet analysis (WMM) is utilized to transform signals in the time-frequency domain to achieve features for detection and classification of fault. The simulation considerations have been validated by experimental results. The phase consisting of a faulty switch can be identified from the WMM pattern of phase voltages. The variation in phase voltage WMM from the normal is observed only for the phase affected by fault. The type of switch fault is resolved from the DC bus current WMM, which increases for a shorted switch and reduces to zero for a longer period for the switch opened. Moreover, to some extent, it is possible to analyze the switch affected by the fault from the WMM pattern of DC bus currents. The fault is diagnosed almost at the instant or within one cycle of occurrence of the fault depending on the instant of fault and switch operation. Thus, WMM analysis not only detects the faulty leg but also the fault type and faulty device to define the best post-fault strategy. It is possible to detect the exact moment when fault appears. Thus, the proposed wavelet-based fault diagnosis system in this research gives a better understanding of fault behavior and detection for MLI systems. The signatures obtained from the proposed diagnostic system can be used to train expert systems (ANN or fuzzy logic) to develop fault identifier.

REFERENCES


FIGURE 14. Experimental waveforms: (a) phase voltage under fault, (b) WMM analysis of (a), (c)–(g) WMM analysis of DC bus currents (X-axis: samples).
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