Full Adders for High-Speed/Low power Arithmetic Circuits: A Comparison

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Abstract
In this paper, interesting full adder circuits are reviewed and compared concerning speed, power consumption, and silicon area. A modified full adder is also investigated by combining hybrid logics, namely, pass transistor logic and branch based logic. This architecture uses two independent parts to generate SUM and carry signals. The results show that ultra low power evolution, very small propagation delay and small silicon area have been accomplished by this design comparing with conventional static CMOS full adder circuit. Moreover, implementation of this design into multi-bit adder provides the advantage of eliminating the need for extra inverters, saves much more silicon area, and has ultra small total power dissipation. The investigations have been made using 0.13um CMOS process.

Key words: full adder, arithmetic, CMOS logic, adders, transmission gate logic, pass transistor logic

1. Introduction

With tremendous growth in portable devices and evolution of the shrinking technology, research efforts in low-power microelectronics has been intensified and low-power VLSI systems have emerged as highly in demand. Today, the most important requirements in portable applications are small-area low-power high-throughput circuitry. Therefore, circuits with low power consumption become the major candidates for design of microprocessors and system-components whose functionality is majored by arithmetic operations [1, 2]. To execute an arithmetic operation, high amount of power is consumed for high speed operations.

Therefore, designers are faced with more constraints such as high speed, high throughput, small silicon area and at the same time, low power consumption. This is why building low-power, high-performance adder cells is of great interest.

With technology scaling, dynamic power is continuously being reduced, while static leakage power tends to increase and is expected to become a large contributor to total power in a few technology generations. Leakage power is becoming a real issue and requires suitable power management, particularly as systems spend most of their time in silent mode. Leakage power is thus a critical parameter for portable electronic devices [1].

In many computers and other kinds of
processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, etc. Circuit performance is strongly influenced by the choice of logic style to design digital circuits.

Propagation delay time is one of the major factors affecting full adder performance. It is determined by not only number of transistors, but also its size and parasitic capacitance including intrinsic capacitance and capacitance due to routing. While dynamic power consumption depends on the switching activity and the number and size of transistors (i.e., their contribution to parasitic capacitances). Among all previously mentioned factors, the die area depends on the number and size of transistors and routing complexity [3].

There are many easy way to improve multi-bit adder performance by efficiently implementing the carry propagation chain. This can be addressed by either improving the structure of the 1-bit full adder which is one of the basic cells in adders such as the carry select or carry skip, as well as the building block of the ripple carry adder (RCA) since an n-bit RCA is formed by 1-bit fulladders, or by using improved fast adder architectures such as conditional SUM adders (CSAs) or carry look-ahead (CLA) adders.

Many full adders have been investigated by the academic and industrial research communities. The usual performance evaluations are speed, power consumption, and silicon area. However, since mobile and embedded applications have prioritized the power consumption to stand at the top of circuit and system performance evaluations, the goal of many of these full-adder variants has traditionally been the reduction of transistor count. However, it was investigated before that although some of these full adders feature good behavior when implementing a 1-bit cell, they may show performance degradation when used to implement more complex structures.

The rest of the paper is organized as follows. Section 2 explores a review of the full adder design in different logic styles, analyzing the concept of design and its advantages and disadvantages, while section 3 presents proposed hybrid full adder cell design based on pass logic and complementary CMOS logics. Simulation results comparing our proposed cell with previous selected cells in low power regime are presented in section 4. Finally, conclusions are stated in section 5.

2. Review of Full Adder Cells

There are different implementations with various logic styles that have been used in the past to design full-adder cells. Although they all have similar function, the way of producing the loads on the inputs and intermediate nodes and the transistor count are varied. Different logic styles tend to favor one performance aspect at the expense of the others. Some of them use one logic style for the whole full adder and others use more than one logic style for their implementation which we call them hybrid logic design style.

The complementary CMOS full adder (C-CMOS) [4] as shown in (Fig. 1a) is based on a regular CMOS structure with conventional pull-up and pull-down transistors and has 28 transistors. C-CMOS generates Cout throughout a single static CMOS gate. The main disadvantage of C-CMOS full adder is that the input capacitance of a static CMOS gate is large because each input is connected to the gate of at least one PMOS and one NMOS device. So that additional buffers at the last stage are needed to provide the required driving power because the series transistors in the output stage form a weak driver. The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing.

On the other hand, the hybrid full adder by
Chang et al. [5] shown in (Fig. 1b) has been implemented using 26 transistors. It utilizes a modified low-power pass logic XOR/XNOR circuit that cogenerates the intermediate XOR and XNOR outputs which has been improved to get the full swing logic, balanced output and good output drivability. This full-adder cell can work at low supply voltage. In this design, worst case delay problems due logic transitions are also solved by adding more transistors; however, these additional transistors increase the power consumption of the full adder cell.

Another full adder by Aguirre et al. [6], shown in (Fig. 1c) is the complementary pass-transistor logic (CPL) with level restoration to obtain balanced paths which are based on the multiplexing of the Boolean functions XOR/XNOR and AND-OR, to obtain the SUM and carry outputs respectively. CPL produces many intermediate nodes and their complement to make the outputs. Similar adder by Geol et al. [7] is shown in (Fig. 1d) which also uses a XOR/XNOR circuit that produces balanced full-swing outputs. It has high-speed operation due to the cross-coupled pMOS pull up transistors providing the intermediate signals quickly and a hybrid- MOS output stage with a static inverter at the output. However, full adder was suggested by Agarwal et al. [8] (Fig. 1e) uses the CPL logic which composed by NMOS transistors with pull-up PMOS transistors to obtain full swing output voltage. Due to positive feedback and use of NMOS transistors, the circuit is inherently fast and has a balanced structure for the generation of SUM and carry signals. This helps in simultaneous arrival of signals in tree structured circuits.

The basic difference between the pass-transistor logic style and the complementary CMOS logic style is that the source side of the pass logic transistor network is connected to some input signals instead of the power lines. One pass-transistor network is enough to implement the logic function; therefore results are generated by a smaller number of transistors and a smaller input load. Pass-transistor logic has intrinsic problems of threshold voltage drop, and drivability of output inverters. CPL is not an appropriate choice for low power due to its high switching activity of intermediate nodes, high transistor count, static inverter and overloading of its inputs.

Fig. 1f shows full-adder design [5, 9] which contains transmission function full adder. This design is based on transmission function theory and transmission gates and has 16 transistors. Transmission gate consists of a PMOS transistor and an NMOS transistor that are connected in parallel which is a particular type of pass-transistor logic circuit. There is no voltage drop problem but it requires double the number of transistors to design a similar function. Transmission logics are inherently low power consuming and they are good for designing XOR or XNOR gates. The main disadvantage of these logic styles is their lack driving capability. Also, if they are cascaded, their performance degrades significantly.

10T [10] in (Fig. 1g) uses more than one logic style for their implementation and they are called Hybrid logic design style. They generate A XOR B and use it and its complement as a select signal to generate the outputs. They benefit from small transistor count and exploit the non full swing pass transistors with swing restored transmission gate techniques. The problem that produces high capacitance values for the inputs is less clear in these designs. This full adder has lower loading of the inputs and intermediate nodes, lower-transistor count and balanced generation of SUM and Cout signals. These full adders lack driving capabilities in fan-out situation and their performance degrades drastically when they are cascaded.

3. Proposed low power full adder

This architecture consists of two separate
Fig. 1. Full Adder Cells of different logic styles. For all NMOS transistors, W/L = 0.25μm/0.13μm and for all PMOS transistors, W/L = 0.5μm/0.13μm.
parts. The first one is to generate sum using pass transistor XOR/XNOR logic which is used in this architecture for its minimum area and minimum number of transistors. However the problem of pass logic is that it provides weak logic 1 or 0 or both. So it is so important to use level restorer to retain voltage to its normal value. The simplest and more efficient way to keep the logic level to its normal state is to put an inverter in the output, but in this case, a complement of sum will be generated. This problem can be avoided by adding another inverter or it's better to change the second XOR to XNOR. Low power XOR and XNOR gates (Fig. 2) are presented and discussed to understand the challenges we face in full adder design.

![Fig 2. XOR and XNOR using transistor pass logic](image)

They were proposed previously by[11]. From the low power XOR gate analysis, it can be seen that the output signal has a good logic level for input signal \((A,B)=(0,1),(0,1),(1,1)\). For the \((A,B)=(0,1)\) configuration, each pMOS is switched on and passes a weak logic "0" (i.e., \(V_{IP}\)). Reciprocally, The XNOR gate shows good logic levels for input signal \((A,B)=(0,0), (1,0),(0,1)\). For the \((A,B)=(1,1)\) configuration, each nMOS is switched on and passes a weak logic "1" as shown in (Fig. 3). In order to enhance the driving capability at the output nodes, CMOS inverter is used at the output. Simply, restorer can be implemented by pull up pMOS to solve weak 1 logic, pull down nMOS to solve weak 0 logic, or an inverter to work as a buffer. Also, different kinds of restorers were used depending on the circuit design.

![Fig 3. Simulation results for transistor pass XOR](image)

The low power XOR gate has the lowest leakage power in comparison with XOR gates based on other well-known topologies [11]. By using the low power XOR/XNOR gates, the SUM block does not need true input signals and their complements at the same time. Thus, in the case of the RCA implementation, the SUM block does not need the complementary carry-in signal since we implement it with low power XOR and XNOR gates, as opposed to the SUM block. This avoids the need of inverters on the carry chain in multiple-bit adders. The output inverter in the carry block can then be removed. For sum generation, we use previous XOR and XNOR with a restorer to solve the problem of weak 1 or weak 0. Fig. 4 shows circuit design for sum generation and Fig. 5 shows the results of using this circuit. It can be observed that the restorer has a great effect on the output level and delay.
Fig 4. Proposed full Adder sum generation

Fig 5. Simulation result for proposed full Adder sum generation

However, for carry generation (Fig. 6), we use complementary CMOS logic to give high reliability and performance.

We can observe that the output is the complementary of Cout, so we are in need of inverter to get Cout. Fortunately, we can make use of the complementary of Cout without complement in multi-bit design. We can modify the sum generation of the next stage to take the inputs as (A, B, Complement of Cin) by using a combination between XOR and XNOR in designing sum generation circuit. Also, next full adder carry generation circuit can have the same inputs to give Cout. So that for multi-bit adder, sum generation circuit uses 10 transistors (either it consists of XOR/XNOR combination or XOR/XOR combination), while carry generation circuit uses 12 transistors (either the inputs are A, B, Cin or A, B, Cin to produce Cout or Cout, respectively) without need for inverter. As a result total number of transistors will be 22.

Fig 6. Proposed full adder carry generation circuit for inputs a) A, B, and Cin b) A, B, and Cin.

4. Discussion

In previous sections, we analyzed and compared most known full adder designs in low power regime. We simulated most of these full adders to give a complete overview and exclude the advantages and disadvantages for each of them. These circuits have been built using Samsung Electronics L13G33 MOSFET process and simulated at room temperature (25° C). We can observe that C-CMOS full adder has an advantage of low static power consumption while it consumes more dynamic power. So that it is not recommended in fast circuits. Similar, Goel et al. full adder design consumes little static power but it has less propagation delay and less number of
transistor. However, Chang et al. full adder has low propagation delay and static power consumption but it still uses 26 transistors. On the hand, our proposed full adder provides many advantages. It has less number of transistors and it does not require additional inverters in multi-bit adder design. Also, it consumes less static and dynamic power and operates faster than comparable adders.

Table1. Comparison between different full adders simulated on 0.13μm process and 100MHz

<table>
<thead>
<tr>
<th>Design</th>
<th>Delay (ns)</th>
<th>Total power (μW)</th>
<th>PDP (Joule)</th>
<th>Static power (nW)</th>
<th>Device count</th>
</tr>
</thead>
<tbody>
<tr>
<td>C-CMOS</td>
<td>0.2</td>
<td>15.636</td>
<td>3.127</td>
<td>0.82</td>
<td>28</td>
</tr>
<tr>
<td>Chang</td>
<td>0.08</td>
<td>5.22</td>
<td>0.417</td>
<td>1.896</td>
<td>26</td>
</tr>
<tr>
<td>Goel</td>
<td>0.12</td>
<td>11.268</td>
<td>1.352</td>
<td>2.64</td>
<td>24</td>
</tr>
<tr>
<td>Ahawal</td>
<td>0.09</td>
<td>17.4</td>
<td>1.566</td>
<td>3.432</td>
<td>26</td>
</tr>
<tr>
<td>Aguirre</td>
<td>0.2</td>
<td>9.52</td>
<td>1.904</td>
<td>3.025</td>
<td>24</td>
</tr>
<tr>
<td>proposed</td>
<td>0.07</td>
<td>3.57</td>
<td>0.249</td>
<td>1.34</td>
<td>22</td>
</tr>
</tbody>
</table>

Fig 7. Comparison between different full adders as percentages of related CMOS values

5. Conclusions

In this paper, different interesting full adders are analyzed and compared with our proposed hybrid low power/high speed full adder which has the advantage for lowest propagation delay, and power delay product. It also consumes the smallest amount of static and dynamic power compared with other full adders.

Acknowledgements

This work was supported by the research grant of the Chunguk National University in 2009

REFERENCES


