Work In Progress - Area Level Assessment Process

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Abstract— **Outcomes assessment is now an integral part of the ABET accreditation criteria. The process to implement an automated on-line area level assessment test that helps meet ABET requirements is discussed. Selection of appropriate technology, on-line test questions generation and administering the test, initial implementation results and future work are discussed.**

I. Introduction

The Electrical and Electronics Engineering Department at California State University Sacramento has recently completed a successful EAC of ABET accreditation visit in Fall 2003. To better prepare for the next accreditation visit in 2009, the Department has formed an Assessment committee to quantify Program Outcomes at the area level. The required courses in the EEE department have been categorized according to areas. Six areas have been identified: Circuits, Electronics, Communications, Control, Digital and Microprocessors. The committee is currently developing a pilot process to automate the on-line assessment of program outcomes beginning with the Circuits area. The fully automated online test will be distributed to students at the senior and junior level. Grades, by themselves, are insufficient as direct measures of specific outcomes, therefore this area level assessment test tests students on the topics that were not specifically taught during the class that the test is distributed. In addition the student's grade in the course that the exam was distributed in is not a factor in the evaluation of the learning outcomes. The use of this online test tool is geared to specific program outcomes as opposed to specific course learning outcomes. This paper addresses the initial survey of technologies that was considered, the technology that was chosen, the process for successful design, implementation and test of an online testing tool at the area level, some practical challenges and limitations as well as data from the on-line automated test that was performed during the Spring semester of 2005.

II. Initial Survey of Technologies

The Electrical and Electronic Engineering department has started this endeavor by envisioning a simple, secure, free, user-friendly, custom and maintenance free assessment area level test tool. The quiz questions were initially envisioned as a fill-in-the-blank or multiple choice type with randomized input variables and a set of equations that define the correct and incorrect output variables. It was with great disappointment that we realized that such a test tool is not currently available to our knowledge. Subsequently we decided to establish a custom quiz utility by connecting MySQL database to an HTML secure web site through PHP web-scripting language. In addition the multiple equations within the test questions as well as the graphics would be written as java applets. The development of such a tool would require a significant investment of time as well as considerable resources to maintain the database once the tests are administered. Subsequently, a survey of current Learning Management Systems and learning environments was undertaken. Many of the current LMS are reviewed on the edutools webpage: http://www.edutools.info. Currently, WebCT and Blackboard are the two major commercial competitors that supply a learning management system (LMS) technology. In addition there is a trend to use open-source environments for LMS, such as Moodle or Spaghetti. Due to the limited time that was available, security issues, connectivity with university's e-mail databases, maintenance at the university level, some previously implemented statistical processing capability and finally cost at the department level (free) WebCT was chosen as the technology of choice. The disadvantage of using WebCT is that it has a severely limited test tool. Once the technology was chosen, the assessment process was developed, as shown in Figure 1. Generation of an online assessment test consists of three parallel processes: select appropriate technology, select generate area level questions and administer the test.

III. Process to generate area level questions

To implement the process the entire faculty in the department have agreed on the following statements: The test must meet ABET criteria, the required effort needs to be manageable for both faculty and students, the implementation must meet department budget constraints, the assessment must be area based, not course based and the assessment needs to be applied uniformly across the given area. The required courses in the EEE department have been categorized according to disciplines. Six areas have been identified: Circuits, Electronics, Communications, Control, Digital and Microprocessors. The pilot assessment test for the Circuits and Electronics area was selected first. Next the desired test question attributes were selected, namely the questions need to be conceptual, solvable in less than 5 minutes, multiple choice or fill-in-the-blanks type and enable automated grading. Finally sample questions were generated with the involvement of the faculty teaching the identified classes in that area.

IV. Process to Administer the test

The first step in the process is to select how many tests should be administered and when. To monitor longitudinal process, enough time should be allowed between two tests to allow for the student's academic growth and acquisition of advanced concepts. It was decided to test the students once at the junior level and once at the senior level. The classes selected to administer the tests are EEE108 Electronics I and EEE193B Electronic Product Design (Senior Project). Electronics I is

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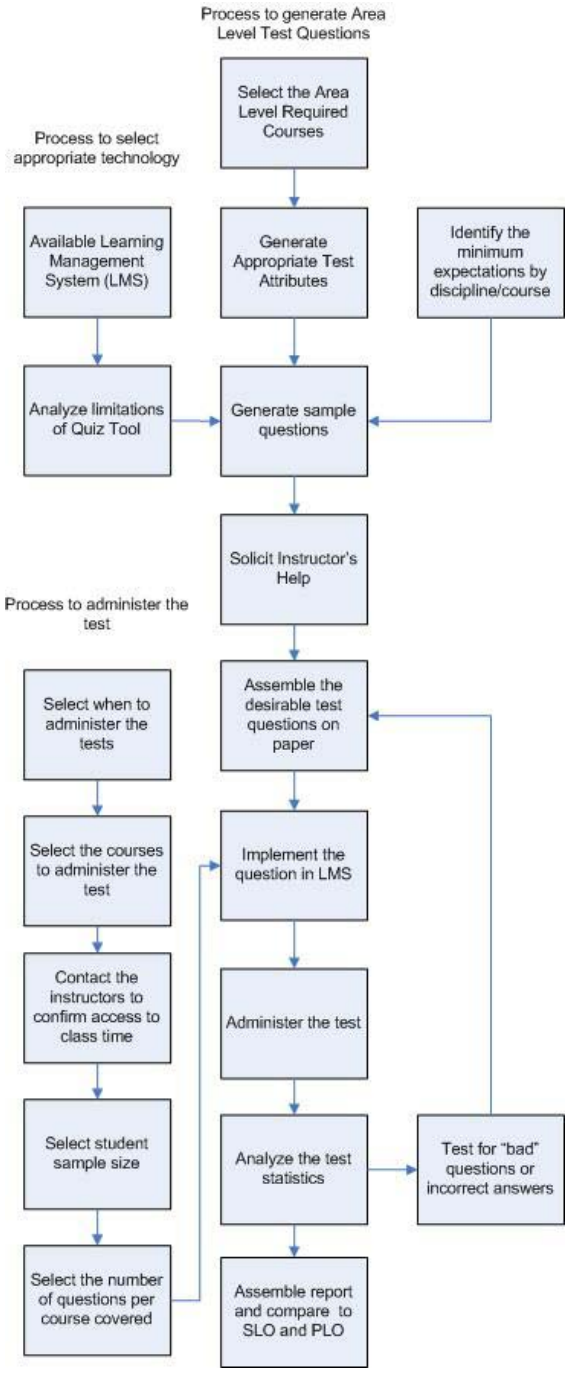

Fig. 1. Area level assessment process

the last course that the students take before they select the area of study. The first area level assessment test is distributed during the Electronics I course in the duration of 75 minutes. The course encompasses topics from the following required classes: ENGR17 Introduction to Circuit Analysis, EEE117 Network Analysis and EEE108 Electronics I. The second area level test during the senior year will encompass topics from an additional course EEE109 Electronics II. When the test is finalized for all areas, the students enrolled in EEE193B Electronic Product Design class will take a single area level assessment test that encompasses topics from all three areas of study: Communications, Controls and Circuit and Electronics. Each area will contribute questions that can be solved in 25 minutes, so that the total duration of the test is 75 minutes. The students will be offered extra credit within the two individual classes to take the test. The course grades will not be used in evaluating the success of the assessment outcomes; only the test results will be compiled over time. In addition we intend to close the loop with Program Learning Outcomes as the second test is administered during the final weeks of the students residence at Sacramento State.

V. Conclusions and Future Work

Analysis of successfully solved problems within the area of study, within specific courses, for each question, each concept and each student are envisioned. Currently, only the first area level assessment test has been administred. The results are available for the area level, specific course and each question in the test, as these statistics are readily available in WebCT. For example an average score for all test questions from Introduction to Circuit Analysis is 56%, Network Analysis is 35% and Electronics I is 34%. The overall area level mean is 45%. It should be noted here that the debugging of the questions is not yet finalized and that could have been a potential reason for the scores being lower than expected. Due to current calculations of the mean value the same weight is assigned to the mean value of one student answering the question incorrectly and several students answering a question incorrectly. The sample is not yet statistically significant.

Ideally, the questions integrate one to four concepts learned in different classes. Within each question the concepts necessary to answer the question are identified. The weight of concepts within a question will be distributed and the statistics on concepts will be examined. In addition we plan on studying whether the questions were good. If the same concept is consistently identified in one question and not in another, it may suggest that the question is not adequately conceived. These issues will be used to close the loop with instructors and corresponding Student Learning Outcomes in a particular course. The real success of this endeavor is in perpetual question modification to pinpoint specific concepts of interest or potential problems. In addition the database assembly of potential common misconceptions is envisioned. Finally by closing the loop between the Area level assessment process and Student and Program Learning Outcomes we strive to make improvements to our program and the scholarship of Assessment in Electrical Engineering.