Conduction mechanisms of silicon oxide/titanium oxide MOS stack structures

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Abstract

During the last years, high-\(k\) dielectrics have been studied intensively looking for an alternative material to replace the SiO\(_2\) films as gate dielectric in MOS transistors. Different materials and structures have been proposed. An important concern not yet solved, is the interfacial quality between high-\(k\) materials and silicon substrate. For this reason, stack structures with SiO\(_2\) as an interfacial layer between silicon substrate and high-\(k\) film have been studied. In this contribution we analyze the main conduction mechanism observed in SiO\(_2\)/TiO\(_2\) MOS stack structures obtained by room temperature plasma oxidation in different conditions and reactors. Films fabricated in a parallel-plate type reactor showed better quality with low current density where thermionic conduction mechanism is predominant. In lower quality films, for example those fabricated in a barrel type equipment, the current density is higher and the conduction mechanism observed is Poole–Frenkel. Finally we show that the presence of thermionic mechanism provides a weak thickness dependence and a strong current density reduction with respect to silicon oxide MOS structures with the same equivalent oxide thickness.

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1. Introduction

During the last decades, the dimensions of MOS transistors (MOST) have been continuously scaled down. This reduction has produced the necessity of ultrathin gate dielectric films, with thickness less than 1.2 nm for the sub-100 nm technology node for high performance MOST [1].

It is well known that as the SiO\(_2\) film thickness is reduced below 2 nm, several problems appear that limit its use as gate dielectric in MOST [1–3]. In order to continue with the device scaling, it is necessary to look for alternative gate dielectrics and structures.

Several high-\(k\) dielectric materials have been studied as possible candidates for this purpose, although several concerns have not yet been solved. Among them, low interfacial quality and stability [4,5], as well as the small conduction band offset at silicon/dielectric interface [2,3] as \(k\) increases, are the main problems that make difficult their application.

To avoid these problems, stack structures formed by a SiO\(_2\) interfacial layer and a high-\(k\) dielectric over it have been proposed as possible candidates with the advantage of a better interface with silicon and a physically thicker overall layer [6–9]. In this case the equivalent oxide thickness (\(T_{eq}\)) can be expressed as

\[
T_{eq} = T_{SiO_2} + \frac{k_{SiO_2}}{k_{H-k}} \cdot T_{H-k}
\]  

where \(T_{SiO_2}\) and \(k_{SiO_2}\) are the thickness and the dielectric constant of the underlying or interfacial SiO\(_2\) layer in contact with the silicon substrate. \(T_{H-k}\) and \(k_{H-k}\) are the thickness and the dielectric constant of the high-\(k\) material.

According to (1), if a medium dielectric constant material is used in the stack, for example HfO\(_2\) or ZrO\(_2\), it will be necessary a very thin high-\(k\) layer in order to obtain an \(T_{eq}\) below 1.5 nm. In this case, the physical thickness would not be enough to maintain the benefits of high-\(k\) dielectrics.
On the other hand, if a higher dielectric constant film is used, the $T_{eq}$ can be reduced even below 1.5 nm, with the benefits of both a good quality SiO$_2$ interfacial film and high-$k$ material. A material such as TiO$_2$, with a dielectric constant between 40 and 100, could be used for this purpose. Its low band offset with Si may not be a problem due to the presence of the interfacial SiO$_2$. To verify this assumption, it is necessary to study the conduction mechanisms and barrier present in these structures, in order to determine their advantages and possibilities, as well as, to improve and control their properties.

Previously we reported stack structures formed by a TiO$_2$ layer on top of a SiO$_2$ layer obtained using room temperature plasma oxidation (RTPO) technique [10,11]. In this contribution we complement the characterization of stack structures prepared under different conditions and using different reactor types, in order to determine their characteristics and the main conduction mechanism in each case. The expected general behavior and advantages are summarized indicating possible fields of application.

### Table 1

<table>
<thead>
<tr>
<th>Sample</th>
<th>SiO$_2$ films</th>
<th>TiO$_2$ films</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reactor type</td>
<td>Gas</td>
<td>Thickness (nm)</td>
</tr>
<tr>
<td>TiOA</td>
<td>Barrel</td>
<td>O$_2$</td>
</tr>
<tr>
<td>TiOB</td>
<td>Barrel</td>
<td>O$_2$</td>
</tr>
<tr>
<td>TiOC</td>
<td>Barrel</td>
<td>O$_2$</td>
</tr>
<tr>
<td>TiOD</td>
<td>Barrel</td>
<td>O$_2$</td>
</tr>
<tr>
<td>TiOE</td>
<td>P-P</td>
<td>N$_2$O</td>
</tr>
<tr>
<td>TiOF</td>
<td>P-P</td>
<td>N$_2$O</td>
</tr>
<tr>
<td>TiOG</td>
<td>P-P</td>
<td>N$_2$O</td>
</tr>
<tr>
<td>TiOH</td>
<td>P-P</td>
<td>N$_2$O</td>
</tr>
<tr>
<td>TiOI</td>
<td>P-P</td>
<td>N$_2$O</td>
</tr>
<tr>
<td>TiOJ</td>
<td>P-P</td>
<td>N$_2$O</td>
</tr>
<tr>
<td>TiOK</td>
<td>P-P</td>
<td>N$_2$O</td>
</tr>
</tbody>
</table>

### 2. Experiment

The stack structures were prepared on 0.1 Ω cm n-type, (100) oriented silicon substrate, using RTPO technique as was described previously in [10,11]. Different structures were made varying the SiO$_2$ and TiO$_2$ film thickness. The SiO$_2$ interfacial films were obtained by RTPO using O$_2$ or N$_2$O as oxidant gases; the TiO$_2$ films were obtained by RTPO using O$_2$, parallel-plate (P-P) and barrel reactors were used to compare the behavior of films with different
qualities. The thicknesses of both films were determined through ellipsometry and C–V characterizations as was described previously [10,11]. MOS structures were prepared using chromium as gate electrode. Table 1 summarizes the samples with different thickness prepared in different reactor types and oxidation gases.

3. Conduction mechanism

Fig. 1 shows the band diagram in strong accumulation of a stack structure. An appropriate determination of the conduction mechanisms in MOS structures requires knowledge of the electric field in each dielectric film. If we consider that a positive voltage is applied at the gate, it will produce a band bending across each film as shown in Fig. 1. The gate voltage is expressed as

$$V_G = V_{SiO_2} + V_{H-k} + \phi_S + V_{FB}$$

where $V_{SiO_2}$ is the voltage across the silicon oxide film, $V_{H-k}$ the voltage across the high-$k$ film, $\phi_S$ is the silicon surface potential and $V_{FB}$ is the flat-band voltage of the MOS structure. The overall voltage that falls across the dielectric films ($V_I$) is related to the total semiconductor charge ($Q_S$) as

![Graph](graph.png)

Fig. 3. (a) and (b) $J–V$ curves for stack structures where SiO$_2$ film was fabricated in barrel reactor.


\[ V_1 = V_{\text{SiO}_2} + V_{\text{H}-k} = -\frac{Q_S}{C} \]  

(3)

where \( C \) is the dielectric capacitance.

Considering that the stack structure is formed by two series capacitances, the \( C \) capacitance will be obtained as

\[ C = \frac{C_{\text{SiO}_2} \cdot C_{\text{H}-k}}{C_{\text{SiO}_2} + C_{\text{H}-k}} \]  

(4)

where \( C_{\text{SiO}_2} = k_{\text{SiO}_2} \cdot \varepsilon_0 / T_{\text{SiO}_2} \); \( C_{\text{H}-k} = k_{\text{H}-k} \cdot \varepsilon_0 / T_{\text{H}-k} \) and \( k_{\text{SiO}_2} \) and \( k_{\text{H}-k} \) are the dielectric constant for \( \text{SiO}_2 \) and high-\( k \) material, respectively.

The voltage drop across each layer is:

\[ V_{\text{SiO}_2} = -\frac{Q_S}{C_{\text{SiO}_2}} \]  

(5)

\[ V_{\text{H}-k} = -\frac{Q_S}{C_{\text{H}-k}} \]  

(6)

Thus the voltage across each dielectric film is proportional to the thickness–dielectric constant ratio \((T/k)\). In typical MOS stack structures with ultrathin equivalent thickness, the \( \text{SiO}_2 \) \( T/k \) ratio is greater than the high-\( k \) dielectric \( T/k \) ratio, so the voltage across the silicon oxide

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Fig. 4. (a) and (b) \( J-V \) curves for stack structures where \( \text{SiO}_2 \) film was fabricated in parallel-plate reactor.
will be greater than that across the high-$k$ material. The electric field is obtained once the voltage has been determined.

In an accumulated stack structure different conduction mechanisms can contribute to the current density, which are direct or FN tunneling ($J_{DT}$, $J_{FN}$), thermionic emission ($J_{TE}$) and Poole–Frenkel ($J_{PF}$). However, direct tunneling is expected to dominate as the overall thickness is reduced below 5 nm. In the typical stack structure the physical thickness is expected to be greater enough to avoid it; therefore direct tunneling is not considered. Any of the other two mechanisms $J_{TE}$ and $J_{PF}$ may be present and with the increase of the electric field, FN tunneling may appear.

The current density behavior of each mechanism can be expressed as

$$J_{DT} = \frac{A \cdot E_d^2 \exp \left[ \frac{B \phi_b^{3/2} - (\phi_b - q \cdot V_d)^{3/2}}{\phi_b^{3/2}} \right]}{1 - (\phi_b - q \cdot V_d)^{3/2}} \cdot \exp \left[ \frac{B \phi_b^{1/2} - (\phi_b - q \cdot V_d)^{1/2}}{\phi_b^{1/2}} \cdot E_{TFS} \right]$$

$$J_{FN} = A \cdot E_d^2 \exp \left[ -\frac{B}{E_d} \right]$$

(7)  

(8)

Fig. 5. Semilogarithmic curves for samples prepared by plasma oxidation in barrel reactor, showing (a) $J/E_{TiO_2}$ vs. $E_{TiO_2}^{1/2}$ and (b) $J$ vs. $E_{TiO_2}^{1/2}$.  

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\[ J_{PF} = E_d \cdot \exp \left[ -\frac{q}{kT} \left( \phi_b - \sqrt{\frac{qE_d}{n_0 k_d}} \right) \right] \] (9)

\[ J_{TE} = A' T^2 \cdot \exp \left[ -\frac{q}{kT} \left( \phi_b - \sqrt{\frac{qE_d}{4n_0 k_d}} \right) \right] \] (10)

where: \( A = \frac{q^2 m_0}{8 \pi n_0 \epsilon_0 \phi_b} \); \( B = \frac{4 \sqrt{2 \pi n_0 \epsilon_0 \phi_b}}{3q} \); \( A' = 120 \) [A m\(^{-2}\) K\(^{-2}\)].

\( m_0 \) is the free electron mass, \( m_{te} \) is the effective mass in the dielectric film, \( \phi_b \) is the barrier height, \( V_d, E_d \) and \( k_d \) are the voltage drop, the electric field and the dynamic dielectric constant of the dielectric film, respectively.

4. Experimental results

Fig. 2 shows a comparison between the voltage drop across the whole stack and across the each of the dielectric layers for a SiO2/TiO2 stack structure with 1.5/8.5 nm thickness, respectively, calculated according with Eqs. (3), (5) and (6).

Fig. 3a and b show typical J–V curves for two different samples fabricated in the barrel reactor, where some dispersion on the measured current can be observed. Fig. 4a and b show typical J–V curves for two different samples where SiO2 interfacial film was fabricated in the parallel-plate reactor. As can be seen the dispersion of the measured current for these structures is lower than that for those in Fig. 3, probably because the SiO2 films and SiO2–Si interface obtained in the parallel-plate reactor have better quality than those obtained in the barrel reactor [11].

The presence of PF or TE can be determined using a semilogarithmic plot of \( J/E_{TiO_2} \) vs. \( E_{TiO_2} \) for samples TiOA, TiOB, TiOC and TiOD in Table 1, where \( E_{TiO_2} \) is the electric field in this dielectric. As can be seen from these figures, both conduction mechanisms seem to be possible from to the presence of a straight-line region in both graphic representations. According to Eqs. (9) and (10), the dynamic dielectric constant \( k_d \) can be obtained from the slope of the plots. However, the slope of the curves shown in Fig. 5b gives values for \( k_d \) lower than 1, which is impossible, indicating that TE is not the mechanism that is taking place. On the contrary, if we consider that PF mechanism is present, the value of \( k_d \) obtained is around 5 for samples TiOA and TiOB and around 9.7 for samples TiOC and TiOD which are expected values for the thickness ratio of the analyzed stacks. Hence the main conduction mechanism observed in these samples, where both dielectric layers were prepared in the barrel equipment is PF. This mechanism has also been observed by Chen and collaborators in MOS structures prepared with sputtered TiO2 film as gate dielectric [12].

Fig. 6 shows the semilogarithmic plots of \( J/E_{TiO_2} \) vs. \( E_{TiO_2}^{1/2} \) for the samples TiOE to TiOK where the SiO2 layer was prepared by plasma oxidation in the P-P equipment, see Table 1. As can be seen a straight-line region is not observed in the plots indicating that no PF is present for any of these samples.

Fig. 7a–c show the semilogarithmic plots of \( J \) vs. \( E_{TiO_2}^{1/2} \) for the samples shown in Fig. 6. As can be observed, in all cases there is a straight-line region, which implies the presence of TE as conduction mechanism.

The behavior of J–V with temperature for TiOK sample is presented in Fig. 8 in the form of a semilogarithmic plot of \( J/T^2 \) vs. \( E_{TiO_2}^{1/2} \). As can be seen from this figure, a
straight-line region is observed at all temperatures measured. Additionally, Fig. 9 shows the semilogarithmic plot of $J/T^2$ vs. $1/T$, where also a straight-line region is observed. Both figures confirm the presence of TE as main conduction mechanism. A more detailed analysis of the behavior with temperature of these structures can be found in [13]. This mechanism has also been observed for thick deposited films, [14,15].

Table 2 summarizes the values of dielectric constant and barrier height obtained from curves 5a, 7a-c for the different stack structures under analysis.

5. Discussion

As indicated in Table 1, both dielectric films, for samples TiOA to TiOD were processed in a barrel reactor type. The barrel reactor does not reach high vacuum. This feature allows the presence of high density of impurities in the reactor chamber and thus low films quality. For this reason the stack structure obtained seems to have higher trap density and PF become the main conduction mechanism. The barrier height $\phi_b$ was always smaller than 0.7 eV. The dynamic dielectric constant of TiO$_2$ has been reported
around 7.8 [16], although its value for the stack structure is lower, depending on the thickness ratio of the layers. For these samples, $k_d$ varied from one process to another in a wide range, see Table 2, this fact can be related with the low film quality and repeatability.

For the rest of the samples, the SiO$_2$ film was grown in a parallel-plate reactor, leading the improvement of the film quality due to the high vacuum possibility in this reactor. The better quality of the SiO$_2$ layer and of the SiO$_2$–Si interface produces that TE became the main conduction mechanism.

Another interesting result is that for samples where the TiO$_2$ layer was still processed in the barrel reactor (samples TiOE to TiOI in Table 2), the barrier height was lower than 0.6 eV. When both dielectric films were processed in the parallel-plate reactor it was possible to obtain barrier heights higher than 0.7 eV and even close to 0.8 eV, confirming that films processed in P-P reactor presented higher
quality with better electrical behavior. In this case, the variation of the dynamic dielectric constant for different samples was much smaller. Additionally the refractive index experimentally obtained varies from 1.8 to 2.7. These values correspond to dynamic dielectric constants of 3.24–7.3, which agree with the values observed in Table 2.

Using Fig. 8, it is possible to obtain the \( k_d \) value from the current measured at different temperatures. The values obtained varied from 3.5 to 4.2, which agree with the value obtained from the room temperature measurement.

Fig. 9 again confirms that the conduction mechanism present in these samples is thermionic emission. The slope of this curve is related to the values of \( k_d \) and \( \phi_b \), thus the barrier height can be obtained if the dynamic dielectric constant is known.

Considering the mean value of \( k_d \), obtained from the curves in Fig. 8 (which was 3.85), the value of 0.78 eV is obtained for \( \phi_b \), which also agrees very well with the value obtained from the room temperature measurement.

Table 2: Dynamic dielectric constant and barrier heights obtained for the different samples

<table>
<thead>
<tr>
<th>Sample</th>
<th>Conduction mechanism</th>
<th>( k_d )</th>
<th>( \phi_b )</th>
</tr>
</thead>
<tbody>
<tr>
<td>TiOA</td>
<td>PF</td>
<td>5.3</td>
<td>0.63</td>
</tr>
<tr>
<td>TiOB</td>
<td>PF</td>
<td>5.0</td>
<td>0.59</td>
</tr>
<tr>
<td>TiOC</td>
<td>PF</td>
<td>9.7</td>
<td>0.47</td>
</tr>
<tr>
<td>TiOD</td>
<td>PF</td>
<td>9.7</td>
<td>0.44</td>
</tr>
<tr>
<td>TiOE</td>
<td>TE</td>
<td>5.7</td>
<td>0.57</td>
</tr>
<tr>
<td>TiOF</td>
<td>TE</td>
<td>5.2</td>
<td>0.49</td>
</tr>
<tr>
<td>TiOG</td>
<td>TE</td>
<td>4.9</td>
<td>0.56</td>
</tr>
<tr>
<td>TiOH</td>
<td>TE</td>
<td>5.5</td>
<td>0.6</td>
</tr>
<tr>
<td>TiOI</td>
<td>TE</td>
<td>6.5</td>
<td>0.6</td>
</tr>
<tr>
<td>TiOJ</td>
<td>TE</td>
<td>4.5</td>
<td>0.71</td>
</tr>
<tr>
<td>TiOK</td>
<td>TE</td>
<td>3.5</td>
<td>0.81</td>
</tr>
</tbody>
</table>

An additional verification of these results was done using ATLAS simulator from Silvaco, which allows self-consistent calculation of DT gate current. Simulations confirmed that for a stack structure with 1.5/8.5 nm of SiO\(_2\)/TiO\(_2\) thickness ratio no direct tunneling is observed. On the other hand, if the simulation considers thermionic emission as mechanism for a barrier height in the range of 0.5–1 eV for the TiO\(_2\) material, the current densities produced are similar to the experimental currents measured.

An interesting result observed when TE is the main conduction mechanism is shown in Figs. 10–12. In Fig. 10 the calculated current density for stack structures with 0.8 nm of SiO\(_2\) thickness and several TiO\(_2\) thickness, varying from 5 to 11 nm is shown. In Fig. 11 the current density for stack structures with 5 nm TiO\(_2\) thickness and SiO\(_2\) thickness varying from 0.8 to 2 nm is shown. In both figures, the \( T_{eq} \) considering the previously experimentally obtained value of \( k_{T,eq} = 50 \), is included [11]. The current densities were calculated considering \( k_d = 6.0 \) and \( \phi_b = 0.8 \) eV, which were obtained for best process. In both cases the variation of the current density with \( T_{eq} \) is relatively small.

In Fig. 12 the predicted dependence of \( J \) vs. \( T_{eq} \) for a stack and for a single SiO\(_2\) layer are compared for a gate voltage of 2 V applied on the metal electrode. From this figure, it can be observed that the stack structure current density behaves quite different from the single film case, as the \( T_{eq} \) is reduced. As it was pointed out above, the conduction mechanism TE will be predominant until a given TiO\(_2\) film thickness. If the thickness is further reduced, the tunneling probability increases and for a given overall thickness the current through the stack will be dominated by the DT mechanism. According to Fig. 12, a stack structure with \( \phi_b = 0.8 \) eV and \( k_d = 6.0 \) will present TE as conduction mechanism even for \( T_{eq} \) as low as 1.17 nm, which...
corresponds to a TiO₂ thickness as low as 4.7 nm. If the TiO₂ thickness is reduced below this value the current becomes dominated by tunneling and a strong increase in it will be observed.

Fig. 12 also shows that the current density in stack structures with TE as main conduction mechanism, show a weak dependence with films thickness. For the stack structures, the current density will undergo only a small increase as the $T_{eq}$ is reduced from 2.4 to 1.15 nm, even for $T_{eq}$ as low as 1.15 nm the current density will be maintained almost in the same order of magnitude. On the other hand the DT mechanism in SiO₂ single layer structures shows the typical strong dependence with $T_{eq}$, increasing about 7 orders of magnitude as $T_{eq}$ decreases from 2.4 to 1.1 nm.

Unfortunately the $T_{eq}$ for a stack structure cannot be scaled down easily for thickness below 1.1 nm, since it is necessary to obtain SiO₂ interfacial films with thickness
in the order or less than 0.8 nm, or if the physical thickness of the high-κ dielectric film is reduced beyond the point where the tunneling probability will be increased. Some reduction can be still obtained if oxynitride or nitride films are used instead of SiO₂, but anyway there is a limit. Hence SiO₂/TiO₂ MOS stack structures appear to be an interesting approach to significantly reduce the leakage current in devices with Teq in the range from about 1.2 to 2 nm, where the DT current reaches prohibited values, as for example in low power applications. In these applications, a stack structure with equivalent thickness in the above mentioned range, which can reduce the current density by several orders of magnitude more that those observed even for oxynitrides, may represent an important advantage.

6. Conclusions

The main conduction mechanism observed in SiO₂/TiO₂ MOS stack structures fabricated by RTPO in parallel-plate and barrel reactors was analyzed. It was demonstrated that good quality films, where the main conduction mechanism is thermionic emission through a barrier higher than 0.7 eV, can be obtained when both dielectric films are processed in the P-P reactor for Teq down to 1.2 nm. Considering the values of the measured barrier heights and dynamic permittivity, the current density as function of the equivalent thickness of the stack was calculated, from which it is seen that the current density for an Teq in the range between 2 and 1.2 nm is reduced by several orders of magnitude with respect to the value expected when the main conduction mechanism is DT. For structures with smaller Teq, the physical thickness of the high-κ dielectric has to be reduced beyond a limit where the DT mechanism again becomes predominant with the consequence increase in current.

Therefore SiO₂/TiO stack structures, with equivalent oxide thickness in the range of 1.2 to 2 nm, combine the advantage of a good SiO₂–Si interface with a strong current reduction, with respect to the SiO₂ single layer, due to the presence of the thermionic mechanism with a barrier higher than 0.7 eV, resulting in an interesting approach for nanometric devices where low power consumption is an issue.

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References


