Evaluating the impact of scaling on temperature in FinFET-technology multicore processors

P. Zajac, M. Janicki, M. Szermer, A. Napieralski

Department of Microelectronics and Computer Science, Lodz University of Technology, Wolczanska 221/223, 90-924 Lodz, Poland

ARTICLE INFO

Article history:
Received 30 December 2013
Received in revised form
14 April 2014
Accepted 12 May 2014

Keywords:
Multi-core processors
Technology scaling
Thermal simulation
Activity migration

ABSTRACT

Every new technology node allows higher transistor density and more complex processors to be manufactured. Unfortunately, it also means that, for the same operating conditions, power density in the chip has to increase. However, it is not obvious how this increased power density translates into temperatures in the processor, therefore in this paper we analyze the influence of technology scaling on temperature of integrated circuit manufactured in FinFET technologies. The problem is discussed based on the results of both steady-state and transient thermal simulations obtained for two modern multi-core processors manufactured in 32 nm and 22 nm technologies.

© 2014 Elsevier Ltd. All rights reserved.

1. Introduction

The recent introduction of new transistor devices, referred to as FinFETs or Tri-Gate transistors, was mainly meant to alleviate the problem of constantly increasing leakage power in state-of-the-art integrated technologies. Unfortunately, it is very difficult to properly evaluate the impact of these recent advancements on the temperature of modern multi-core processors built with these devices. The reason is the lack of accurate block-level power models for these processors. Without such models, validated against measured data, it is impossible to obtain reliable power trace data for processor units which are absolutely indispensable for performing accurate thermal simulations for multi-core processors.

Nevertheless, in this paper the authors try to evaluate integrated circuit temperature using as benchmarks the Intel® Sandy Bridge and Ivy Bridge processors. The paper is structured as follows: Section 2 presents the organization of the floorplan in these processors and explains in detail the methodology adopted by the authors to determine the power trace data. In Section 3, results of the steady-state simulations using analytical solver based on Green's functions are presented. Section 4 describes transient thermal simulations of both processors obtained using a Hotspot thermal simulator. Conclusions and future work are presented in Section 5.

2. Power data estimation

2.1. Benchmark processors

To investigate the impact of scaling on temperatures in more detail, we analyze two Intel’s quad-core architectures: Sandy Bridge [1] and Ivy Bridge [2], fabricated in 32 nm and 22 nm technology, respectively. The floorplans of these two architectures are shown in Fig. 1. In particular, two high-performance processors are analyzed: i7-3770k as an example of the Ivy Bridge architecture and i7-2700k from the Sandy Bridge family. They have the same size of L3 cache (8 MB) and nominal operating frequency (3.5 GHz) as well as comparable core voltage at the nominal frequency. Floorplans are also very similar; the only noticeable difference is that Ivy Bridge has a more advanced (and therefore a little larger) graphics unit. The dynamic and static power for the entire chip for both Sandy Bridge (SB) and Ivy Bridge (IB) processors assumed in the analyses is based on the measured power data published in [3,4]. The power measurement methodology in those articles was based on measuring the current of processors under heavy load for various values of operating frequency, temperature and core voltage values. Based on these data, we evaluated that the total power dissipated in SB and IB processors at 3.5 GHz and at 1.06 V core voltage was 100 W and 85 W respectively. Both of the above values slightly exceed the Thermal Design Power (TDP) for these processors published by Intel. This is caused by the fact that the author used a dedicated application for the so-called torture testing, which is more power demanding than the applications used for determining TDP.

http://dx.doi.org/10.1016/j.mejo.2014.05.014
One interesting feature of the measurements presented in [3] and [4] is that they were performed for different values of operating frequency while maintaining the same temperature. Such an approach allows estimating the static power in the following manner: first, the total measured power is plotted against frequency. Next, by extrapolation, its component linearly dependent on frequency (dynamic power) is found. Then, we simply subtract dynamic power from total power to obtain static power. In the end, the static power was estimated at 19.9 W and 16.5 W for SB and IB, respectively.

However, for the purpose of our simulations, evaluating total power data was not enough; the data for particular processor units was needed. Given the total static and dynamic power, the power dissipation in individual processor blocks was estimated based on the several assumptions. In the first approximation, using the published SB and IB floorplans, the total dissipated power was distributed among four major units indicated in Fig. 2: 4 cores, processor graphics (PG), system agent and memory controller (SA) and the L3 cache. Furthermore, to better reflect the power density variation within a core, in the second approximation, each core was divided, as shown in the above figure, into three regions. One of these regions, CoreEX, corresponds to the core execution units and is therefore characterized by a higher power density. According to publicly available floorplans, core execution units are located in the top left corner of each core and have the area approximately equal to one-sixth of the total core area. Further details on the calculation of static and dynamic power dissipation in particular processor units are presented in the following subsections.

2.2. Static power

In the simplest approach, the static power may be distributed among processor blocks proportionally to their area. However, it would be most likely inaccurate, considering that the transistor density in regular memory-type blocks, such as the L3 cache memory, is much higher than in other blocks. Therefore, in our approach, the static power for L3 cache was estimated as being proportional to the number of transistors in cache, which can be easily calculated knowing the cache size and assuming six-transistor (6T) cells with 10% overhead due to the tag array and logic.

Then, the remaining static power can be distributed among other units according to their area. However, since cores are typically hotter than PG and SA, a slight correction is made; for cores an additional 10% of static power is added. Note that in our approach the fact that particular processor units have different power supply values was neglected. The static power distribution was carried out identically for both SB and IB processors.

2.3. Dynamic power

Determining the correct distribution of the dynamic power is a much more complex task because it significantly varies depending on the executed application. For the measurements published in [3,4], the authors used the application designed especially for processor testing i.e. Prime95 [6]. Thus, one may suppose that the graphics unit was not extensively used and, along with the SA unit, should be the coolest part of the chip. On the other hand, the cores should be the hottest units and the dynamic power density in the Ivy Bridge core may reach 0.9 W/mm² and for the execution part (CoreEX) even 1 W/mm².

Based on these power densities, we first calculated the dynamic power values for the cores for the IB processor. Then, the remaining amount of the dynamic power was distributed arbitrarily among SA, PG and L3 units. Next, the dynamic power for each unit of SB processor was calculated as a proportion between total...
dynamic power for the IB and SB processors. For example, if the dynamic power of the graphics unit amounts to 8.8% of the total dynamic power in the IB processor, then the same proportion was maintained in the case of the SB processor. Consequently, since the SB processor chip is larger, lower power densities were obtained. This method seems viable, since both processors, although manufactured in different technologies, have virtually identical architecture.

Tables 1 and 2 represent the final power trace data calculated for the IB and SB processors, which were then used in the thermal simulations whose results are presented and discussed in the following sections. Note that the processors comprise four cores, thus to calculate the actual total power based on the data from the tables, the numbers for core units should be of course multiplied by 4. Moreover, it should be noted that the CoreA and CoreB units have the same power density. The only reason why this region is divided into two separate units is that thermal tools that we used are capable of simulating only rectangular blocks.

### 3. Steady-state simulation

The thermal simulation results presented in this section were obtained by our dedicated thermal simulation tool which is able to solve heat equation using an analytical Green’s function solution method [5,11], where, unlike in numerical solvers, the simulation accuracy does not depend on the mesh size, but on the number of structure eigenvalues used in the simulations. In this case, the thermal maps for 10,000 nodes and 70 eigenvalues were computed in less than 2 min on a Core i7-based computer. The modelled structure has two layers, die and heat spreader. The convection occurs at the bottom of the spreader and is modelled with a heat exchange parameter, which was set to a practically attainable value of the total junction-to-case resistance of 0.5 K/W. All other boundary conditions were adiabatic.

The obtained simulation results are shown in Figs. 3–6. Two figures represent total temperature rise maps, while the other two only show the temperature rise due to the dissipation of static power. Note also that the temperature scale (color scale) is different for both analyzed processors. In addition, the exact values of minimal, average and maximal temperatures rise are given in Table 3.

Several interesting conclusions can be derived from the obtained results. As expected, the IB processor is indeed hotter than its predecessor; the maximal temperature rise in IB chip is 7.1 K higher than SB chip. Consequently, the fact that IB processors are characterized by higher temperatures than SB processors is not just the effect of using cheaper thermal paste (as was widely speculated among scientific community), but also simply because of the reduction of dimensions and therefore higher power density.

As far as static power is considered, recall that in planar technologies, its impact grew considerably with each technology node, mostly due to increasing subthreshold current. Therefore, one of the challenges for chip manufacturers was to ensure that the leakage power is not increased, or at least not increased as quickly with each technology node. Our results show that this goal was partially achieved. In both processors, the static power dissipation is highest in L3 cache and the maximal temperature rise due to static power is only 2.9 K higher in IB processor. It means that the reduction of leakage due to new technologies cannot fully compensate for the reduction of dimensions. However, it must be emphasized that it constitutes a significant improvement over planar technologies in which static power dissipation grew dramatically with each technology node.

One final observation that can be made is that the temperature gradient, i.e., the difference between the highest and lowest temperatures in the chip, is much higher in case of IB processor. Although it may be partially explained by the fact that the relatively cold graphics unit in IB processor is larger, one can still suppose that the gradient will increase with each technology node. Therefore, we may expect that this effect will become a problem in future technologies, as high temperature differences are a serious issue from a reliability point of view.

### 4. Transient thermal simulations

Since steady-state simulation can only partly shows the differences between two processors, it was decided to use transient thermal simulations to provide additional insights about the differences in thermal behavior between SB and IB chips. As a method of comparison, we chose the transient simulation of core swapping mechanism, also called activity migration. The idea of activity migration [8,9] in the area of multi-core processors relies on the concept of periodically exchanging workload between cores. In other words, two or more cores cooperate together so that the workload from the hottest core is moved to another core allowing the former to cool down. Thus, the temperature in the chip is distributed more equally and therefore the maximal temperature is minimized. Some researchers proposed the activity migration even at the level of particular processor units, in [10] authors propose to duplicate the hottest parts of a processor (typically execution units and register file) and periodically move the workload between them. It would seem that with multi-cores, activity migration should be even easier because no additional hardware is required: simply, when not all cores are in use, idle ones can be used as spares when the temperature of hot ones becomes too high. Meanwhile, working cores can even operate at higher frequency. In addition, switching workload between cores is a fairly trivial mechanism. However, as the constant miniaturization of dimensions with each technology node allows increasing the computational power of processors by putting more and more cores on the same die, it also increases the effect of thermal coupling between the cores. In other words, the closer distance

<table>
<thead>
<tr>
<th>Unit</th>
<th>Power (W)</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Static</td>
<td>Dynamic</td>
<td>Total</td>
</tr>
<tr>
<td>-----------</td>
<td>-----------</td>
<td>-------</td>
<td>-------</td>
</tr>
<tr>
<td>L3 cache</td>
<td>5.20</td>
<td>8.10</td>
<td>13.30</td>
</tr>
<tr>
<td>PG</td>
<td>4.21</td>
<td>6.00</td>
<td>10.21</td>
</tr>
<tr>
<td>SA</td>
<td>1.73</td>
<td>4.00</td>
<td>5.73</td>
</tr>
<tr>
<td>CoreA</td>
<td>0.67</td>
<td>6.38</td>
<td>6.85</td>
</tr>
<tr>
<td>CoreB</td>
<td>0.45</td>
<td>4.12</td>
<td>4.57</td>
</tr>
<tr>
<td>CoreEX</td>
<td>0.22</td>
<td>2.30</td>
<td>2.52</td>
</tr>
</tbody>
</table>

Table 2

Power breakdown for Sandy Bridge processor.

<table>
<thead>
<tr>
<th>Unit</th>
<th>Power (W)</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Static</td>
<td>Dynamic</td>
<td>Total</td>
</tr>
<tr>
<td>-----------</td>
<td>-----------</td>
<td>-------</td>
<td>-------</td>
</tr>
<tr>
<td>L3 cache</td>
<td>6.90</td>
<td>9.45</td>
<td>16.35</td>
</tr>
<tr>
<td>PG</td>
<td>3.46</td>
<td>7.00</td>
<td>10.46</td>
</tr>
<tr>
<td>SA</td>
<td>2.62</td>
<td>4.65</td>
<td>7.27</td>
</tr>
<tr>
<td>CoreA</td>
<td>0.86</td>
<td>7.24</td>
<td>8.10</td>
</tr>
<tr>
<td>CoreB</td>
<td>0.58</td>
<td>4.82</td>
<td>5.40</td>
</tr>
<tr>
<td>CoreEX</td>
<td>0.29</td>
<td>2.69</td>
<td>2.98</td>
</tr>
</tbody>
</table>
between two cores, the more the temperature of one core influences the temperature of the other. This in turn provokes the inevitable question of whether thermal management techniques based on activity migration will be still effective in these new technologies. Recall that for the activity migration to work, there should be a considerable temperature difference.
between “hot” and “cold” cores. For example, the following questions can be raised: if an idle core is located between two “hot” cores, will its temperature really be much lower than that of its neighbors? How will it affect the core swapping efficiency? How the effectiveness of activity migration will change with each new technology node?

Therefore, in this paper we investigate how effective is core swapping (activity migration) mechanism for reducing the maximal temperature in two modern quad-core processors. Moreover, we compare the results obtained for two processors manufactured in different technologies to evaluate the influence of technology scaling on transient thermal behavior of these chips.

A well-known Hotspot tool was used for thermal simulations. Hotspot uses an architectural dynamic compact model, i.e., the thermal behavior of a chip is modelled using an equivalent electrical RC circuit. In our work, we used the Hotspot’s “grid” model which means that the chip is partitioned into an array of rectangular blocks and each block is modelled by one node in the RC circuit. In our simulations the grid size of 128 x 64 was chosen, which constitutes a good compromise between good simulation accuracy and relatively short simulation time.

Hotspot model uses the following assumptions: the chip package is composed of four layers (from bottom to top): die, thermal interface material (TIM), heat spreader and heat sink. The heat is generated in the die layer. The heat dissipation from the top of the package to the ambient is modelled by one convection resistance (heat sink to ambient) which is a configurable parameter. The heat dissipation through other package sides is neglected (boundary conditions are considered adiabatic). Each layer is divided into a grid of elements. Each element is characterized by one capacitance, four lateral resistances (resistance to adjacent elements in the same layer) and two (or one) vertical resistances to the corresponding element in the layer above/below. For more information about the model, please refer to [12].

Material properties used for simulation include thermal conductivity, specific heat and density for all layers. They were found assuming that the die is made of silicon while heat spreader and heat sink of copper. For the TIM layer, thermal conductivity was set to 4 W/mK and the product of specific heat and density was set to 46 J/m³K.

The input to Hotspot is based on the data specified in Tables 1 and 2. Using the obtained power data (as explained in Section 2), we generate power trace files for the entire quad-core processor which serve as inputs to Hotspot. For the sake of simplicity, we assume that the execution of the benchmark produces constant power dissipation. We believe that this assumption is understandable, given that the difference in power dissipation between working and idle cores is much higher than the variations of power dissipation during the execution. We also assume that when a core is executing, it dissipates both static and dynamic power, whereas when it is idle, it only dissipates static power. We also neglect the time needed to perform the core swap, as it is much shorter than the core swapping period. The core swapping frequency was set to 500 Hz, which according to the results presented in [13,15] should not cause significant performance degradation. We also arbitrarily chose the core swapping pairs: core 0 exchanges workload with core 1 and core 2 exchanges workload with core 3. Our choice was based on experiments which showed that such a configuration produces the best results. In addition, since only two cores at a time are under heavy load, we assumed that their frequency can be increased by 20% (such a technique is well known, see for example Intel’s Turbo Boost technology [14]). Therefore, the dynamic power data from Tables 1 and 2 was scaled accordingly.

Most technological and other simulation parameters were set to Hotspot’s default values; however some of them were modified to values better corresponding to the parameters of modern processors. For example, chip thickness was changed to 765 μm and the thermal interface thickness was changed to 60 μm. It is also worth mentioning that the thermal interface material (TIM) conductivity in our simulations was the same for both processors. Although in reality this is not correct (Intel changed thermal interface material used in SB for a cheaper one in IB), it allows eliminating the impact of TIM on temperatures and, therefore, analyze only the impact of scaling and technology.

Before running transient simulations, it was decided to look first at steady-state temperatures in the chip with two idle cores. Perhaps the best way to visualize the results is presenting the temperature profile across the cross-section of the chip (see Fig. 2 for the used cross-section and Figs. 7 and 8 for the results). The results show that in SB processor the difference between active and idle cores reaches 11 K, whereas the same difference for IB chip is only 8 K. The reason is that in a smaller chip the influence of the temperatures of adjacent active cores on the idle one is greater. Hence, it may be supposed that the reduction of dimensions outweighed the reduction in leakage power obtained thanks to the introduction of Tri-Gate transistors. Therefore, one may expect that the temperature differences between active and idle cores in future processors will become even smaller, unless manufacturers decide to redesign the processor’s floorplan.

As an output of transient simulation, Hotspot is able to compute the temperature of each grid block at every time instant. From this data, the user can extract the average, minimal or maximal temperatures for each processor unit. In what follows, whenever one temperature value is used to describe the temperature of an unit, it always indicates the maximal temperature found in the grid blocks which correspond to this unit.

Following the guidelines from [12], when performing transient simulations, we first perform a steady-state run and then use the results as initial values for the transient run. Since the thermal constant of the package is quite large, such an approach is needed because otherwise it would be necessary to run dozens of minutes of transient simulation to allow the package to heat up. Of course such long simulation would take prohibitively long time even on a very powerful PC.

Although during simulations the ambient temperature was set to 30 °C, in the results, on the y axis the value of temperature rise...
was used. When performing the simulations it was also noticed that the location of a core plays an important role when it comes to cooling. We discovered for example that core 0 has a lower steady-state temperature because it is adjacent to graphics unit which has relatively low dissipated power density. Consequently, for example in IB processor, when swapping the workload with core 1, core 0 can be in execution mode 58% of the time, while core 1 only 42% of the time. The same percentages for cores 2 and 3 are 55% and 45%, respectively. For SB processor, the relative execution times for cores 0–3 were 57%, 43%, 49% and 51%, respectively. Using such a workload distribution, it was possible to obtain almost the same maximal temperatures for all cores, i.e., the case when core swapping mechanism was most effective.

For IB chip, the maximal steady-state temperature rise was equal to 38 K in two active cores (see Fig. 7). When we applied the cores swapping mechanism, the maximal temperature slightly exceeded 33 K (see Fig. 9), constituting a 5 K reduction. Other interesting conclusions can be also derived from the results, for example, the maximal temperature rise of cores 2 and 3 is almost never lower than 32 K, even when they are idle; one can clearly see here the effect of thermal coupling. Only core 0 (which is located close to the relatively cool PG unit) is able to cool down a little more when idle.

In the case of IB processor it was discovered that without core swapping mechanism the maximal temperature rise in the chip (i.e. the maximal temperature rise of two working cores) equaled almost 41 K (see Fig. 8). Meanwhile, as shown in Fig. 11, when core swapping mechanism is implemented, the maximal temperature rise is only about 36 K. Thus, the results are fairly similar to those of its predecessor (5 K reduction). Moreover, we see a similar effect of thermal coupling: idle cores are able cool down normally in their centers, i.e., their temperatures are not influenced by the rising temperatures of other cores. However, as shown previously, the maximal temperature in a unit can be much higher due to thermal coupling from other cores. This puts into question relying on the data read from built-in temperature sensors present in modern Intel processors. Such sensors, which are certainly located in the hottest part of the core, will show correctly the maximal temperature of the core when it is active. However, when the core is idle, its maximal temperature may not correspond to that indicated by the sensor. Although this fact may not be of

Fig. 8. Temperature profile across IB processor (with 2 idle cores).

Fig. 9. Transient simulation with core swapping mechanism for SB processor.

Fig. 10. Transient simulation with core swapping mechanism at 19% higher operating frequency for SB processor.

We also performed additional simulations to discover by how much we can increase the operating frequency so that the temperature rise does not exceed the temperature reached without swapping. After several experiments, it was discovered, that for SB chip it was possible to increase the frequency by another 19% with respect to its previous value. The same potential frequency increase for the IB chip was a little lower and equalled 17%. Figs. 10 and 11 show the temperature rise for all cores when the operating frequency was increased; it can be observed that the temperature rise is around 38 K for SB and 41 K for IB, i.e., the same temperatures that were obtained without core swapping mechanism (see Figs. 7 and 8), although the processors were running at 19% (SB) and 17% (IB) higher frequency.

Consequently, we may conclude that the impact of core swapping technique was very similar in SB and IB chips; in both processors it was possible to either minimize the maximal temperature by 5 K or increase the operating frequency by 19% (SB) or 17% (IB) and maintain the same temperature as in the case without core swapping.

To investigate the impact of the temperature of neighboring cores, one more set of simulations was run. Figs. 13 and 14 represent the result of the same simulations as Figs. 9 and 11, but the curves represent the temperature in the center of a core execution unit (CoreEX) instead of its maximal temperature. The difference is clear: during the core swapping, the cores are able cool down “normally” in their centers, i.e., their temperatures are not influenced by the rising temperatures of other cores. However, as shown previously, the maximal temperature in a unit can be much higher due to thermal coupling from other cores. This puts into question relying on the data read from built-in temperature sensors present in modern Intel processors. Such sensors, which are certainly located in the hottest part of the core, will show correctly the maximal temperature of the core when it is active. However, when the core is idle, its maximal temperature may not correspond to that indicated by the sensor. Although this fact may not be of
primary importance, as most often we are interested in the core temperature when it is active, it may not always be negligible when using various Dynamic Thermal Management (DTM) techniques which heavily rely on the sensor data. It may even be advisable to use several temperature sensors in each core unit in future processor generations which would provide a better outlook of temperature distribution within a core.

5. Conclusions

When moving to next technology node, the maximal temperature in the chip can be only maintained at the same level if the power density is kept constant (assuming the same cooling conditions). It means that the dissipated power should be reduced because the area gets smaller. However, from the technological perspective, this is very difficult to achieve.

The results of thermal simulations presented in this paper clearly demonstrated that even in new FinFET technologies the processors get hotter when migrating to the next technology node. However, one important conclusion is that, thanks to the introduction of FinFET-based technologies, the dramatic increase of static power dissipation with each node was mitigated, which constitutes a significant improvement over the pessimistic forecasts from a couple of years ago [7]. Currently, one issue which should certainly be tackled in the future is the rising temperature gradient in the chip. Obviously the results presented in this paper were obtained for partly approximate power trace data, however since the same approximations we used in case of both processors, it should not significantly affect the conclusions derived from their comparison.

It was also shown that thermal coupling between cores increases with technology scaling, although it should be also emphasized that the transient thermal behavior of both Sandy Bridge and Ivy Bridge chips was quite similar. Moreover, it was discovered that the temperature reported by a sensor of an idle core may not always be the real maximal temperature of this core.

We also demonstrated that the mechanisms for reducing hotspot temperatures based on activity migration may be less effective in future technologies. Although the effectiveness may somewhat improve if there are more cores on chip due to the possibility of moving workload between a higher number of cores, the more important factor is the increase of static power density with each technology node which reduces the temperature difference between working and idle cores and therefore puts into question the effectiveness of exchanging workload.

Acknowledgment

This research was supported by the grant of Polish National Center of Science No. N515 5091 40.

References


Please cite this article as: P. Zajac, et al., Evaluating the impact of scaling on temperature in FinFET-technology multicore processors, Microelectron. J (2014), http://dx.doi.org/10.1016/j.mejo.2014.05.014

